PCM-3753I

**96-channel Digital I/O
PCI-104 Module**

User Manual

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CE Notification

PCM-3753I developed by ADVANTECH CO., LTD., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

Printed in Taiwan   February 2008

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

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2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.

3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.

4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.

5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Technical Support and Assistance

Step 1. Visit the Advantech web site at **www.advantech.com/support** where you can find the latest information about the product.

Step 2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
- Product name and serial number
- Description of your peripheral attachments
- Description of your software (operating system, version, application software, etc.)
- A complete description of the problem
- The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

• 1 x PCM-3753I

• 1 x CD-ROM

• 1 x Startup Manual

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.

2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

Contents

General Information

Chapter 1 General Information

1.1 Introduction

The PCM-3753I is a 96-ch digital I/O PCI-104 module. The card emulates mode 0 of the 8255 PPI chip, but the buffered circuits offer a higher driving capability than the 8255. The 96 I/O lines are divided into twelve 8-bit I/O ports: A0, B0, C0, A1, B1, C1, A2, B2, C2, A3, B3 and C3. Users can configure each port as input or output via software.

Dry Contact Support for Digital Input

Each digital input channel at the PCM-3753I accepts either 0 ~ 5 VDC wet contact or dry contact inputs. This dry contact capability allows the channel to respond to changes in external circuitry (e.g., the closing of a switch in the external circuitry) when no voltage is present in the external circuit.

Reset Protection Fulfills the True Requirement of Industrial Applications

When the system is hot reset (the power is not turned off), the PCM-3753I can either retain the last I/O port settings and outputs value, or return to its default configuration, depending on the jumper setting. This function protects the system from wrong operations during unexpected system resets.

Interrupt Functions Ensure Faster System Response

Two lines of each port C (i.e., ports C0, C1, C2 and C3) are connected to an interrupt circuit. The "Interrupt Control Register" of the PCM-3753I controls how these signals generate an interrupt. More than one interrupt request signals can be generated at the same time, and then the software can process these request signals by ISR. The multiple interrupt sources provide the card with more capability and flexibility.

The PCM-3753I also provides "Pattern Match" interrupt function for port A0. The card monitors the states of port A0 and compares them with a pre-set pattern. When the received state matches the pre-set pattern, the PCM-3753I generates an interrupt signal to the system.

"Change of State" interrupt function is provided at port B0. When any signal line of port B0 changes its state, the card generates an interrupt to the system to handle this event.

These interrupt functions release the CPU from the burden of pulling all I/O points, enabling a PC to handle more I/O points with higher performance.

1.2 Features

- 96 TTL digital I/O lines
- Emulates mode 0 of 8255 PPI
- Buffered circuits for higher driving capacity than 8255
- Multiple-source interrupt handling
- Output status read-back
- "Pattern match" and "Change of state" interrupt functions for critical I/O monitoring
- Keeps I/O setting and digital output values when hot system reset
- Supports dry contact and wet contact
- 50-pin pin header
- BoardID switch

1.3 Applications

- Industrial AC/DC I/O devices monitoring and controlling
- Relay and switch monitoring and controlling
- Parallel data transfer
- TTL, DTL and CMOS logic signal sensing
- Indicator LED driving

1.4 Specifications

I/O Channels	96 digital I/O lines
Programming Mode	8255 PPI mode 0
Input Signal	Logic level 0: 0.8 V max. Logic level 1: 2.0 V min.
Output Signal	Logic level 0: 0.44 V max. @ 24 mA (sink) Logic level 1: 3.76 V min. @ 24 mA (source)
Transfer Rate	1.6 Mbytes/sec (tested under DOS, K6 300MHz CPU)
Power Consumption	+5 V @ 105 mA (typical) +5 V @ 210 mA (max.)
Operating Temperature	0 ~ 60° C (32 ~ 140°F) (refer to IEC 68-2-1, 2)
Storage Temperature	-20 ~ 70° C (-4 ~ 158°F)
Operating Humidity	5 ~ 95%RH non-condensing (refer to IEC 68-2-3)
Connector	Four 50-pin box header
Dimensions	96 x 90 mm (3.8" x 3.5")

1.5 Pin Assignments (CN0~CN3)

Assignment		Pin	Assignment	Pin
Port C Hi	PC7	1		2
	PC6	3		4
	PC5	5		6
	PC4	7		8
Port C Lo	PC3	9		10
	PC2	11		12
	PC1	13		14
	PC0	15		16
Port B	PB7	17		18
	PB6	19		20
	PB5	21	All Even Numbered Pins are GROUND	22
	PB4	23		24
	PB3	25		26
	PB2	27		28
	PB1	29		30
	PB0	31		32
Port A	PA7	33		34
	PA6	35		36
	PA5	37		38
	PA4	39		40
	PA3	41		42
	PA2	43		44
	PA1	45		46
	PA0	47		48
+5 VDC		49		50

Installation

Chapter 2 Installation

2.1 Initial Inspection

Before starting to install the PCM-3753I, make sure there is no visible damage on the card. We carefully inspected the card both mechanically and electrically before shipment. It should be free of marks and in perfect order on receipt.

As you unpack the PCM-3753I, check it for signs of shipping damage (damaged box, scratches, dents, etc.). If it is damaged or fails to meet its specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing materials for inspection by the carrier. We will then make arrangements to repair or replace the unit.

2.2 Unpacking

The PCM-3753I contains components that are sensitive and vulnerable to static electricity. Discharge any static electricity on your body to ground by touching the back of the system unit (grounded metal) before you touch the board.

Remove the PCM-3753I card from its protective packaging by grasping the card's rear panel. Handle the card only by its edges to avoid static discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, please store the card in this package for its protection.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

2.3 Jumper Settings

We designed the PCM-3753I with ease-of-use in mind. It is a "plug and play" card, i.e. the system BIOS assigns the system resources such as base address and interrupt automatically. The following section describes how to configure the card. You may want to refer to the figure below for help in identifying card components.
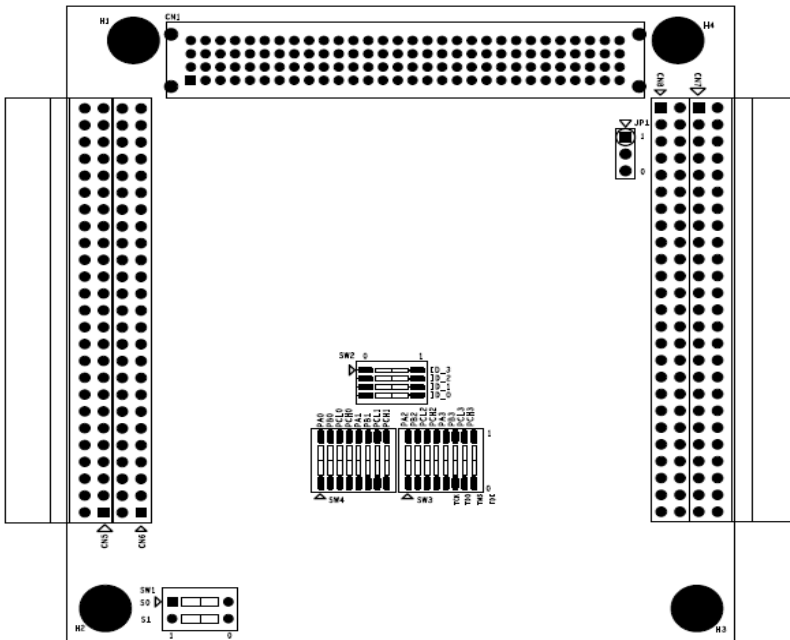
Figure 2.1: Location of Connectors and Jumpers

Jumper Settings to Set Ports as Input or Output by Software

When the two pins of jumpers JPA0, JPB0, JPC0L, JPC0H, JPA1, JPB1, JPC1L, JPC1H, JPA2, JPB2, JPC2L, JPC2H, JPA3, JPB3, JPC3L or JPC3H are not shorted (i.e., by setting a jumper), the corresponding ports are set to be configurable as input or output ports by software. (JPA0 means jumper for port A0, JPB0 means jumper for port B0, etc. See Table 2-1) If jumper JP1 is not enabled (i.e., by shorting the upper two pins of JP1), all ports configured by software are automatially set as input ports during system startup a reset, with a default signal level of logic 1(high). (But see Jumper JP1 discussion below.)

Using Jumpers to Set Ports as Output Ports

By shorting the two pins of the jumpers JPA0, JPB0, JPC0L, JPC0H, JPA1, JPB1, JPC1L, JPC1H, JPA2, JPB2, JPC2L, JPC2H, JPA3, JPB3, JPC3L or JPC3H, a user sets the corresponding ports to be output ports. (JPA0 means jumper for port A0, JPB0 means jumper for port B0, etc.) Shorting the two pins of a port's jumper disables the port from being software configurable as an input port. The initial state of each of these ports after system power on or reset will be logic 0 (voltage low), unless jumper JP1 determines otherwise. (See JP1 below.)

Jumper JP1 Restores Ports to Their Condition Prior to Reset

Jumper JP1 gives the PCM-3753I a new and valuable capability. With JP1 enabled (i.e., by shorting the lower two pins of JP1), the PCM-3753I "memorizes" all port I/O settings and output values, and, in the event of a "hot" reset, the settings and output values present at the port just prior to reset are restored to each port following reset. This feature applies to both ports set by software, and to ports configured as output ports via jumper. Depending on the application, this capability may allow a card to be reset without requiring a complete shutdown of processes controlled by the card (since port values are left unchanged and are interrupted only momentarily).

Complete loss of power to the chip clears chip memory. Thus, even if JP1 is enabled, if the power to the card is disconnected, the card's initial power-on state will be the state of an input port with voltage high input (for software-set ports) or the state of an output port with voltage low output (for jumper-set ports).

When jumper JP1 is not enabled both power-off and reset results in ports returning to the state of an input port with voltage high input or returning to the state of output port with voltage low output (for jumper-set ports).

Table 2.1: Summary of Jumper Settings		
Jumpers	**Function Description**	
JP1		Keep the last digital output status after hot reset
JP1		Load default configuration while hot reset (Default)

2.4 Setting the BoardID Switch (SW2)

You can use the BoardID command (0x20) to get the board's unique identifier. PCM-3753I has a built-in BoardID SMD switch (SW2), which is used to define each card's unique identifier. You can determine the identifier in the register as shown in Table 2.2. When there are multiple cards on the same chassis, this BoardID setting is useful for identifying each card's device number. We set the PCM-3753I's BoardID switch to 0 at the factory. If you need to adjust this setting, please see below.

Table 2.2: BoardID Setting (SW2)				
BoardID (DEC)	**Switch Position**			
	ID3	**ID2**	**ID1**	**ID0**
0*	ON	ON	ON	ON
1	ON	ON	ON	OFF
2	ON	ON	OFF	ON
3	ON	ON	OFF	OFF
4	ON	OFF	ON	ON
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	ON
7	ON	OFF	OFF	OFF
8	OFF	ON	ON	ON
9	OFF	ON	ON	OFF
10	OFF	ON	OFF	ON
11	OFF	ON	OFF	OFF
12	OFF	OFF	ON	ON
13	OFF	OFF	ON	OFF
14	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF
* : Default				

2.4.1 BoardID Register

You can determine the BoardID setting in the register as shown below.

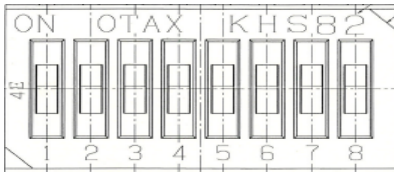| Table 2.3: BoardID register of PCM-3753I				
Base+20	3	2	1	0
Abbreviation	ID3	ID2	ID1	ID0

Note: ID0: The least significant bit (LSB) of BoardID

ID3: The most significant bit (MSB) of BoardID

2.5 SW3 & SW4 Settings

When set to "On (0)", the Digital Port will be set to Output.

When set to "Off (1)", the Digital Port will be set by software. (Default)

2.6 Hardware Installation

1. Turn the PC.s power off. Turn off the power of any peripheral devices such as printers and monitors.

2. Disconnect the power cord and any other cables from the back of the computer.

3. Remove the system unit cover (see the user.s guide for your chassis if necessary).

4. Remove the CPU card from the chassis (if necessary) to gain access to the card.s PCI-104 connector.

5. Connect connector J1 of the PCM-3753I card to the PCI-104 connector. Carefully align the pins with the PC-104 connector. Slide the module into the connector. The module pins may not slide all the way into the connector; do not force the pins into place, or the module may be damaged.

6. Fasten the module to the CPU card by using the included brass screw. Screw the brass spacer into the threaded hole on the CPU card. Do not tighten too much, or the threads may be damaged.

7. Attach any accessories to the PCM-3753I using 50 pin flat cables.

8. Reinstall the CPU card and replace the system unit cover. Reconnect the cables you removed in step 2. Plug in and turn on the power. This completes the hardware installation. Install the software driver as described in the following section.

Operation

Chapter 3 Operation

3.1 Overview

This chapter describes the operating characteristics of the PCM-3753I. The driver software bundled with this card allows a user to access all of the card's functions without register level programming. Please see the User's Manual included on the driver CD-ROM for more information. For users who prefer to implement their own bit-level programming to drive the card's functions, information useful for making such a program is included in this chapter.

3.2 Digital I/O Ports

3.2.1 Introduction
The PCM-3753I each emulate four 8255 programmable peripheral interface (PPI) chips in mode 0, but with higher driving capability than a standard 8255 chip. Each of these 8255 chip emulators has 24 programmable I/O pins that are divided into three 8-bit ports. The total 96 digital I/O pins on the PCM-3753I is divided into 12 ports, designated PA0, PB0, PC0, PA1, PB1, PC1, PA2, PB2, PC2, PA3, PB3 and PC3. Each port can be programmed as an input or an output port. The I/O pins in port A0 are designated PA00, PA01,..., PA07; the pins in port B0 are designated PB00, PB01,..., PB07, etc. These port names are used both in this manual and in the software library. Please refer to Section 1.5, Pin Assignments.

3.2.2 8255 Mode 0
The basic 8255 mode 0 features included on the PCM-3753I cards are:

• 8-bit I/O ports - port A (PA) and port B (PB)

• Port C is divided into two nibble-wide (4-bit) I/O ports - PC upper and PC lower

• Any port can be used for either input or output.

• Output status can be read back.

3.2.3 Input/Output Control

A control word can be written to a port's configuration register (Base+3, 7, 11 and 15 respectively for ports 0, 1, 2 and 3 on the PCM-3753I, and Base+35, 39, 43 and 47 respectively for ports 0, 1, 2 and 3 on the PCM-3753IE) to set the port as an input or an output port, unless the ports are set as output ports via jumpers (refer to Section 2.3, Jumper Settings). Table 3-1 shows the format of a control word.

Table 3.1: Bit map of port configuration register							
D7	D6	D5	D4	D3	D2	D1	D0
Not read	Not read	Not read	PortA 0: output 1: input	Port C higher bits 0: output 1: input	Not read	Port B 0: output 1: input	Port C lower bits 0: output 1: input

Note   *A control word has no effect if the corresponding port is set as an output port by a jumper.*

Warning   *Before setting any port as an output port via software, make sure that a safe output value has also been set. An output voltage will appear at the pins immediately following the control word taking effect. If no output value was specified, the value will be indeterminate (either 0 or 1), which may cause a dangerous condition.*

3.2.4 Initial Configuration

The initial configuration of each port depends on the input/output jumper setting of each port, on the setting of the jumper JP1, and on whether the power was actually disconnected or whether the system was hot reset.

If jumper JP1 is not enabled, all ports configured by software are automatically set as input ports during system start up or reset, with a default signal level of logic 1 (high). All ports set via jumpers as output ports are set as output ports during system start up or reset, signal level logic 0 (0 V).

If the jumper JP1 is enabled and the initial configuration is caused by a reset, all ports will return to the states they had just prior to the reset. The reset must be a "hot" reset (power not disconnected) for enabled JP1 to return ports to their prior values. Otherwise, the card behaves as though JP1 were not enabled. Please refer to "Jumper settings" in Chapter 2 for more information.

3.2.5 Dry Contact Support for Digital Input

Each digital input channel accepts either dry contact or $0 \sim 5$ VDC wet contact inputs. Dry contact capability allows the channel to respond to changes in external circuitry (e.g., the closing of a switch in the external circuitry) when no voltage is present in the external circuit. Figure 3-1 shows external circuitry with both wet and dry contact components, connected as an input source to one of the card's digital input channels.
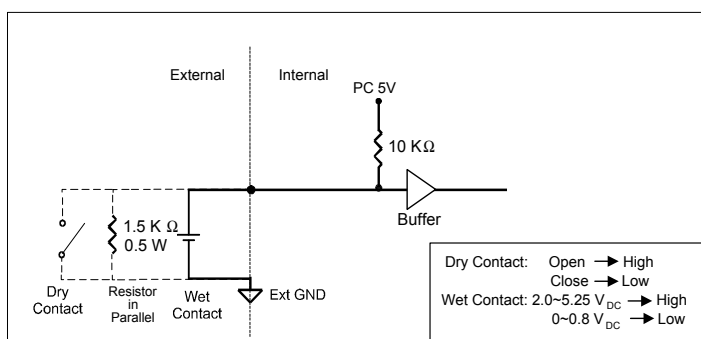
Figure 3.1: Wet and dry contact inputs

Note   For wet contact configurations, a malfunction
            may occur if the internal resistance of the voltage
            source is significant (> 1.5 kW). It is advisable to
            connect a 1.5 kW resistor in parallel with such a
            voltage source to avoid a voltage rise inside the
            voltage source.

3.3 Interrupt Functions

3.3.1 Introduction
Two lines of each I/O port C, plus ports A0 and B0, are connected to the interrupt circuitry. The "Interrupt Control Register" of the PCM-3753I controls how the combination of these signals generates an interrupt. Six interrupt request signals can be generated at the same time, and then the software can service these six request signals by IRQ. The multiple interrupt sources provide the card with more capability and flexibility.

3.3.2 IRQ Level
The IRQ level is set automatically by the PCI plug-and-play BIOS and is saved in the PCI controller. There is no need for users to set the IRQ level. Only one IRQ level is used by this card, although it has six interrupt sources.

3.3.3 Interrupt Control Registers
The "Interrupt Control Registers" (Base + 16, 17, 18 and 19 for the PCM-3753I, and Base + 48, 49, 50 and 51 for the PCM-3753IE) control the interrupt signal sources, edges and flags. The following table shows the bit map of each interrupt control register. These registers are readable/writable. When writing to one of them, it is used as a control register, and when reading from it, it is used as a status register.

Table 3.2: Interrupt control register bit map								
Base+16/48	Port 0							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F0	E0	M01	M00	F02	M2	F01	M1
Base+17/49	Port 1							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F1	E1	M11	M10	-	-	-	-
Base+18/50	Port 2							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F2	E2	M21	M20	-	-	-	-
Base+19/51	Port 3							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F3	E3	M31	M30	-	-	-	-

Mn0 and Mn1: "mode bits" of port Cn (n = 0 ~ 3)

M1: pattern match port enable control bit of port A0

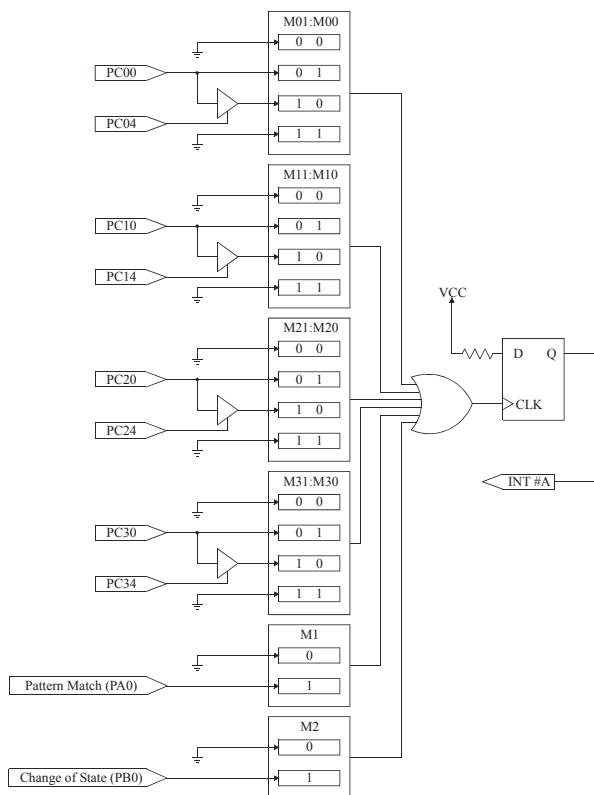M2: change of state port enable control bit of port B0

En: triggering edge control bit (n = 0 ~ 3)

Fn: interrupt flag bit of port Cn (n = 0 ~ 3)

F01: pattern patch interrupt flag bit of port A0

F02: change of state interrupt flag bit of port B0

Figure 3.2: Interrupt sources

3.3.4 Interrupt Source Control

The "mode bits" in the interrupt control registers determine the allowable sources of signals generating an interrupt. For the PCM-3753I, bit 4 and bit 5 of Base+16 determines the interrupt source of port C0, bit 4 and bit 5 of Base+17 determines the interrupt source for port C1, and so forth. Because of sharing the same PCI controller with the PCM-3753I, the PCM-3753IE's interrupt sources are also controlled by the PCM-3753I's interrupt control register. Bit 4 and bit 5 of Base+48 determines the interrupt source of port C0 on the PCM-3753IE, bit 4 and bit 5 of Base+49 determines the interrupt source of port C1, and so forth. Please refer the table in Appendix A to find the corresponding address for the interrupt source control of each port C.

The following table shows the relationship between an interrupt source and the values in the mode bits.

Table 3.3: Interrupt mode bit values					
Base+16/48		**Port 0**	**Base+17/49**		**Port 1**
M01	M00	Description	M11	M10	Description
0	0	Disable interrupt	0	0	Disable interrupt
0	1	Source = PC00	0	1	Source = PC10
1	0	Source = PC00 and PC04	1	0	Source = PC10 and PC14
1	1	Disable interrupt	1	1	Disable interrupt
Base+18/50		**Port 2**	**Base+19/51**		**Port 3**
M21	M20	Description	M31	M30	Description
0	0	Disable interrupt	0	0	Disable interrupt
0	1	Source = PC20	0	1	Source = PC30
1	0	Source = PC20 and PC24	1	0	Source = PC30 and PC34
1	1	Disable interrupt	1	1	Disable interrupt

3.3.5 Interrupt Triggering Edge Control

The interrupt can be triggered by a rising edge or a falling edge of the interrupt signal, selectable by the value written in the "triggering edge control" bit in the interrupt control register, as shown in following table.

Table 3.4: Triggering edge control bit values	
En (n = 0 ~ 3)	Triggering edge of interrupt signal
1	Rising edge trigger
0	Falling edge trigger

3.3.6 Interrupt Flag Bit

The "interrupt flag" bit is a flag indicating the status of an interrupt. It is a readable and writable bit. Read the bit's value to find the status of the interrupt; write "1" to this bit to clear the interrupt. This bit must be cleared in the ISR to service the next incoming interrupt.

Table 3.5: Interrupt flag bit values		
F01, F02 and Fn (n = 0 ~ 3)		Interrupt Status
Read	1	Interrupt exists
	0	No interrupt
Write	1	Clear interrupt
	0	Don't care

F01: pattern patch interrupt flag bit of port A0

F02: change of state interrupt flag bit of port B0

Fn: interrupt flag bit of port Cn (n = 0 ~ 3)

3.3.7 Pattern Match Interrupt Function

The PCM-3753I provides the pattern match interrupt function for port A0. It monitors the status of the enabled input channels, which are chosen in Base+24 (or Base+56 for the PCM-3753IE), and compares the received state values with the pre-set state values written in Base+20 (Base+52 for the PCM-3753IE). When the actual state values match the pre-set state values, the PCM-3753I will deliver an interrupt signal to the system. This function releases the CPU from the burden of polling all of the I/O points, enabling a PC to handle more I/O points with higher performance. The following is an example.

Example 3.1 Assume that the pattern match function for the I/O channels PA01, PA02, PA06 and PA07 of the PCM-3753I is enabled (i.e. PA00, PA03, PA04 and PA05 on the PCM-3753I and port A0 on the PCM-3753IE are ignored during the pattern match monitoring process). The user can set the pattern match values for the enabled input channels, and these will be compared to the actual channel states of the enabled channels. The following is an example.

a) First, enable the pattern match interrupt function for channels PA01, PA02, PA06 and PA07

Bit #	7	6	5	4	3	2	1	0
Base+24	1	1	0	0	0	1	1	0

b) Write the pre-set pattern-match state of the enabled channels

Bit #	7	6	5	4	3	2	1	0
Base+20	1	0	X	X	X	1	1	X

c) Finally, enable the pattern match function for port A0 of the PCM-3753I by writing a "1" in bit 0 of Base+16.

M2	Description
1	Enable the change of state interrupt function for port A0
0	Disable the change of state interrupt function for port A0

d) When the input signals at channels PA01, PA02 and PA07 are high and PA06 is low, an interrupt signal will be generated. This result is not affected by the states of channels PA00, PA03, PA04 and PA05.

3.3.8 Change of State Interrupt Function

The PCM-3753I also provides the change of state interrupt function for port B0. It monitors the status of the enabled channels of port B0, which are chosen in Base+28 (or Base+60 for the PCM-3753IE). When one of the enabled channels changes its state, the PCM-3753I delivers an interrupt signal to the system to handle this event. The following is an example.

Example 3.2 Assume that the change of state interrupt function for the I/O channels PB01, PB02, PB06 and PB07 on the PCM-3753IE are enabled (i.e. the signals in PB00, PB03, PB04 and PB05 on the PCM-3753IE and port B0 of the PCM-3753I are ignored during the change of state process). When a change of state occurs in either PB01 or PB02 or PB06 or PB07, an interrupt signal will be delivered to the system.

a) First, enable the change of state interrupt function for PB01, PB02, PB06 and PB07 of the PCM-3753IE.

Bit #	7	6	5	4	3	2	1	0
Base+60	1	1	0	0	0	1	1	0

b) Then, enable the change of state interrupt function for port B0 of the PCM-3753IE by writing a "1" in bit 2 of Base+48.

M2	Description
1	Enable the change of state interrupt function for port A0
0	Disable the change of state interrupt function for port A0

c) When a change of state occurs in PB01 or PB02 or PB06 or PB07 on the PCM-3753IE, an interrupt signal is generated.