pqi

DiskOnModule

Turbo DH 88 Series

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1. Product Description
1.1 Product Overview
CoreSolid Storage designs DiskOnModule (DOM) in PQI brand name is the storage device based on NAND flash memory technology. This product complies with 44 PIN IDE (ATA) standard interface and is suitable for data storage media and code storage device for embedded system and boot disk. By using **DiskOnModule,** it is possible to operate good performance for the systems, which have IDE interface.

With small form factor, the applicable appliance can add or install IDE storage device on its Mother Board or Complete set.

- **Application Fields;**
  - Industrial PC and Thin Client
  - Game and Telecommunication Machine
  - Ticketing, Examining, testing machine
  - Army, Health and Production Equipment and Machine

1.2 Product Features
- Small form factor with IDE (ATA) Standard Interface connector
- Memory Capacities: 32MB ~ 6GB
- High performance and reliability
- Noiseless and stable installation to system
- Operating voltage 3.3V or 5.0V operation
- Standard IDE (ATA) Interface
- Operating as Boot Disk
- Data Storage Device to 6GB
- Code Storage Device for Embeded Operating System

1.3 System Requirement
- The Host system which is connected to DiskOnModule should meet system requirements at minimum;

1.3.1 Power Requirement
- Voltage: DC +3.3V ± 5% or DC +5.0V ± 10%

1.3.2 Operating System
- Windows 2000/XP
- Linux
- DOS
- WinXP Embedded
- WinCE

1.3.3 Interface
- IDE (ATA) Standard Interface

2. Specification
2.1 Physical Specifications

2.1.1 Overlook
The overlook views of DiskOnModule are illustrated in Figure 1.

<Front View>   **<Rear View>**
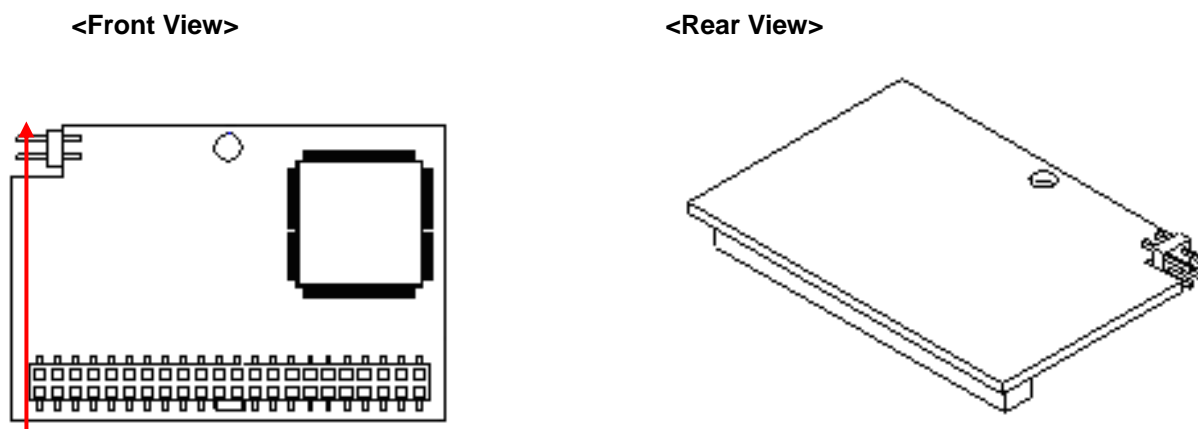
M/S JUMPER

Figure 1: DiskOnModule Overlook Diagram

2.1.2 Dimension

The Dimensions of DiskOnModule are illustrated in Figure 2 and described in Table 1.

DH0XXXX88XX1 (44 PIN)
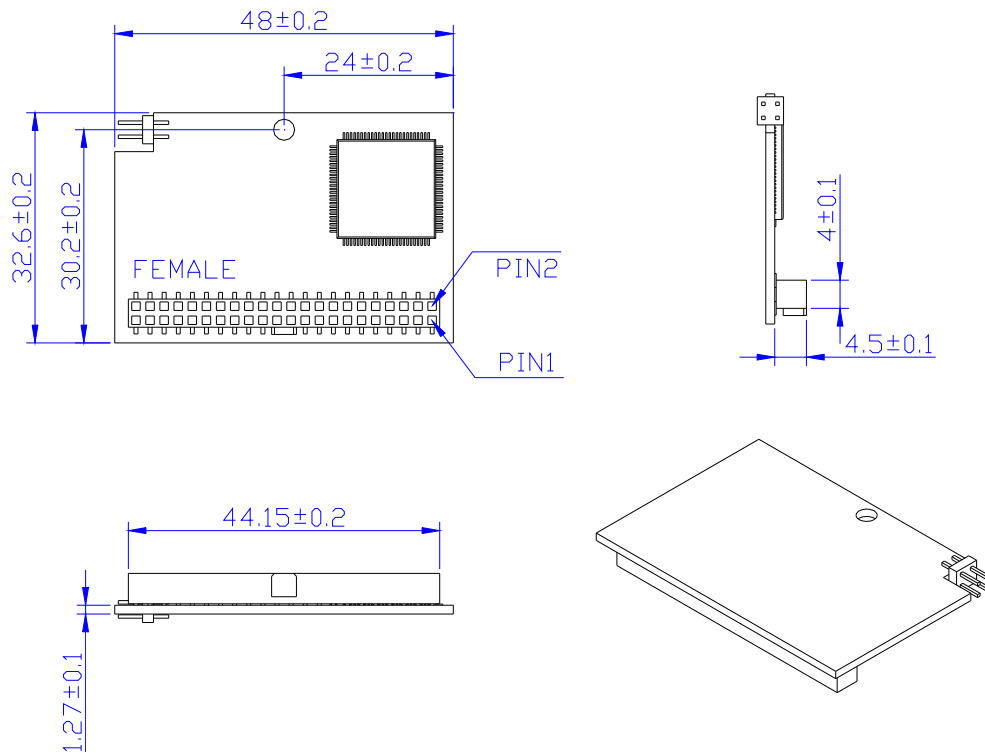
DH0XXXX88XX2 (44 PIN)
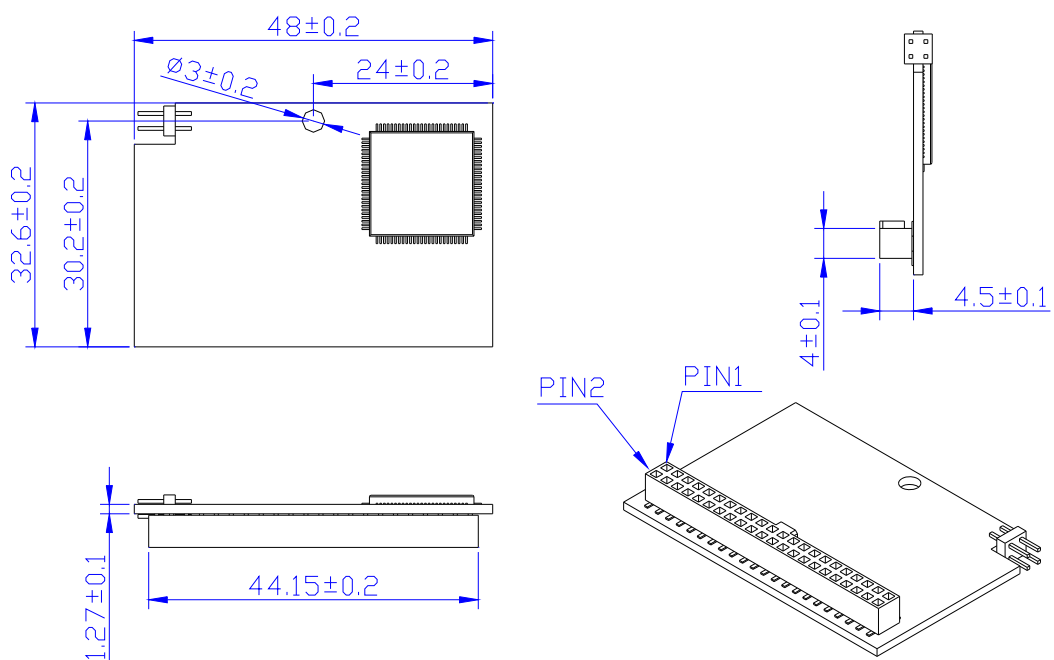
DH0XXXX88XX3 (44 PIN)
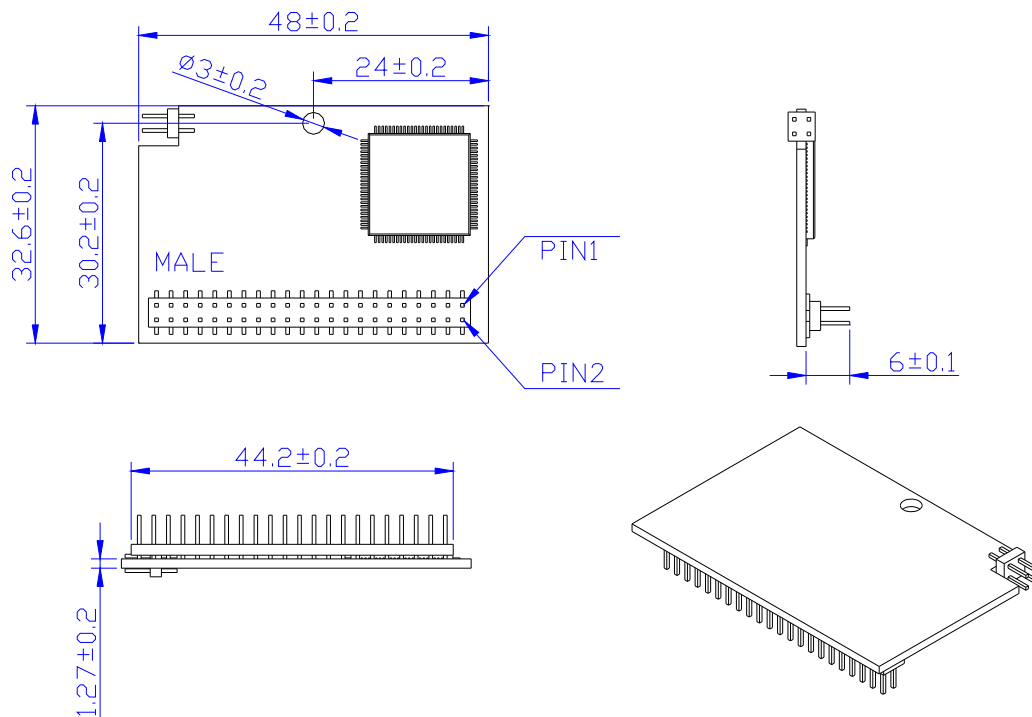
DH0XXXX88XX4 (44 PIN)
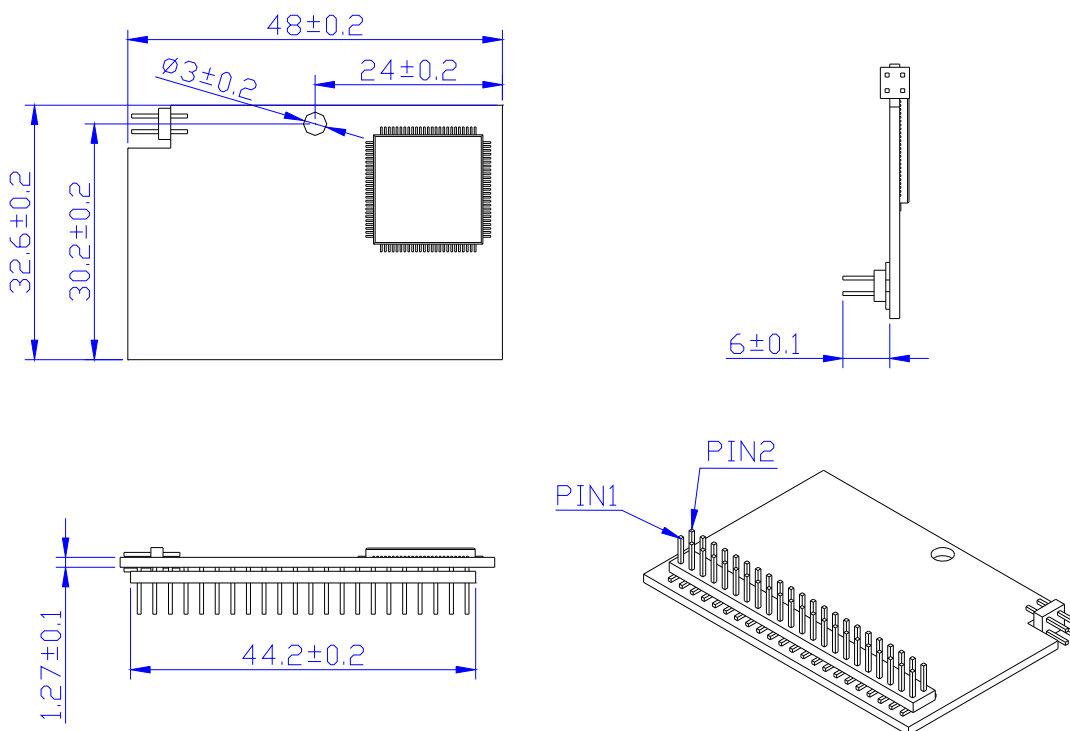
DH0XXXX88XX5 (44 PIN)
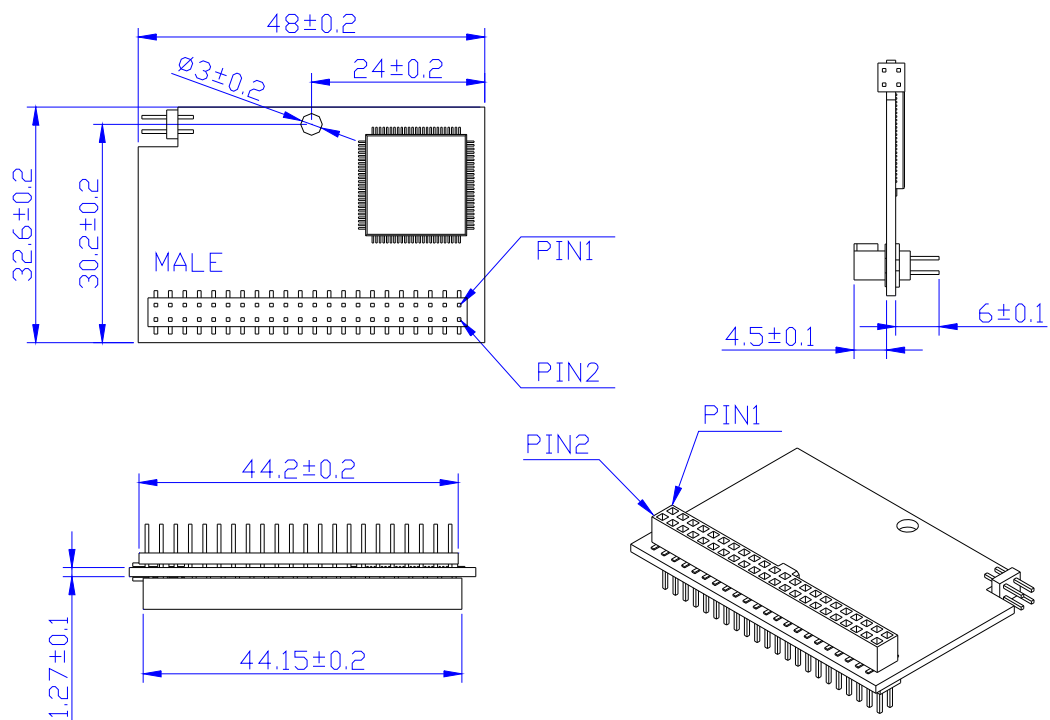
DH0XXXX88XX6 (44 PIN)
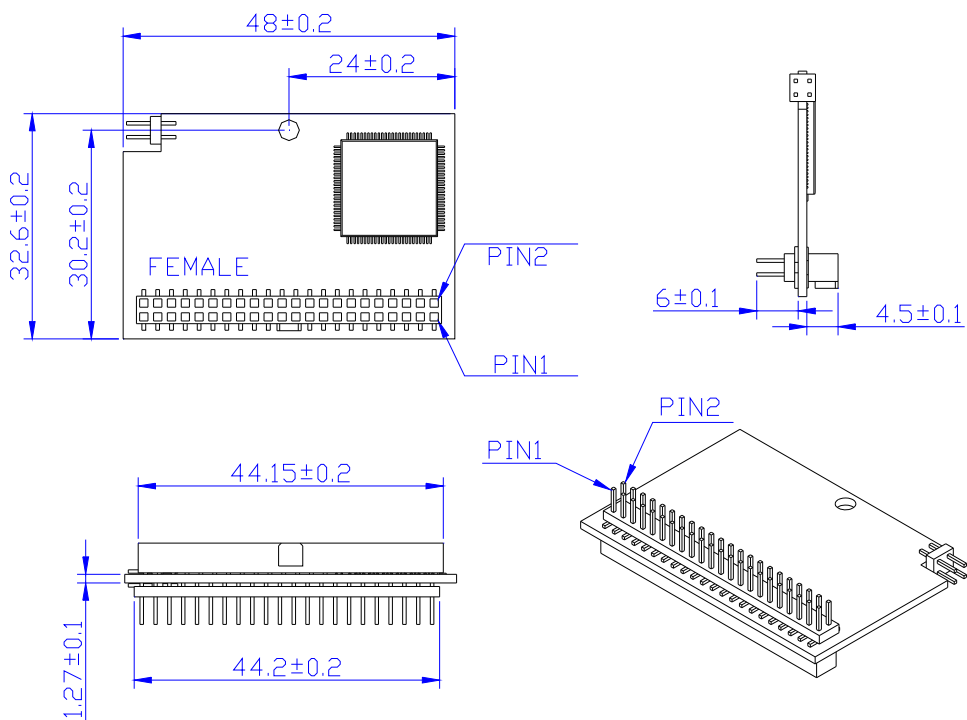
Figure 2: DOM Dimensions

Table 1: DiskOnModule Physical Dimension

Length	44.15 ± 0.2 mm
Width	32.6 ± 0. 2 mm
Thickness	11.77 ± 0.2mm

2.1.3 Weight
- Weight: 15g

2.2 Electronic Specifications

2.2.1 Product Definition
DiskOnModule is designed to operate and work as Data or Code Storage device by NAND Flash Memory and its Controller through IDE (ATA) Standard Interface to Host Systems.
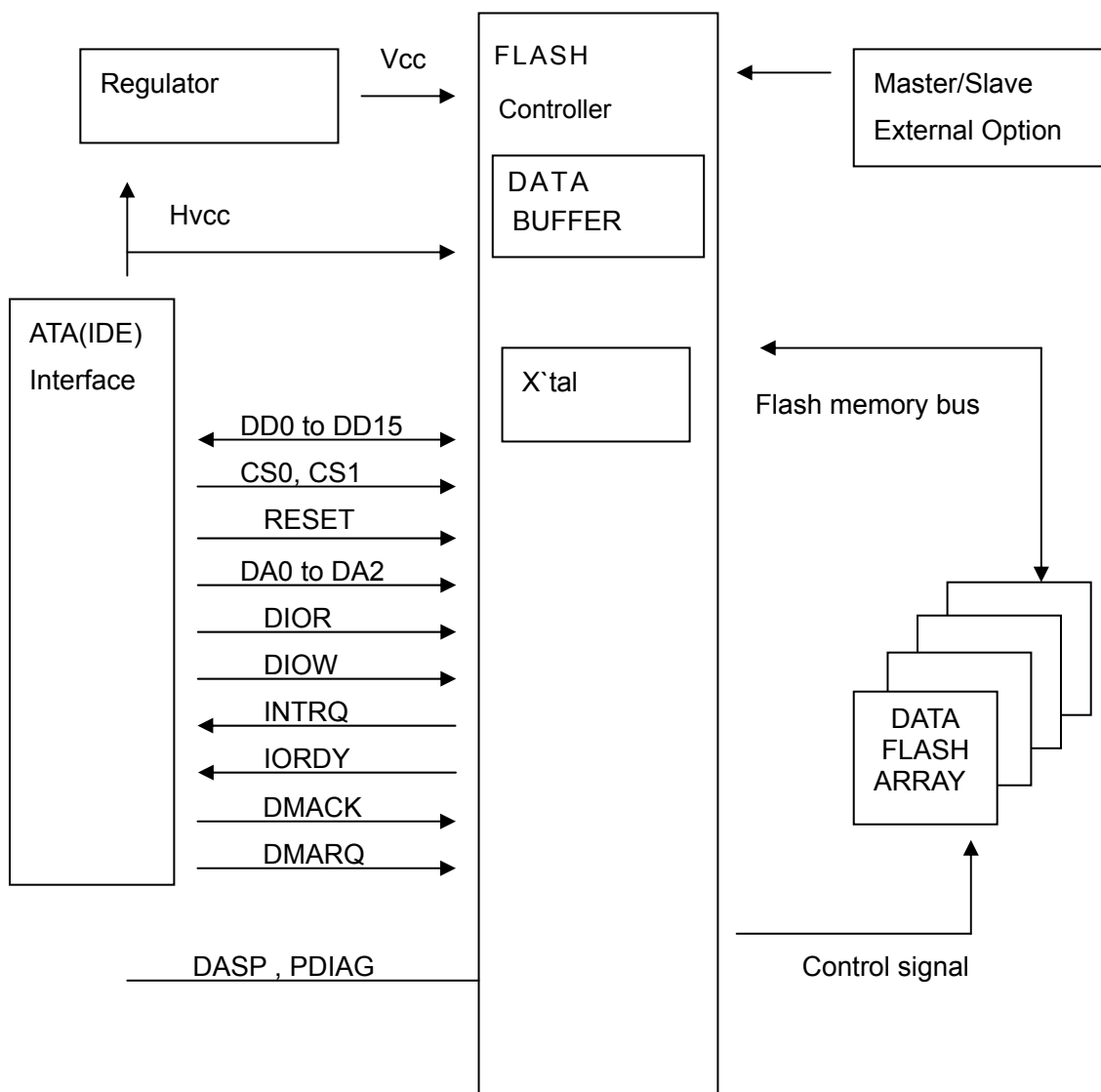
Figure 3: DiskOnModule Block Diagram

2.2.2 Operating Voltage

● Voltage DC +3.3V ± 5% or DC +5.0V ± 10%

2.2.3 Capacity and Block Size information
● Capacity: 32MB ~ 6GB
● Sector Size: 512B

2.2.4 Power Consumption
● DC Information

Voltage	Testing Item	Read Sector Current	Write Sector Current	Stand-By Current
5V	Maximize/Peak Current	34mA	40mA	18.7mA
	Normal Current	33.5mA	39.1mA	8.9mA
	Watts	170mW	200mW	93.5mW
3.3V	Maximize/Peak Current	31mA	36.2mA	16.4mA
	Normal Current	30.2mA	35.7mA	8.1mA
	Watts	102.3mW	119.46mW	54.12mW

※ *Testing Platform;*
- Mother-Board: GA-K8U-939, CPU: K8 2.0G, System Memory: DDR 512MB,
Operating System: DOS 6.22, Test Program: RWALL10 & DOMSV31

2.3 Performance Specifications

2.3.1 Modes
● PIO mode 4
● Ultra DMA 2
● Setting to Ultra DMA 0 or 1 also available as following to Customer's request

2.3.2 Access Time
● DiskOnModule's maximum access time is about 0.25msec.

※ *Testing Platform*
Testing S/W: QBench, Testing OS: DOS, Data: 1sector (512B)
Testing base: Time required Between Host to Device

2.3.3 Seek Time
● DiskOnModule has no seek time by being based on Flash Memory technology.

2.3.4 Mount Time
The Mount Time for initializing and mounting DiskOnModule is different by depending on Operating System and testing Platform.

2.3.5 Data Transfer Time
● Sequential Read: 15 MB/sec
● Sequential Write: 13 MB/sec

※ *Test Platform: GIGA 8I945GME Intel:945+ICH7 3.0GHz DDR:400*
Testing Software: HD Bench 3.4 Testing OS: Windows XP
Notice The value is various bases on the testing platform.

2.3.6 Data Retention
- 10years without requiring power support

2.3.7 Wear-leveling
- Dynamic Wear-Leveling for same level of Write/Erase Cycle

2.3.8 Bad Block Management
- The Bad Blocks of Flash Memory will be replaced into new ones by controller.

2.3.9 Read/Write Cycle
- Read/ Write: 5,000,000 times
          (Estimated on reference to Doc No.SM070001)

2.4 Environmental Specifications

2.4.1 Temperature
- Operating Temperature: 0ºC to +70ºC, Non Operating Temperature: -40ºC to +85ºC (Industrial type)
- Operating Temperature: -40ºC to +85ºC, Non Operating Temperature: -55ºC to +95ºC (Wide Temperature type)

2.4.2 Humidity
- Operating Humidity (30℃ Max. Wet Bulb Temp): 8% to 95%
- Non-Operating Humidity (30℃ Max. Wet Bulb Temp): 8% to 95% (with no condensation relative humidity)

2.4.3 Bare Drop Testing
- Testing Conditions: 75cm height
- Testing Orientation: (Free fell) Front/Rear/Right/Left/Top/Bottom side
- Testing Result: Pass

2.4.4 Vibration
- Random Vibration (Operation) : Testing Specification

Frequency (Hz)	PSD (G2/Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.01	6Grms	30min per axis (X・Y・Z)
100	0.08		
500	0.08		

- Random Vibration (Non-Operating): Testing Specification

Frequency (Hz)	PSD (G2/Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.1	6Grms	30min per axis (X・Y・Z)
100	0.04		
500	0.04		
2000	0.004		

- Frequency Range: 3 ~ 2000Hz
- Testing Result: Pass

2.4.5 Shock and Altitude
     T. B. D.

2.5 Reliability Specifications
2.5.1 ECC/EDC (Error Correction Code/Error Detection Code)
- 1bytes data by 128bytes will be corrected.

2.5.2 Read and Write/Erase Cycle
- Read: No Limitation
- Write/Erase: 5,000,000 times
  (Estimated on reference to Doc No.SM070001)

2.5.3 MTBF (Mean Time Between Failure)
- 2,000,000 hours
  (Estimated on reference to Doc No.SM070002)

2.5.4 Power Cycle
- TBD

2.6 Compliance Specifications
- CE
- FCC

※ Note: Please contact your closest CSS office for other certificate information.

3. Function
3.1 Pin Signal Assignment
- The signals assigned for ATA applications are described in Table 2

Table 2 : ATA connector pin definitions

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin) or Vcc
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5 V (logic) (see note)	41	41	42	42	+5 V (Motor) (see note)
Ground(return) (see note)	43	43	44	44	TYPE- (0=ATA) (see note)

NOTE – Pins which are additional to those of the 44-pin cable.
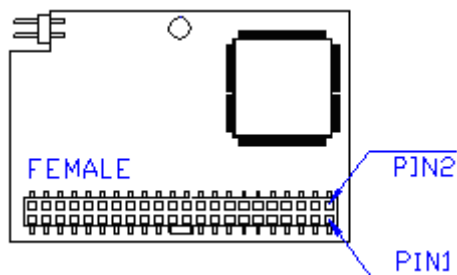
Figure 4: Signal Connector

※ *Notes:*

1. All pins are in a dual row, with a 2.0 mm (0.0785")pitch.

2. The comments on the mating sequence apply to the case of backplane blind mate connector only. In this case, the mating sequences are:

• - the pre-charge power pints and the other ground pins.

• - the signal pins and the rest of the power pins.

3.2 Support ATA Commands
● **ATA Command Set**
- ATA Command Set summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 3: ATA Command Set

Table 3: ATA Command Set Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Device	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA	C8h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Standby	E2h or 96h	-	-	-	-	D	-
1	Standby Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y

1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write DMA	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

Definitions:
  FR = Features Register
  SC = Sector Count Register
  SN = Sector Number Register
  CY = Cylinder Registers
  DH = Card/Drive/Head Register
  LBA = Logical Block Address Mode Supported (see command descriptions for use).
  Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the device
      and head parameters are used
  D - only the device parameter is valid and not the head parameter; C – The register contains command specific data
      (see command descriptions for use).

(1) Check Power Mode - 98h or E5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Check Power Mode

This command checks the power mode.
If the device is in, going to, or recovering from the sleep mode, the device sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.
If the device is in Idle mode, the device sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

(2) Execute Drive Diagnostic - 90h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Execute Drive Diagnostic

This command performs the internal diagnostic tests implemented by the device.

When the diagnostic command is issued in a PCMCIA configuration mode, this command runs only on the device that is addressed by the Drive/Head register. This is because PCMCIA card interface does not allows for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 4: Diagnostic Codes are returned in the Error Register at the end of the command.

Table 4: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

(3) Erase Sector(s) - C0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Erase Sector

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

(4) Format Track - 50h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

Format Track

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the device expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the device. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

(5) Identify Device – ECh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Identify Device

The Identify Device command enables the host to receive parameter information from the device. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 7. All reserved bits or words are zero. Hosts should not depend on Obsolete words in Identify Device containing 0. Table 7 specifies each field in the data returned by the Identify Device Command. In Table 5, X indicates a numeric nibble value specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 5: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the device
	0XXX	2	General configuration – Bit Significant with ATA-3 definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	XXXXh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	XX00h	2	Capabilities
50	0000h	2	Reserved
51	0X00h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	000Xh	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track

57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0X0Xh	2	Multiword DMA transfer. In PCMCIA mode this value shall be 0h
64	00XXh	2	Advanced PIO modes supported
65	XXXXh	2	Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h
66	XXXXh	2	Recommended Multiword DMA transfer cycle time. In PCMCIA mode this value shall be 0h
67	XXXXh	2	Minimum PIO transfer cycle time without flow control
68	XXXXh	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	XXXXh	6	Features/command sets supported
85-87	XXXXh	6	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode Supported and Selected
89	XXXXh	2	Time required for Security erase unit completion
90	XXXXh	2	Time required for Enhanced security erase unit completion
91	XXXXh	2	Current Advanced power management value
92-127	0000h	72	Reserved
128	XXXXh	2	Security status
129-159	0000h	64	Vendor unique bytes
160	XXXXh	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	XXXXh	2	CF Advanced True IDE Timing Mode Capability and Setting
164	XXXXh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability
165-175	0000h	22	Reserved for assignment by the CFA
176-255	0000h	140	Reserved

Word 0: General Configuration

This field indicates the general characteristics of the device.   When Word 0 of the Identify drive information is 848Ah then the device is a device and complies with the CFA specification and CFA command set. It is recommended that PCMCIA modes of operation report only the 848Ah value as they are always intended as removable devices.
Bits 15-0: CF Standard Configuration Value
Word 0 is 848Ah.   This is the recommended value of Word 0.

Some operating systems require Bit 6 of Word 0 to be set to 1 (Non-removable device) to use the card as the root storage device. The Card must be the root storage device when a host completely replaces conventional disk storage with a device in True IDE mode. To support this requirement and provide capability for any future removable media Cards, alternate handling of Word 0 is permitted.
Bits 15-0: CF Preferred Alternate Configuration Values 044Ah: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while preserving all Retired bits in the word.   0040h: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while zeroing all Retired bits in the word

Bit 15-12: Configuration Flag If bits 15:12 are set to 8h then Word 0 shall be 848Ah. If bits 15:12 are set to 0h then Bits 11:0 are set using the definitions below and the Card is required to support for the CFA command set and report that in bit 2 of Word 83. Bit 15:12 values other than 8h and 0h are prohibited.

> Bits 11-8: Retired. These bits have retired ATA bit definitions. It is recommended that the value of these bits be either the preferred value of 0h or the value of 4h that preserves the corresponding bits from the 848Ah CF signature value.
>
> Bit 7: Removable Media Device If Bit 7 is set to 1, the Card contains media that can be removed during Card operation. If Bit 7 is set to 0, the Card contains nonremovable media.
>
> Bit 6: Not Removable Controller and/or Device
>
> *Alert! This bit will be considered for obsolescence in a future revision of this standard.*
>
> If Bit 6 is set to 1, the Card is intended to be nonremovable during operation. If Bit 6 is set
>
> to 0, the Card is intended to be removable during operation.
>
> Bits 5-0: Retired/Reserved
>
> *Alert! Bit 2 will be considered for definition in a future revision of this standard and shall be 0 at this time.*
>
> Bits 5-1 have retired ATA bit definitions.
>
> Bit 2 shall be 0.
>
> Bit 0 is reserved and shall be 0.
>
> It is recommended that the value of bits 5-0 be either the preferred value of 00h or the value of
>
> 0Ah that preserves the corresponding bits from the 848Ah CF signature value.

Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Words 7-8: Number of Sectors per Card

This field contains the number of sectors per device. This double word value is also the first invalid address in LBA translation mode.

Words 10-19: Serial Number

This field contains the serial number for this device and is right justified and padded with spaces (20h).

Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h.

Words 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

Words 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

Word 47: Read/Write Multiple Sector Count

Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the device supports for Read/Write Multiple commands.

Word 49: Capabilities
Bit 13: Standby Timer
If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command
If bit 13 is set to 0 then the Standby timer operation is defined by the vendor.
Bit 11: IORDY Supported
If bit 11 is set to 1 then this device supports IORDY operation.
If bit 11 is set to 0 then this device may support IORDY operation.
Bit 10: IORDY may be disabled
Bit 10 shall be set to 0, indicating that IORDY may not be disabled.

Bit 9: LBA supported
Bit 9 shall be set to 1, indicating that this device supports LBA mode addressing.   Devices shall support LBA addressing.
Bit 8: DMA Supported
If bit 8 is set to 1 then Read DMA and Write DMA commands are supported.
Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF cards.

Word 51: PIO Data Transfer Cycle Timing Mode
The PIO transfer timing for each device falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

Word 53: Translation Parameters Valid
Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any device that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

Words 54-56: Current Number of Cylinders, Heads, Sectors/Track
These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Words 57-58: Current Capacity
This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting
Bits 15-9 are reserved and shall be set to 0.
Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid.
Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

Words 60-61: Total Sectors Addressable in LBA Mode
This field contains the total number of user addressable sectors for the device in LBA mode only.

Word 63: Multiword DMA transfer
Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the device to indicate the multiword DMA mode which is currently selected.
Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected. Selection of Multiword DMA modes 3 and above are specific to device are reported in word 163 as described in section 6.33: Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.
Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the Multiword DMA modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the device supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the device supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the device supports Multiword DMA modes 2, 1 and 0.

Support for Multiword DMA modes 3 and above are specific to device are reported in word 163 as described in section 6.33: Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

Word 64: Advanced PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the advanced PIO modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the device supports PIO mode 3. Bit 1, if set to one, indicates that the device supports PIO mode 4.

Support for PIO modes 5 and above are specific to device are reported in word 163 as described in section 6.33: Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

Word 65: Minimum Multiword DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer.

If this field is supported, bit 1 of word 53 shall be set to one.   The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device.   This field shall be supported by all device supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

Word 66: Recommended Multiword DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the device will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one.   The value in word 66 shall not be less than the value in word 65.   This field shall be supported by all device supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by device prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid.   The values

in these words should not be depended on by host implementers.

Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.

If bit 1 of word 82 is set to one, the Security Mode feature set is supported.

Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.

If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported.

Bit 7 of word 82 shall be set to zero; release interrupt is not supported.

Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.

Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 82 is obsolete.

Bit 12 of word 82 shall be set to one; the device supports the Write Buffer command.
Bit 13 of word 82 shall be set to one; the device supports the Read Buffer command.

Bit 14 of word 82 shall be set to one; the device supports the NOP command.

Bit 15 of word 82 is obsolete.

Bit 0 of word 83 shall be set to zero; the device does not support the Download Microcode command.

Bit 1 of word 83 shall be set to zero; the device does not support the Read DMA Queued and Write DMA Queued commands.

Bit 2 of word 83 shall be set to one; the device supports the CFA feature set.

If bit 3 of word 83 is set to one, the device supports the Advanced Power Management feature set.

Bit 4 of word 83 shall be set to zero; the device does not support the Removable Media Status feature set.

Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by device prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.
Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.
If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command.
Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
If bit 5 of word 85 is set to one, write cache is enabled.
If bit 6 of word 85 is set to one, look-ahead is enabled.
Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.

Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
Bit 11 of word 85 is obsolete.
Bit 12 of word 85 shall be set to one; the device supports the Write Buffer command.
Bit 13 of word 85 shall be set to one; the device supports the Read Buffer command.
Bit 14 of word 85 shall be set to one; the device supports the NOP command.
Bit 15 of word 85 is obsolete.
Bit 0 of word 86 shall be set to zero; the device does not support the

Download Microcode command.
Bit 1 of word 86 shall be set to zero; the device does not support the Read DMA Queued and Write DMA Queued commands.
If bit 2 of word 86 shall be set to one, the device supports the CFA feature set.
If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
Bit 4 of word 86 shall be set to zero; the device does not support the Removable Media Status feature set.

Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected.   Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected.   If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported.
Bits 15-13: Reserved
Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
Bits 7-5: Reserved
Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.
Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.
Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.
Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
Bit 0: 1 = Ultra DMA mode 0 is supported

Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete.   This command shall be supported on devices that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete. This command shall be supported on devices that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 91: Advanced power management level value

Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

Word 128: Security Status

Bit 8: Security Level If set to 1, indicates that security mode is enabled and the security level is maximum. If set to 0 and security mode is enabled, indicates that the security level is high.

Bit 5: Enhanced security erase unit feature supported If set to 1, indicates that the Enhanced security erase unit feature set is supported.

Bit 4: Expire If set to 1, indicates that the security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset.

Bit 3: Freeze

If set to 1, indicates that the security is Frozen.

Bit 2: Lock

If set to 1, indicates that the security is locked.

Bit 1: Enable/Disable

If set to 1, indicates that the security is enabled.

If set to 0, indicates that the security is disabled.

Bit 0: Capability If set to 1, indicates that device supports security mode feature set. If set to 0, indicates that device does not support security mode feature set.

Word 160: Power Requirement Description

This word is required for devices that support power mode 1.

Bit 15: VLD If set to 1, indicates that this word contains a valid power requirement description. If set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV

This bit is reserved and shall be 0.

Bit 13: -XP If set to 1, indicates that the device does not have Power Level 1 commands. If set to 0, indicates that the device has Power Level 1 commands

Bit 12: -XE

If set to 1, indicates that Power Level 1 commands are disabled.

If set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current

This field contains the device's maximum current in mA.

Word 162: Key Management Schemes Supported

Bit 0: CPRM support If set to 1, the device supports CPRM Scheme (Content Protection for Recordable Media) If set to 0, the device does not support CPRM.

Bits 1-15 are reserved for future additional Key Management schemes.

Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings

This word describes the capabilities and current settings for CFA defined advanced timing modes using the True IDE interface.

Notice!   The use of True IDE PIO Modes 5 and above or of Multiword DMA Modes 3 and above impose significant restrictions on the implementation of the host as indicated in section 4.3.7: Additional Requirements for CF Advanced Timing Modes.

There are four separate fields defined that describe support and selection of Advanced PIO timing modes and Advanced Multiword DMA timing modes.   The older modes are reported in words 63 and 64 as described in sections 6.2.1.6.18: Word 63: Multiword DMA transfer and 6.2.1.6.19: Word 64: Advanced PIO transfer modes supported.

Bits 2-0: Advanced True IDE PIO Mode Support Indicates the maximum True IDE PIO mode supported by the card.

Value	Maximum PIO mode timing supported
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 5-3: Advanced True IDE Multiword DMA Mode Support Indicates the maximum True IDE Multiword DMA mode supported by the card.

Value	Maximum Multiword DMA timing mode supported
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 8-6: Advanced True IDE PIO Mode Selected Indicates the current True IDE PIO mode selected on the card.

Value	Current PIO timing mode selected
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 11-9: Advanced True IDE Multiword DMA Mode Selected Indicates the current True IDE Multiword DMA Mode Selected on the card.

Value	Current Multiword DMA timing mode selected
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 15-12 are reserved.

Word 164: CF Advanced PCMCIA I/O and Memory Timing Modes Capabilities and Settings
> This word describes the capabilities and current settings for CFA defined advanced timing modes using the Memory and PCMCIA I/O interface.
> **Notice! The use of PCMCIA I/O or Memory modes that are 100ns or faster impose significant restrictions on the implementation of the host as indicated in section 4.3.7: Additional Requirements for CF Advanced Timing Modes.**
> Bits 2-0: Maximum Advanced PCMCIA I/O Mode Support Indicates the maximum I/O timing mode supported by the card.

Value	Maximum PCMCIA IO timing mode supported
0	255 ns Cycle PCMCIA I/O Mode
1	120 ns Cycle PCMCIA I/O Mode
2	100 ns Cycle PCMCIA I/O Mode
3	80 ns Cycle PCMCIA I/O Mode
4-7	Reserved

Bits 5-3: Maximum Memory timing mode supported Indicates the Maximum Memory timing mode supported by the card.

Value	Maximum Memory timing mode Supported
0	250 ns Cycle Memory Mode
1	120 ns Cycle Memory Mode
2	100 ns Cycle Memory Mode
3	80 ns Cycle Memory Mode
4-7	Reserved

Bits 15-6: Reserved

(6) Idle - 97h or E3h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

Idle

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

(7) Idle Immediate - 95h or E1h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95h or E1h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Idle Immediate

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

(8) Initialize Drive Parameters - 91h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

Initialize Drive Parameters

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

(9) Read Buffer - E4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Read Buffer

The Read Buffer command enables the host to read the current contents of the device's sector buffer. This command has the same protocol as the Read Sector(s) command.

(10) Read DMA – C8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read DMA

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the device sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.
When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

(11) Read Long Sector - 22h or 23h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22h or 23h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Read Long Sector

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the device does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

(12) Read Multiple - C4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read Multiple

Note: This specification requires that devices support a multiple block count of 1 and permits larger values to be supported.

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command. Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where
n = (sector count) modulo (block count).
If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any. Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

(13) Read Sector(s) - 20h or 21h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read Sector(s)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the device sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

(14) Read Verify Sector(s) - 40h or 41h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read Verify Sector(s)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the device sets BSY.

When the requested sectors have been verified, the device clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

(15) Recalibrate - 1Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Recalibrate

This command is effectively a NOP command to the device and is provided for compatibility purposes.

(16) Request Sense - 03h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03h							
			X	Drive	x			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Request Sense

This command requests extended error information for the previous command. Table 6 defines the valid extended error codes for the device Series product. The extended error code is returned to the host in the Error Register.

Table 6: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

(17) Seek - 7Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Seek

This command is effectively a NOP command to the device although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

(18) Set Features – EFh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

Set Features

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the Compact Flash Storage Card shall return command aborted. Table 7: Feature Supported defines all features that are supported.

Table 7: Feature Supported

Feature	Operation
01h	Enable 8 bit data transfers.
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Count register.
05h	Enable Advanced Power Management.
09h	Enable Extended Power operations. *(Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)*
0Ah	Enable Power Level 1 commands.
44h	Product specific ECC bytes apply on Read/Write Long commands.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Disable Extended Power operations*. (Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)*
8Ah	Disable Power Level 1 commands.
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.

AAh	Enable Read Look Ahead.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses.   The host shall not enable this feature for DMA transfers.

Features 02h and 82h allow the host to enable or disable write cache in devices that implement write cache. When the subcommand disable write cache is issued, the device shall initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one Multiword DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Table 8: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

If a device supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of "00000000b", it shall set its default PIO mode. If the value is "00000001b" and the device supports disabling of IORDY, then the device shall set its default PIO mode and disable IORDY. A device shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

A device reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported.

A device reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.

If an Ultra DMA mode is enabled any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device. Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Table9: Advanced power management levels show these values.

Table 9: Advanced power management levels

Level	Sector Count Value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.

Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the device with extended power.

Features 55h and BBh are the default features for the device; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register were set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

(19) Set Multiple Mode - C6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Set Multiple Mode

This command enables the device to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the device sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands.

If the block count is not supported, an Aborted Command error is posted and the Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

(20) Set Sleep Mode- 99h or E6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Set Sleep Mode

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

(21) Standby - 96h or E2h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96h or E2h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Standby

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

(22) Standby Immediate - 94h or E0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94h or E0h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Standby Immediate

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

(23) Translate Sector - 87h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Translate Sector

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 10 represents the information in the buffer. Please note that this command is unique to the device.

Table 10: Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) 1
1Bh-1FFh	Reserved

Notes 1) A value of 0 indicates Hot Count is not supported.

(24) Wear Level - F5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

Wear Level

For the device that do not support security mode feature set, this command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register shall always be returned with a 00h indicating Wear Level is not needed. If the device supports security mode feature set, this command shall be handled as Security Freeze Lock.

(25) Write Buffer - E8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Write Buffer

The Write Buffer command enables the host to overwrite contents of the device's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

(26) Write DMA – CAh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write DMA

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the device sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

(27) Write Long Sector - 32h or 33h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Write Long Sector

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state device, the four bytes of ECC transferred by the host may be used by the device. The device may discard these four bytes and write the sector with valid ECC data. This comm device and has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

(28) Write Multiple Command - C5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Multiple Command

Note: This specification requires that devices support a multiple block count of 1 and permits larger values to be supported.

This command is similar to the Write Sectors command. The device sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$n = $ (sector count) modulo (block count).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation shall be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector numbers of the sector where the error occurred. The Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

(29) Write Multiple without Erase – CDh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Multiple without Erase

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

(30) Write Sector(s) - 30h or 31h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the device sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

(31) Write Sector(s) without Erase - 38h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s) without Erase

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

(32) Write Verify - 3Ch

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Verify

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

3.3 Firmware Upgrade
● The Firmware of DiskOnModule can not be upgraded by customers, so please contact your nearest CSS Office.

4. Installation
4.1 Installation
● For Installation of DiskOnModule to your system, please follow up below steps;
1. Make sure your computer is turned off before you open the case.
2. Plug the DiskOnModule carefully into the IDE slot on your computer or host adapter.
3. Connect the power cable of the DiskOnModule.
4. Check cable connections and DiskOnModuel is firm enough.

4.2 Partition
● For DOS Operating System：
- To partition your new DiskOnModule for example use Microsoft DOS program:
1. Insert a bootable DOS diskette into your diskette drive and restart your computer.
2. Insert a DOS program diskette that contains the **FDISK.EXE** and **FORMAT.COM** programs into your diskette drive. Use the same DOS version that is on your bootable diskette. At the A: prompt, type **FDISK** and press **ENTER**.
3. Select "Create DOS partition or logical DOS drive" by pressing **1**. Then press **ENTER**.
4. Select "**Create primary DOS partition**" by pressing 1 again. Then press ENTER. Create your first drive partition. If you are creating a partition that will be used to boot your computer (drive C), make sure that the partition is marked active.
5. Create an extended partition and additional logical drives as necessary, until all the space on your new hard drive has been partitioned.
6. When the partitioning is complete, **FDISK** reboots your computer.
   ※ *Note: Make sure to use the correct drive letters so that you do not format a drive that already contains data.*
7. At the A: prompt, type **format c:/s**, where c is the letter of your first new partition, Repeat the format process for all the new partitions you have created.
8. After you format your DiskOnModle, it is ready to use.

● **For Windows Operating System：**

- To partition your new DiskOnModule, for example use Microsoft WindowsXP and WindowsXP embedded system：

1. Into your windows system. You can Click the 『Start』→『Control Panel』→『Administrative Tools』→『Computer Management』 then select 『Storage』→『Disk Manager』 to setup the partition.
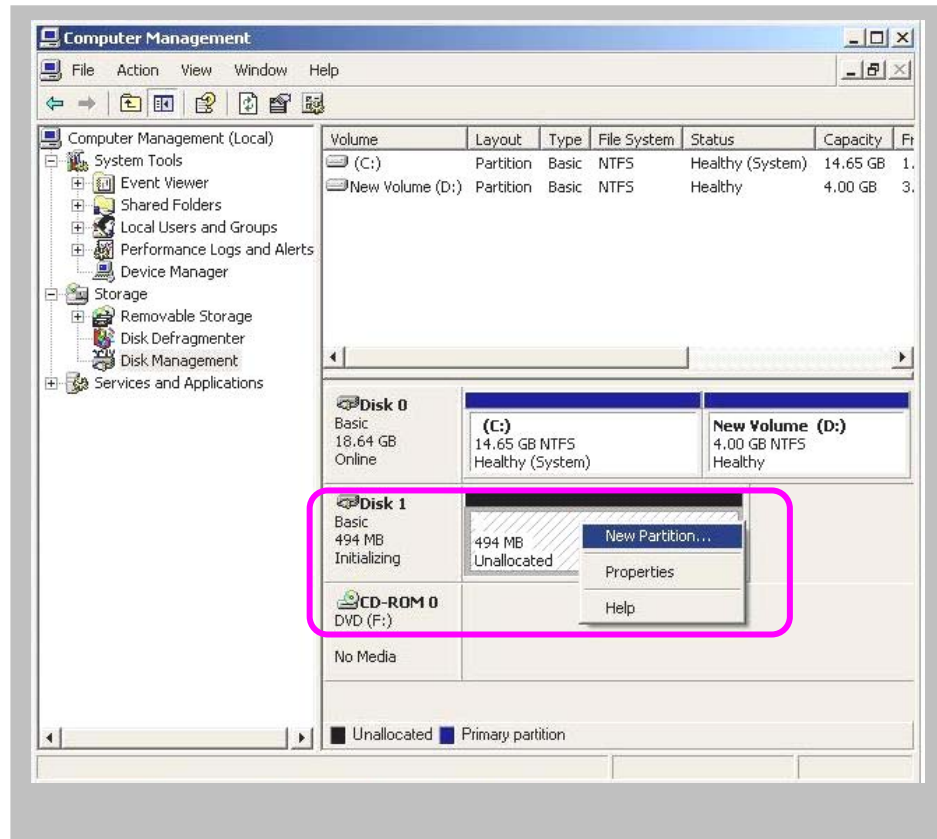
4.3 Format
- **For DOS Operating System：**
  - Before you format or partition your new DiskOnModule, you must configure your computer's BIOS so that the computer can recognize your new DiskOnModule.
    1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE, ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.
    2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (If you use Normal/CHS mode to partition your DOM, you can get the maximum formatted capacity.)
       This allows your computer to configure itself automatically for your new DiskOnModule.
       If your BIOS does not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.

       BIOS Settings (see specification)
Capacity	Cylinders	Heads	Sectors	(unformatted)

    3. Save the settings and exit the System Setup program.
       (Your computer will be automatically rebooted.)

- **For Windows Operating System：**

  - To partition your new DOM, for example use Microsoft WindowsXP and WindowsXP embedded system：

    1. Click the 『Start』→『Control Panel』→『Administrative Tools』→『Computer Management』then select 『Storage』→『Disk Manager』 to setup the file format.
    2. Select "FAT or NTFS" format for user.
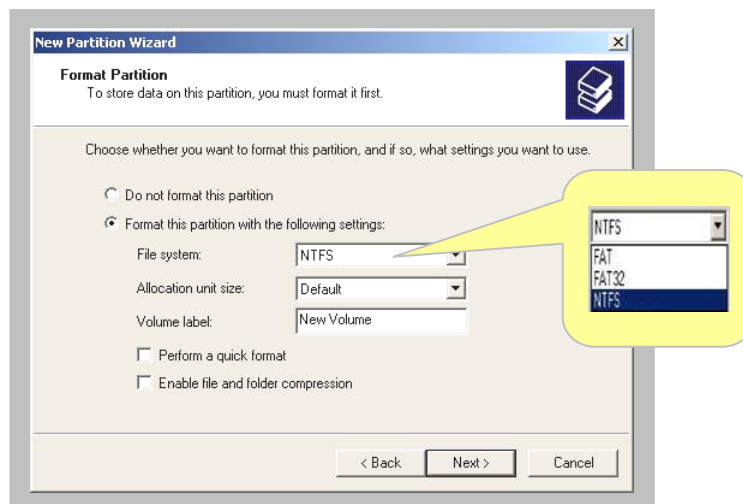
5. Troubleshooting

5.1 BIOS can not identify DiskOnModule
  5.1.1 Check Power Cable Status
  5.1.2 Check Connector status
  5.1.3 Check the Power Voltage (5V or 3.3V)

5.2 DOM can not boot the system
  5.2.1 Check BIOS setting
  Notice   Reinstall your system
      Please contact your closest CSS office for verifying your other troubles.

6. Ordering Information

Table 11: DiskOnModule Ordering Information

P/N	Capacity (Max)
DH0**032M***₁88R*₂**D***₃1*₄	6GB

  *1：032M:32MB, 064M:64MB, 128M:128MB, 256M:256MB, 512M:512MB, 010G:1GB, 020G:2GB, 040G:4GB, 060G:6GB

  *2：R: Industrial type   T: Wide Temperature type

  *3：Flash Density
      D:32MB, E:64MB, F:128MB, I:256MB, L:512MB, N:1GB, P:2GB

  *4：Connector Direction: 1:LFD, 2:LDF, 3:LMD, 4:LDM, 5:LMF, 6:LFM

  *5：DE0**032M**88R**D**1(WP): With Write Protect Switch
      DE0**032M**88R**D**1   : Without Write Protect Switch

7. Contact Information

CoreSolid Storage Corporation, a TDK-PQI storage business company, specializes in the design and marketing of SSD, DOM, and Industry CF products.

For further information, please reach us at the following contact information:

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