Acknowledgments

MS-DOS, Windows®, Microsoft® Visual C++ and Visual BASIC are trademarks of Microsoft®Corporation. Intel® and Pentium® are trademarks of Intel Corporation. Delphi and C++ Builder are trademarks of Borland Software Corporation.

CE notification

The MIC-3756, developed by ADVANTECH CO., LTD., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

On-line Technical Support

For technical support and service, please visit our support website at:

http://www.advantech.com/support

Part No.2003375600 1st Edition

Printed in Taiwan October 2003

(This page is left blank for hard printing.)

Contents

Tables

Figures

CHAPTER 1

Introduction

(This page is left blank for hard printing.)

1. Introduction

This chapter gives background information on the MIC-3756. It then shows you how to configure the card to match your application and prepare it for installation into your system.

The MIC-3756 is a 64-channel Isolated Digital I/O CompactPCI™ DAS Card, which complies with PICMG 2.0 R2.1 CompactPCI specifications. The MIC-3756 features a unique circuit design and complete functions for data acquisition and control. It is a powerful data acquisition (DAS) card for the CompactPCI bus.

1.1 Features

- CPCI bus specification 2.1 compliant
- CPCI 3U size card
- 32 isolated digital input channels
- 32 isolated digital output channels
- High-voltage isolation for input/output channels (2,500 VDC)
- Wide input range (10 ~ 50 VDC)
- Wide output range (5 ~ 40 VDC)
- High-sink current on isolated output channels (200 mA max./ channel)
- High over-voltage protection (70 VDC) for input channels
- Board ID
- Output status read-back for output channels
- Digital output value retained after hot system reset

- Channel-Freeze function for output channels
- One independent 16-bit UP Counter
- 2 Counter Clock Source selectable
- 1MHz input counter frequency on broad
- I/O address automatically assigned by PCI plug-and-play
- OS supported: Windows® NT, Windows® 95/98, Windows® 2000, Windows® XP
- Interrupt status register for increased performance

The Advantech MIC-3756 DAS card offers the following main features:

Robust Isolation

The MIC-3756 features a robust isolation protection for applications in industrial, lab and machinery automation. The MIC-3756 can durably withstand voltages up to 2,500 VDC, preventing your host system from any incidental harms. Even with an input voltage rising up to 70 VDC, the input channels of MIC-3756 can still manage to work properly albeit only for a short period of time.

Wide Input/Output Range

The MIC-3756 has a wide range of input voltage from 10 to 50 VDC, which is suitable for most industrial applications with 12 VDC, 24 VDC and 48 VDC input voltage. The MIC-3756 also features a wide output voltage ranging from 5 to 40 VDC, suitable for most industrial applications with 12 VDC / 24 VDC output voltage. In the mean time,

we are also ready to serve your special needs for specific input/output voltage range. Do not hesitate to ask us about tailoring our standard products to meet your specifications. All these merits make MIC-3756 the best choice for industrial applications.

Board ID Setting

The MIC-3756 has a built-in DIP switch that helps define each card's ID when multiple cards have been installed on the same CompactPCI system. The board ID setting function is very useful when users build their system with multiple MIC-3756 cards. With the correct Board ID settings, you can easily identify and access each card during hardware configuration and software programming.

Channel-Freeze Function

The MIC-3756 provides ***Channel-Freeze*** function, which can be enabled either in dry contact or wet contact mode (selectable by the on-board jumper JP2). When the ***Channel-Freeze*** function is enabled, the last status of each digital output channel will be safely kept for emergency use. Moreover, you can enable this function through software as it is useful in software simulation and testing program.

Reset Protection

When the system has undergone a hot reset (i.e. without turning off the system power), the MIC-3756 can either retain output values of each channel, or return to its default configuration as open status, depending on its on-board jumper (JP3) setting. This function

protects the system from faulty operations when the system resets unexpectedly.

1.2 Specifications

- **Bus Interface:** CPCI bus specification 2.1 compliant
- **Bus Controller:** PLX9030
- **Dimensions:** 160 mm (L) x 100 mm (W)
- **Operating temperature:** 0 ~ 60℃ (referring to IEC68-2-1, 2)
- **Operating Humidity:** 5 ~ 95% Relative Humidity, non-condensing (referring to IEC 68-2-1, 2)
- **Storage Temperature:** -20 ~ 80 ℃ (See the **Appendix A** for more details.)
- **Hot-Swap**

CHAPTER 2

Hardware Configuration

(This page is left blank for hard printing.)

2. Hardware Configuration

This chapter gives users a package item checklist, proper instructions about unpacking and step-by-step procedures for card installation.

2.1 Initial Inspection

You should find the following items inside the shipping package of MIC-3756 (in addition to this manual):

- CompactPCI card MIC-3756
- Advantech Automation Software CD-ROM
- MIC-3756 user's manual

Prior shipment, we have carefully inspected the CompactPCI card series. It should be free of marks and scratches and in perfect working order on receipt. As you unpack the CompactPCI card series, check it for signs of shipping damages (damaged box, scratches, dents, etc.) If it is damaged or fails to meet specifications, notify our service department or your local sales representative immediately, and your carrier. Retain the shipping carton and packing materials for inspection by the carrier. Upon inspection, we will make all necessary arrangements to repair or replace the unit.

When you handle the CompactPCI card series, remove it from its protective packaging by grasping the front metal panel. Keep the anti-vibration packing. Whenever you remove the card from the CompactPCI system, store it in this package for protection.

Note:

Discharge your body' s static electric charge by touching the back of the grounded chassis of the system unit (metal) before handling the board. You should avoid contact with materials that hold a static charge such as plastic, vinyl and Styrofoam. Handle the board only by its edges to avoid static damage to its integrated circuits. Avoid touching the exposed circuit connectors. We also recommend that you use a grounded wrist strap and place the card on a static dissipative mat whenever you work with it.

2.2 Hardware Installation

Note:

Make sure you first install the driver before installing the card. We strongly recommend that you install the software driver before installing the hardware into your system, since this will guarantee a smooth and trouble-free installation process.

For more information about the driver installation, configuration and removal procedures for Windows 9X, Windows NT, Windows 2K and Windows XP, please see the *Device Driver Manual*.

When installing the MIC-3756 Card, Please make sure the DLL driver of MIC-3756 installation is completed, you can now go on to install the MIC-3756 card in your CompactPCI system. If you have any doubt, please consult the user's manual or related documentation. Please follow the following steps to install the card on your system.

To install a card:

Step 1: Remove one cover on the unused slot of your CompactPCI computer slot.

Step 2: Hold the Card Vertically. Be sure that the card is pointing in the correct direction. The components of the card should be pointing to the right-hand side and the black handle of the card should be pointing to the lower edge of the backplane.

Step 3: Hold the lower handle and pull the handle down to unlock it.

Step 4: Insert the MIC-3756 card into the CompactPCI chassis carefully by sliding the lower edges of the card into the card

guides.

Step 5: Push the card into the slot gently by sliding the card along the card guide until J1 meets the long needle on the backplane, then the **Blue LED** on the front panel of the card will lit.

Note:

If your card is correctly positioned and has slid all the way into the chassis, the handle should match the rectangular holes. If not, remove the card from the card guide and repeat step 3 again. Do not try to install a card by forcing it into the chassis.

Step 6: Now push the card into the right place, and the **Blue LED** will turn off.

Step 7: After the **Blue LED** is off**,** push the handle to secure the card and lock it into place.

Step 8: Because the CompactPCI system can "Hot-Swap", if your CompactPCI computer power is on the system can configure the card automatically. Once the system finished configuration, you can find the card information in the **Device Manager**.

Note:

If your card is properly installed, you should see the device name of your card listed on the Device Manager tab.

To remove a card:

Step 1: Push the handle down to unlock the card, and the CompactPCI

system will automatically uninstall the card configuration.

Step 2: Once the system completes the configuration, the **Blue LED** will lit. Now you can slide the card out**.**

2.3 Board Layout

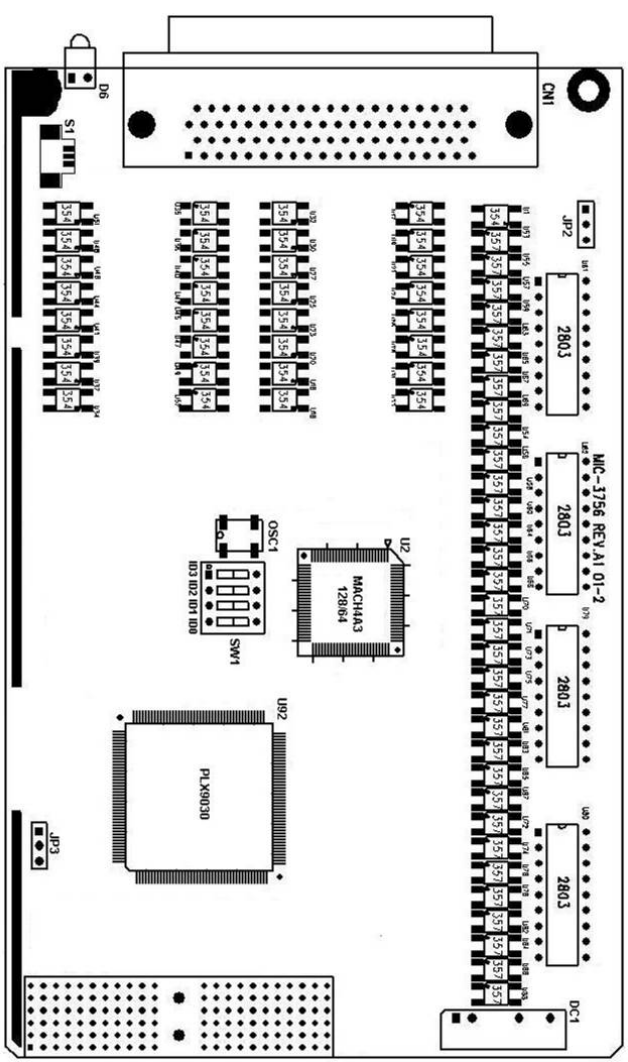


Fig. 2-1 MIC-3756 board layout

Connector

MIC-3756 has one 78-pin DB female connector. For more details about jumper, switch and connector, please see ***Chapter 4 Pin Assignment & Jumper Setting*** and ***Chapter 5 Operation***.

(This page is left blank for hard printing.)

CHAPTER 3

Pin Assignment and Jumper Setting

(This page is left blank for hard printing.)

3. Pin Assignment and Jumper Setting

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid unnecessary and costly damage to your system and other hardware devices. This chapter provides useful information about how to connect input and output signals to the MIC-3756 via the I/O connector.

3.1 Pin Assignment

The I/O connector on the MIC-3756 is a 78-pin DB female connector. *Fig. 3-1* shows the pin assignments for the 78-pin DB connector on the MIC-3756, and *Table 3-1* shows its connector signal description.

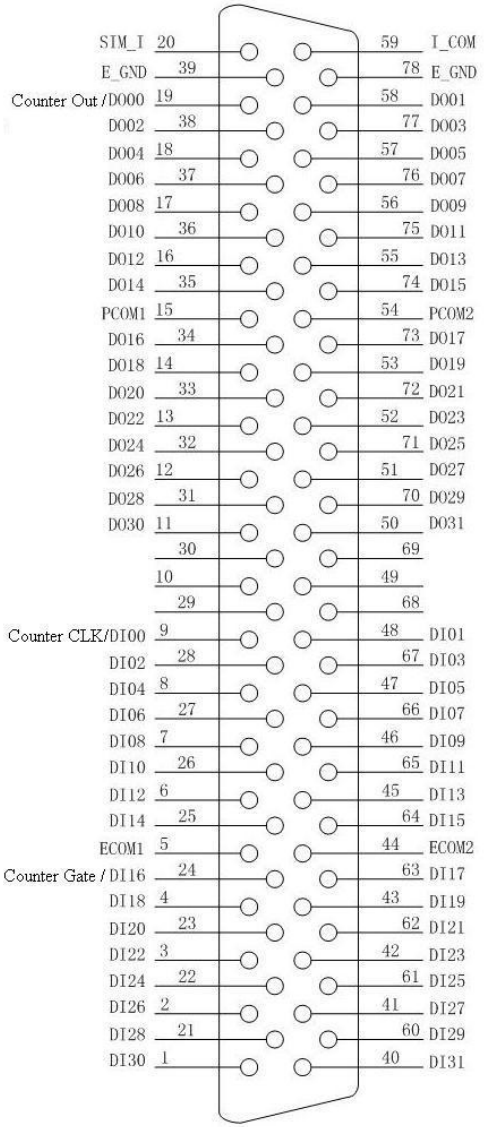


Fig. 3-1 I/O Connector pin assignments for the MIC-3756

Table 3-1 MIC-3756 I/O Connector Signal Description

Signal Name	Reference	Direction	Description
Counter CLK / DI00	- / ECOM1 (DI00)	Input	Counter Clock Source input & Isolated digital input DI00 of group0
DI<01...15>	ECOM1	Input	Isolated digital input of group 0
Counter Gate / DI16	- / ECOM2 (DI16)	Input	Counter Gate Control Pin & Isolated digital input DI16 of group1
DI<17...31>	ECOM2	Input	Isolated digital input of group 1
Counter Output / DO00	- / PCOM1	Output	Counter Output& Isolated digital output D000 of group0
DO<01...15>	PCOM1	Output	Isolated digital output of group 0
DO<16...31>	PCOM2	Output	Isolated digital output of group 1
ECOM1	-	Input	External common input of group 0
ECOM2	-	Input	External common input of group 1
PCOM1	-	Output	External common output of group 0
PCOM2	-	Output	External common output of group 1
E_GND	-	-	Isolated ground
CH_FRZ_IN	CH_FRZ_COM	Input	Channel-Freeze function input pin
CH_FRZ_COM	-	Input	Common pin for Cannel-Freeze function input

3.2 Location of Jumpers and DIP switch

Fig. 3-2 shows the names and locations of jumpers and DIP switch on the MIC-3756. There are two jumpers JP2, JP3 and one DIP switch SW1 on the MIC-3756. Please refer to ***Section 4.3 Isolated Digital Output Connection***, ***Section 5.2 Board ID*** and ***Section 5.3 Channel-Freeze Function*** for more information about JP2, JP3 and SW1 configurations.

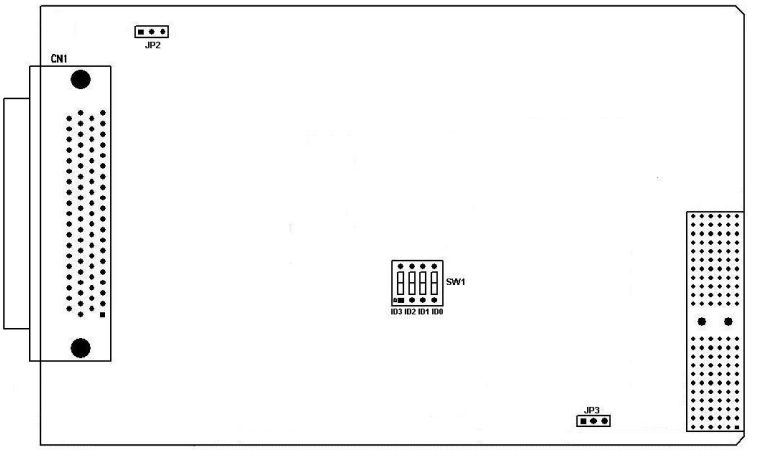


Fig. 3-2 Location of Jumpers and DIP switch on MIC-3756

3.3 Isolated Digital Input Connections

The MIC-3756 has 32 isolated digital input channels designated DI00~DI31.

Interrupt function of the DI signals

There are 2 channels (DI00 and DI16) that can be used to generate hardware interrupts. Users can setup the interrupt configuration by programming the interrupt control register. For detailed information, please refer to *Section 5.1 Interrupt Function.*

Isolated Inputs

Each isolated digital input channels accepts 10~50 VDC voltage input, and accepts bi-directional input, which means that you can apply positive or negative voltage to an isolated input pin. Every 16-input channels share one common pins. *Fig. 3-3* shows how to connect an external input source to one of the card' s isolated input channels

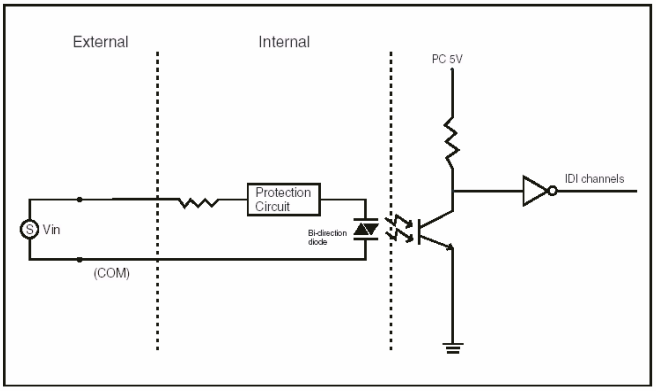


Fig. 3-3 Isolated digital input connection

3.4 Isolated Digital Output Connections

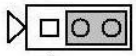
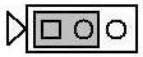
The MIC-3756 has 32 isolated digital output channels designated DO00~DO31.

Power On Configuration

Once the power is on, the default configuration will be when the hardware resets all the isolated output channels to off status (the current of the load can't be sink) so users need not worry about damaging external devices during system startup or reset.

When the system resets, the status of isolated digital output channels are selected by jumper JP3. *Table 3-2* shows the configuration of jumper JP3.

Table 3-2 JP3 Power on configuration after hot reset

MIC-3756 JP3	Power on configuration after hot reset
	Keeps last status after hot reset
	Loads default configuration while resetting

Isolated Outputs

Each isolated output channels come equipped with a Darlington transistor. Every 16 output channels share common collectors and integral suppression diodes for inductive loads.

Note:

If an external voltage (5 ~ 40 VDC) is applied to an isolated output

channel while it is being used as an output channel, the current will flow from the external voltage source to the card. Please keep in mind that the current through each IDO pin do not exceed 200 mA.

Fig. 3-4 shows how to connect an external output load to the card' s isolated outputs.

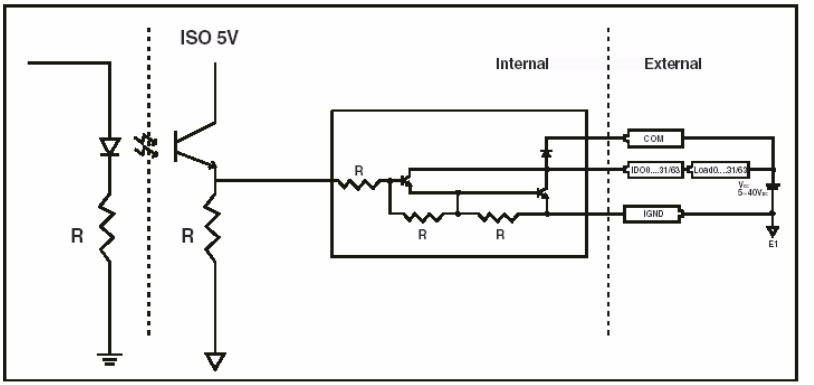


Fig. 3-4 Isolated Digital Output Connection

3.5 Field Wiring Considerations

When you use the MIC-3756 to acquire data from outside, noises in the environment might significantly affect the accuracy of your measurement. The following measures will be helpful to reduce possible interference running signal wires between signal sources and the MIC-3756.

- The signal cables must be kept away from strong electromagnetic sources such as power lines, large electric motors, circuit breakers or welding machines, since they may cause strong electromagnetic interference. Keep the analog signal cables away from any video monitor, since it can significantly affect a data acquisition system.

- If the cable travels through an area with significant electromagnetic interference, you should adopt individually shielded, twisted-pair wires as the analog input cable. This type of cable has its signal wires twisted together and shielded with a metal mesh. The metal mesh should only be connected to one point at the signal source ground.

- Avoid running the signal cables through any conduit that might have power lines in it.

- If you have to place your signal cable parallel to a power line that has a high voltage or high current running through it, try to keep a safe distance between them. Or you should place the signal cable at a right angle to the power line to minimize the undesirable effect.

CHAPTER 4

Operations

(This page is left blank for hard printing.)

4. Operations

This chapter describes the operation of the MIC-3756. The software driver provided allows a user to access all the card' s functions without register level programming. For users who prefer to implement their own bit-level programming, please refer to the following information in this chapter.

4.1 Interrupt Function

The isolated digital input channels (DI00 and DI16 in MIC-3756) are connected to the interrupt circuitry. Users can disable/enable interrupt function, select trigger type or latch the port data by setting the *Interrupt Control Register* of the MIC-3756. When the interrupt request signals occur, then the software will service these interrupt requests by ISR. The multiple interrupt sources provide the card with more capability and flexibility.

IRQ Level

The IRQ level is set automatically by the PCI plug-and-play BIOS and is saved in the PCI controller. There is no need for users to set the IRQ level. Only one IRQ level is used by this card, although it has two or four interrupt sources.

Interrupt Control Register

The *Interrupt Control Register* controls the function and status of each

interrupt signal source. *Table 4-1* shows the bit map of the *Interrupt Control Register*. The register is a readable/writable register. When it's written, it is used as a control register; and when it' s being read, it is used as a status register.

Table 4-1 Interrupt control register bit map

	Group n interrupt control register			
Base Add.+8+2n	3	2	1	0
Abbreviation	Fn	En	INTn/E	Ln/E

n: the group's number

Ln/E: Latch port data disable/enable control bit

INTn/E: Interrupt disable/enable control bit

En: Interrupt triggering edge control bit

Fn: Interrupt flag bit

Latch Port Data Function

The function enables you to latch the last data of each associated digital input channels when the interrupt occurs and you can free the latch function by clearing interrupt. We have organized every 16 bits in one group. When the Latch Port Data Function is enabled for a specific group, the values of all channel ports in this group will be latched. The function is determined by the value in the *latch port data disable/enable control* bit in the interrupt control register, as shown in *Table 4-2*.

Table 4-2 Latch port data disable/enable control bit

Ln/E	Latch port data when the interrupt occurs
0	Disable
1	Enable

Interrupt Enable Control Function

The user can choose to enable or disable the interrupt function by writing its corresponding value to the *interrupt disable/enable control* bit in the *interrupt control registe*r, as shown in *Table 4-3*.

Table 4-3 Interrupt disable/enable control bit values

INTn/E	Interrupt control
0	Disable
1	Enable

Interrupt Triggering Edge Control

The interrupt can be triggered by a rising edge or a falling edge of the interrupt signal, as determined by the value in the *interrupt triggering edge control* bit in the interrupt control register, as shown in *Table 4-4*.

Table 4-4 Interrupt triggering edge control bit values

En	Triggering edge of interrupt signal
0	Falling edge trigger
1	Rising edge trigger

Interrupt Flag Bit

The *interrupt flag* bit is a flag indicating the status of an interrupt. It is a readable/writable bit. To find the status of the interrupt, you have to read the bit value; to clear the interrupt, you have to write "1" to this bit. This bit must first be cleared to service the next incoming interrupt.

Table 4-5 Interrupt flag bit values

Fn		Interrupt status
Read	**0**	No interrupt
	1	Interrupt occur
Write	**0**	Don't care
	1	Clear interrupt

4.2 Board ID

The MIC-3756 has a built-in DIP switch (SW1), which is used to define its board ID. You can determine the board ID on the register as shown on *Table 4-6*. When there are multiple cards on the same chassis, this board ID setting function is useful for identifying each card's device number through board ID. We set the MIC-3756 board ID as 0. If you need to adjust it to other board ID, set the SW1 by referring to the *Table 4-7*.

Table 4-6 Board ID register

	Board ID register			
Base Add.+10 h	3	2	1	0
Abbreviation	ID3	ID2	ID1	ID0

ID0: the least significant bit (LSB) of Board ID

ID3: the most significant bit (MSB) of Board ID

Table 4-7 Board ID setting

Board ID Setting (SW1)				
Board ID(DEC)	**Switch Position**			
	3	**2**	**1**	**0**
0*	ON	ON	ON	ON
1	ON	ON	ON	OFF
2	ON	ON	OFF	ON
3	ON	ON	OFF	OFF
4	ON	OFF	ON	ON
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	ON
7	ON	OFF	OFF	OFF
8	OFF	ON	ON	ON
9	OFF	ON	ON	OFF
10	OFF	ON	OFF	ON
11	OFF	ON	OFF	OFF
12	OFF	OFF	ON	ON
13	OFF	OFF	ON	OFF
14	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF
* : Default				

4.3 Channel-Freeze Function

The MIC-3756 provides the *Channel-Freeze* function for isolated digital output channels. When *Channel-Freeze* function is enabled, all ports on the card will be locked so that the data transmitted (from the host PC) to the card won't be transferred to the DO ports. Once the *Channel-Freeze* function is enabled, each port status is immediately frozen into its last valid value before the *Channel-Freeze*. Since the value transmitted (from the host PC) to the card is also stored in the buffer on the PC, thus when users call the ***DRV_DioGet CurrentDOByte ( )*** function to read back the DO channel value, this function will determine that:

If Channel-Freeze function is disabled, it will return the DO value on the port;

If Channel-Freeze function is enabled, it will return the value from the buffers on host PC.

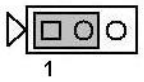
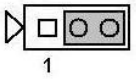
The MIC-3756 provides digital input channel (CH_FRZ_IN) to enable channel-freeze function. The channel-freeze function acts when the pin CH_FRZ_IN is activated. Moreover, you can setup the input mode of channel-freeze function input channel CH_FRZ_IN as dry contact input mode or wet contact input mode selected by on-board jumper JP2, as shown in *Table 4-8*. The wiring in wet contact and dry contact input mode are shown in *Fig. 4-2*. Otherwise, you also can enable the function through software by writing "1" to CFC (Channel-Freeze Function Control) bit on channel-freeze function register, as shown in *Table 4-9* and *Table 4-10*. It's useful in software simulation and

testing program.

The CFS (Channel-Freeze Function Status) bit shows the status of Channel-Freeze function:

A value of 1 for the CFS bit indicates an active Channel-Freeze Function; whereas a value of 0 indicates a non-active Channel-Freeze Function.

Table 4-8 JP2 Channel-Freeze function input mode

MIC-3756 JP2	Input Mode
	Dry contact input mode
	Normal mode (Wet contact input mode)

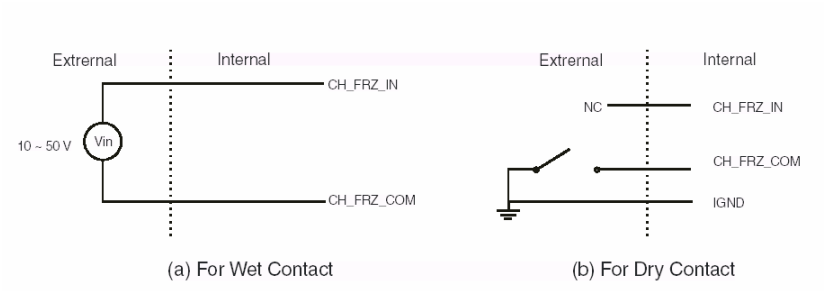


Fig. 4-2 The wiring in wet/dry contact input mode

Table 4-9 Channel-Freeze function register

	Channel-Freeze function register			
Base Add.+12 h	3	2	1	0
Abbreviation			CFS	CFC

Table 4-10 Channel-Freeze function bit value

CFC	**Channel-Freeze function control**
0	Disable
1	Enable
CFS	**Channel-Freeze function status**
0	OFF
1	ON

4.4 Counter Function

The MIC-3756 provides one 16-bit up Counter/Timer function. Counter/Timer function can be configured by setting the corresponding counter registers. Moreover, you can setup the Counter/Timer mode by Counter Mode Register, as shown in *Table 4-11*.

Table 4-11 Counter Mode Register

	Counter Mode Register					
Base Add.+ Ch	5	4	3	2	1	0
Abbreviation	CM5	CM4	CM3	CM2	CM1	CM0

Counter Mode Register
Counter Gate control: CM1, CM0
00 = stop counter
01 = DI16 as GATE high
10 = DI16 as GATE low
11 = No Gating
Interrupt Control Register: CM2
0 = disable interrupt
1 = Enable interrupt
CLK source control: CM3
0 = DI00
1 = 1MHz clock source on broad
DO00 output Control: CM5, CM4
00 = Digital Output DO00
01 = Counter output TC Toggle from low
10 = Counter output TC

Table 4-12 shows the counter read back value register. Users can read this register to get the current value of counter. *Table 4-13* show the counter set value register. The register can set the initial value of counter, and the MAX of initial value is 65535.

Table 4-12 Counter Read Register

	Counter Read Register
Base Add.+ 14h	Bit 15~0
Abbreviation	CR15~0

Table 4-13 Set Value Register

	Set Value Register
Base Add.+ 18h	Bit 15~0
Abbreviation	SE15~0

Note: The default value of Set Value Register is 65535 when power on and counter reset

Table 4-14 shows the counter reset register.

Table 4-14 Counter Reset Register

	Counter Reset Register		
Base Add.+ Eh	Bit 15~2	Bit1	Bit0
Abbreviation	N/A	Clear TC Toggle	Reset All Count register

Counter Reset Register: Bit [1,0]

X 0 = reset all counter register *

01 = only clear TC toggle output

NOTE: * "X" means "don't care".

Table 4-15 shows how to set the counter INT. The Counter INT state register is the read-only register. When Bit0 is "1", the counter's interrupt has occurred. To clear the interrupt of counter, users can write any value (including "0") to the Clear INT register. The Clear INT register is write-only register and has the same address as the INT State register.

Table 4-15 INT Register of Counter

	INT State Register
Base Add.+ 16h (Read Only)	Bit 0
Abbreviation	INT
	Clear INT Register
Base Add.+ 16h (Write Only)	Bit15~0
Abbreviation	Any value

Output Control

Counter mode bits CM4 and CM5 specify the output control configuration. (Refer to register format) select the active output type: Digital output, Counter output TC, or TC Toggle from low output waveforms.

One output form available is called Terminal Count (TC) and represents the period in time that the counter reaches an equivalent value in the Set Value Register (Base Add. + 18h). The TC width is determined by the period of the counting source. The TC will be

active for only one clock cycle. The other output form, TC Toggle, uses the trailing edge of TC to toggle a flip-flop to generate an output level instead of a pulse. The toggle output is 1/2 the frequency of TC. The TC Toggled output will frequently be used to generate variable duty-cycle square waves.

Users can clear the Toggled output by writing the Count Reset Register (Base Add. + Eh). If Bit0 of the Count Reset Register is Logic“1”, write logic“0” into the Bit1 of Count Reset Register, Users can clear the Toggle output.

Count Source Selection

Counter Mode bits CM3 specify the source used as input to the counter and the active edge that is counted. Logic“1” counter clock comes from 1M crystal on board. Logic“0” counter clock come from DI00 pin.

Gating Control

Counter Mode bits CM1 and CM0 specify the hardware gating options. When “no gating” is selected (CM1, CM0 = 11), the counter will proceed unconditionally as long as it is clocked. For any other gating mode, the count process is conditioned by the specified gating configuration. The gating source comes from DI16. The Gate is level sensitive. When it goes low, counting is simply suspended until the Gate goes high again. When “DI16 as GATE high” is selected (CM1, CM0 = 01), counting can proceed only when the Gate source is logical high level. When “DI16 as GATE low” is selected (CM1, CM0 = 10),

counting can proceed only when the Gate source is logical low level. When “Stop Counter” is selected (CM1, CM0 = 00), counting will stop, and the current value of the counter is held in the Counter Read Register (Base add. + 14h).

Counter Reset

This command will reset the counter, set value, set mode and INT register to a preset condition. The value is 0000 hex.

NOTE: The default value of register is “0000”.

Appendixes

(This page is left blank for hard printing.)

Appendix A. Specifications

Isolated Digital Input

Number of Input Channel	32		
Interrupt Inputs	2 (DI00, DI16)		
Optical Isolation	2500 V DC		
Photo-Couple response time	Input Voltage	*OFF delay (± 20%)	*ON delay (± 20%)
	5V	100us	60us
	12V	120us	10us
	24V	140us	5us
	30V	150us	4us
	50V	200us	4us
Over- voltage Protect	70 V DC		
Input Voltage	VIH (max.)	50 V DC	
	VIH (min.)	5 V DC	
	VIL (max.)	2 V DC	
Input Resistance	1KΩ(50V) ~ 4KΩ(5V)		

*OFF delay mean the Photo-Couple turn OFF delay time when DI input voltage be removed.
*ON delay mean the Photo-Couple turn ON delay time when DI input voltage be connected up.

Isolated Digital Output

Number of Output Channel	32	
Optical Isolation	2500 VDC	
DO response time	OFF delay (± 20%)	ON delay (± 20%)
	5us	120us
Supply Voltage	5 ~ 40 VDC	
Sink Current	200 mA max/channel	

Counter

Channels	1 (independent)	
Resolution	16-bit	
Programmable Clock Source	On board 1MHz clock source or External DI00 input	
Gate Control	Stop counter	
	DI16 as GATE high	
	DI16 as GATE low	
	No Gating	

General

I/O Connector Type	78-pin DB female	
Dimensions	160 mm(L)x 100 mm(W)	
Power Consumption	+5V @ 220 mA	
	+3.3V @ 260 mA	
Temperature	Operation	0 ~ +60° C (refer to IEC 68-2-1,2)
	Storage	-20 ~ +80° C
Relative Humidity	5 - 95 % RH non-condensing(refer to IEC 68-2-3)	
Certification	CE Class A certified	

Appendix B. Register Structure and format

B.1 Register Structure

The MIC-3756 is delivered with an easy-to-use 32-bit DLL driver for users to program under Windows 98/NT/2000/XP. We advise users to program the MIC-3756 using the 32-bit DLL driver provided by Advantech to avoid complexity of low-level programming by register.

The most important consideration in programming the MIC-3756 at the register level is to understand the function of the card's registers. The information in the following sections will assist users who would program their own low-level programming.

The MIC-3756 requires 32 consecutive addresses in the PC's I/O space. The address of each register is specified as an offset from the card's base address. For example, BASE+0 is the card's base address and BASE+7 is the base address plus seven bytes.

B.2 Register Format

MIC-3756 Register Format																	
Base Add.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R	Digital Input Group 0															
		DI 15	DI 14	DI 13	DI 12	DI 11	DI 10	DI 9	DI 8	DI 7	DI 6	DI 5	DI 4	DI 3	DI 2	DI 1	DI 0
	W	NA															
2	R	Digital Input Group 1															
		DI31	DI30	DI29	DI28	DI27	DI26	DI25	DI24	DI23	DI22	DI21	DI20	DI19	DI18	DI17	DI16
	W	NA															
4	R	Digital Output Group 0 Read Back															
		DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
	W	Digital Output Group 0															
		DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
6	R	Digital Output Group 1 Read Back															
		DO31	DO30	DO29	DO28	DO27	DO26	DO25	DO24	DO23	DO22	DO21	DO20	DO19	DO18	DO17	DO16
	W	Digital Output Group 1															
		DO31	DO30	DO29	DO28	DO27	DO26	DO25	DO24	DO23	DO22	DO21	DO20	DO19	DO18	DO17	DO16
8	R	Group 0 Interrupt Control Register															
														F0	E0	INT0/E	L0/E
	W	Group 0 Interrupt Control Register															
														F0*	E0	INT0/E	L0/E
A	R	Group 1 Interrupt Control Register															
														F1	E1	INT1/E	L1/E
	W	Group 1 Interrupt Control Register															
														F1*	E1	INT1/E	L1/E

MIC-3756 Register Format (Continue)

Base Add.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	**R**	NA															
	W	Counter Mode Register										CM5	CM4	CM3	CM2	CM1	CM0
E	**R**	NA															
	W	Counter Reset Register														D1	D0
10	R	Board ID Register												ID3	ID2	ID1	ID0
	W	N/A															
12	R	Channel-Freeze Function Control Register														CFS	CFC
	W	Channel-Freeze Function Status Register															CFC
14	R	Counter Read Register															
		CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
	W	NA															
16	R	INT State of Counter															INT
	W	Clear INT of Counter															
18	R	NA															
	W	Set Value Register															
		SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0
1E	R																
	W																

Note:

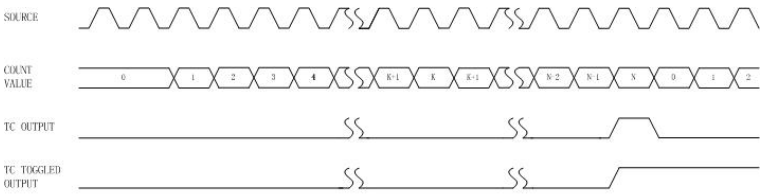
Write “1” to the bit Fn in Interrupt Control Register clears the interrupt

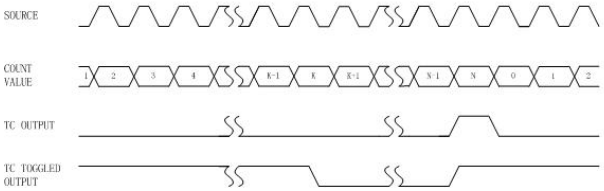
Appendix C. Waveform of Counter Mode

The MIC-3756 offers 1 counter function to fulfill your industrial or laboratory applications. This chapter will describe each counter mode in detail with the waveform diagram.

Counter Mode without Gate Control

In this mode, the gate input does not affect counter operation. Once started, the counter will count to TC repetitively. On each TC the counter will reload the initial value from the counter set value register (Base Add. + 18h); hence the value in the set value register determines the time between TCs. The counter output mode may be obtained with the TC output mode or the TC Toggled output mode by specifying in the Counter Mode register (CM5, CM4); Toggled output uses the trailing edge of TC to toggle a flip-flop to generate an output level instead of a pulse. During the TC Toggled output mode, once the output toggled, it will hold high output level and ignore the following TCs until users clear the Toggled output by writing the Bit1of Count Reset Register (Base Add. + Eh). If Bit0 of the Count Reset Register is Logic“1”, write logic“0” into the Bit1 of Count Reset Register, users can clear the Toggle output.



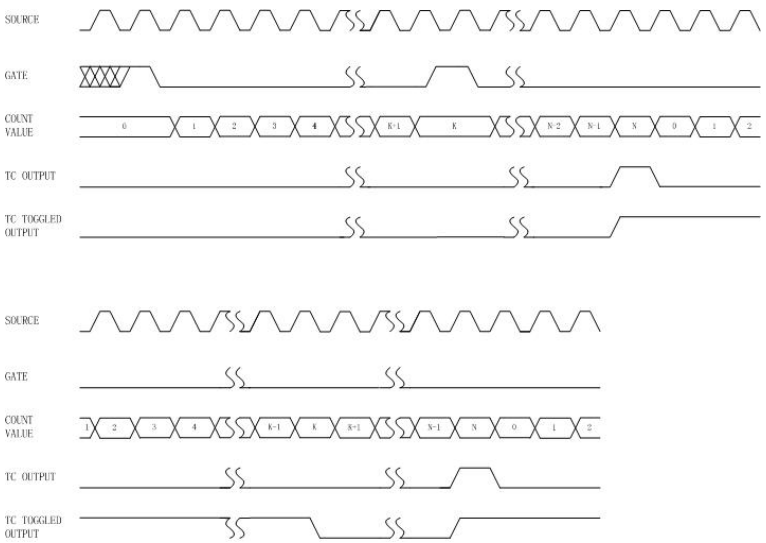


Counter Mode with Low Level Active Gate Control

In this mode, the gate input affects counter operation. Once started, the counter will count to TC repetitively. The counter will count all source edges that occurred while the gate low level is active and disregard those edges that occurred while the gate is inactive.

On each TC the counter will reload the initial value of counter from the counter set value register (Base Add. + 18h). The counter output mode may be obtained with the TC output mode or the TC toggled output mode by specifying in the Counter Mode register (CM5, CM4); Toggled output uses the trailing edge of TC to toggle a flip-flop to generate an output level instead of a pulse. During the TC Toggled output mode, it will hold high output level and ignore the following TCs until users clear the toggled output by writing the Bit1 of Count Reset Register (Base Add. + Eh). If Bit0 of the Count Reset Register

is Logic“1”, write logic“0” into the Bit1 of Count Reset Register, Users can clear the toggle output.



Counter Mode with High Level Active Gate Control

In this mode, the gate input affects counter operation. Once started, the counter will count to TC repetitively. The counter will count all source edges that occurred while the gate high level is active and disregard those edges that occurred while the gate is inactive.

On each TC the counter will reload the initial value of counter from the counter set value register (Base Add.+ 18h). The counter output mode may be obtained with the TC output mode or the TC toggled output mode by specifying in the counter mode register (CM5, CM4);

Toggled output uses the trailing edge of TC to toggle a flip-flop to generate an output level instead of a pulse. During the TC toggled output mode, it will hold high output level and ignore the following TCs until users clear the toggled output by writing the Bit1 of count reset register (Base Add. + Eh). If Bit0 of the count reset register is Logic“1”, write logic“0” into the Bit1 of count reset register, users can clear the toggle output.