MIC-3451/MIC-3451H

6U-sized, 8-slot Backplane for *CompactPCI*®

Copyright Notice

Acknowledgements

Part Number: 2003345100 1st Edition

Printed in Taiwan April 1999

Product warranty

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for one year from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Packing List

Before installation, ensure that the following materials have been received:

* The MIC-3451/MIC-3451H backplane

* This user's manual

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Technical Support and Sales Assistance

If you have any technical questions about the MIC-3451/MIC-3451H or any other Advantech products, please visit our support website at:

- **http://support.advantech.com.tw**

For more information about Advantech's products and sales information, please visit:

- **http://www.advantech.com**

Contents

Figure

Tables

CHAPTER 1

Introduction

1.1 General Information

The MIC-3451/MIC-3451H is a 6U-sized general-purpose backplane that provides eight 32-bit or 64-bit (optional) CompactPCI slots. It accepts a 2-slot (8TE) or 3-slot (12TE) wide processor module and seven peripheral modules.

The MIC-3451/MIC-3451H includes standard IDE and floppy interface connectors on the backplane. Users can easily connect IDE devices and floppy drives to the backplane through the P3 connector on the system slot.

In order to provide users with a flexible system configuration, the MIC-3451/MIC-3451H includes two standard ATX power connectors and an optional two IEC 603-2 (DIN 41612) connectors to accept two ATX power supplies or two 3U size plug-in power modules.

The MIC-3451/MIC-3451H provides a 6-pin connector for connecting to up to 4 cooling fans. A 20-pin connector can be used for connecting an external alarm module (MIC-3920/MIC-3921) to detect system internal conditions, such as bus voltages and fan speed.

The MIC-3451H complies with PICMG 2.1 Hot-Swap Specification providing full hot-swapping capability. Users can build a hot-swap system using hot-swap plug-in boards and software.

1.2 Features

- Eight 32-bit CompactPCI slots (64-bit upon request)
- Supports hot-swappable modules (MIC-3451H)
- Accepts two ATX power supplies or two plug-in power modules (optional, upon request)
- IDE and floppy drive interface
- Alarm board interface
- Fan interface

1.3 Specification

- 8 CompactPCI slots (one system slot and 7 peripheral slots)
- Bus width: 32-bit (64-bit upon request)
- 8-layer PCB, 3.0 mm thick
- Separate power and ground planes
- Power connectors:
  - Two ATX power connectors for connecting standard ATX power supplies
  - Screw terminals (on rear side) for external power inputs
  - Two IEC 603-2(DIN 41612) power connectors for two 2-slot wide plug-in power modules, or two 3-slot wide power modules (the connectors are upon request)
- 20-pin connector for MIC-3920/MIC-3921 alarm board signals
- Two IDE and one FDD connectors (routed to P3 connector, supporting Advantech's 6U processor module)
- Complies with CompactPCI Specification PICMG 2.0, Ver.2.1
- Complies with CompactPCI Hot Swap Specification PICMG 2.1, Ver.1.0 (MIC-3451H)
- V I/O Voltage: 3.3 V or 5 V, jumper selectable
- Supports PXI star trigger signals (optional)
- Logic Ground and Chassis Ground can be isolated or common
- Dimensions: 243.2 x 262.2 mm
- Operating temperature: -40 ~ 80°C (-40 ~ 176°F)

CHAPTER 2

Hardware Configuration

2.1 Connector Locations

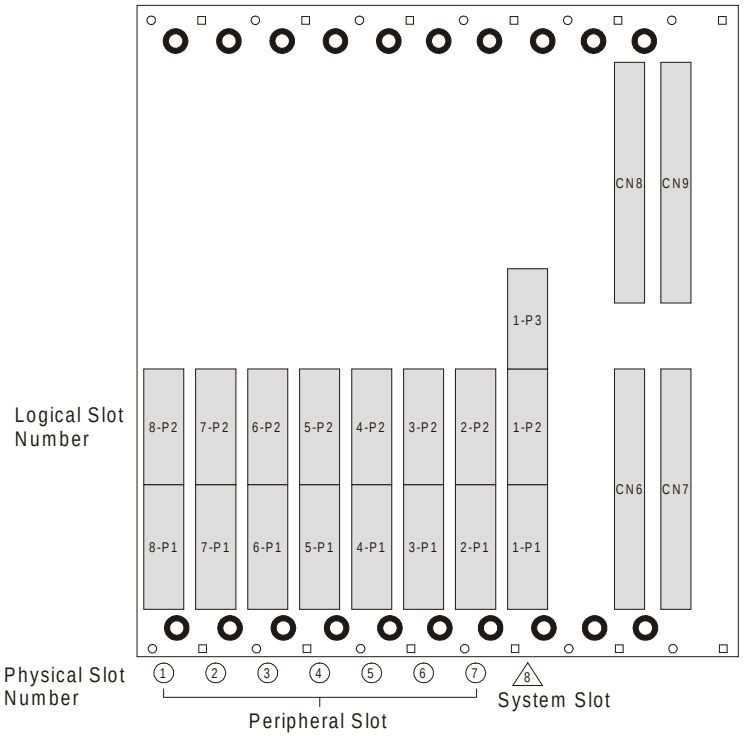


Figure 2-1. The connector locations on the front side

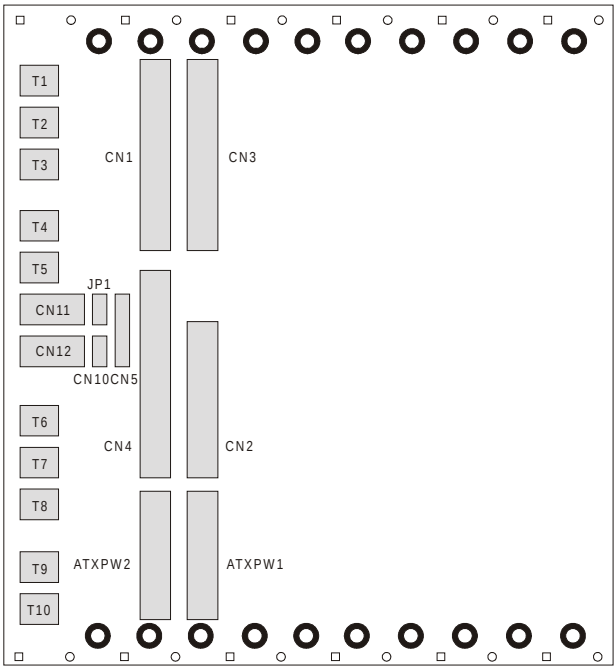


Figure 2-2. The connector locations on the rear side

Table 2-1. Connector Assignments

Name	Function
Slot 8	System Slot Connector
Slot 1~7	Peripheral Slot Connectors
CN1 and CN3	IDE Device Interface Connectors
CN2	Alarm Board Interface Connector
CN4	Floppy Drive Interface Connector
CN5	Fan Module Connector
CN6~CN9	Plug-in Power Module Connectors
CN10	Power Switch Connector
CN11 and CN12	Peripheral Power Connectors
JP1	V I/O Voltage Selection Jumper
ATXPW1 and ATXPW2	ATX Power Connectors
T1~T10	Power Inlet and Ground Screw Terminals

2.2 Slot Assignments

The CompactPCI specification defines slot numbering seperating for physical and logical slots. Each slot has a physical number and a logical number (refer to the CompactPCI specification version 2.0 R2.1 for further information on slot assignments). The physical numbers are printed on the backplane, enclosed in circles or triangles, below each slot. Slot 8, marked by a triangle, is the system slot and can only be used by a processor module. The other slots (slot 1~7) are peripheral slots and can be used by peripheral modules.

The logical number of each slot is defined according to the IDSEL signal and the associated address used to select the slot. Table 2-2 shows the system slot to peripheral slot relationships on the MIC-3451/MIC-3451H. Physical slot 8 (system slot) has a logical number 1, physical slot 7 has a logical number 2, physical slot 6 has a logical number 3, ..., and physical slot 1 has a logical number 8. The connectors in logical slot 1 are designated as 1-P1, 1-P2, and 1-P3. Nomenclature for connectors in other slots is similar, such as 2-P1, 2-P2, 3-P1, 3-P2, etc.

Connector 1-P1 is a keyed connector providing 32-bit CompactPCI busing between the system slot and the peripheral slots (2-P1~8-P1). Connector 1-P2 is an un-keyed connector providing 64-bit Compact-PCI busing between the system slot and the peripheral slots (2-P2~ 8-P2). Connector 1-P3 is an un-keyed 19-row connector providing IDE device and floppy drive interfaces (Advantech's Definition).

Table 2-2. System to Peripheral Slot Signal Assignment

Signal	Connector: Pin	Signal	Connector: Pin
System Slot 8, (Logical Slot 1):		Peripheral Slot 7, (Logical slot 2)	
CLK1 AD31 REQ0# GNT0#	P2:A1 P1:E6 P1:A6 P1:E5	CLK IDSEL REQ# GNT#	P1:D6 P1:B9 P1:A6 P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 6, (Logical slot 3)	
*CLK1(CLK6) AD30 REQ1# GNT1#	*P2:A1(P2:A21) P1:A7 P2:C1 P2:D1	CLK IDSEL REQ# GNT#	P1:D6 P1:B9 P1:A6 P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 5, (Logical slot 4)	
CLK0 AD29 REQ2# GNT2#	P1:D6 P1:B7 P2:E1 P2:D2	CLK IDSEL REQ# GNT#	P1:D6 P1:B9 P1:A6 P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 4, (Logical slot 5)	
*CLK0 (CLK5) AD28 REQ3# GNT3#	*P1:D6 (P2:A20) P1:C7 P2:E2 P2:C3	CLK IDSEL REQ# GNT#	P1:D6 P1:B9 P1:A6 P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 3, (Logical slot 6)	
CLK2 AD27 REQ4# GNT4#	P2:A2 P1:E7 P2:D3 P2:E3	CLK IDSEL REQ# GNT#	P1:D6 P1:B9 P1:A6 P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 2, (Logical slot 7)	
CLK3 AD26 REQ5# GNT5#	P2:B2 P1:A8 P2:D15 P2:E15	CLK IDSEL REQ# GNT#	P1:D6 P1:B9 P1:A6 P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 1, (Logical slot 8)	
CLK4 AD25 REQ6# GNT6#	P2:A3 P1:D8 P2:D17 P2:E17	CLK IDSEL REQ# GNT#	P1:D6 P1:B9 P1:A6 P1:E5

* MIC-3451H clock definitions and pin locations are in the parentheses. Please refer to section 2-9 Clock Routing Configuration.

Table 2-3. Connector Pin Assignments of P1 and P2 (System Slot)

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2 / J2 CONNECTOR
21	GND	CLK6	GND	RSV	RSV	RSV	GND	
20	GND	CLK5	GND	RSV	GND	RSV	GND	
19	GND	GND	GND	RSV	RSV	RSV	GND	
18	GND	*PXI_TRIG3	*PXI_TRIG4	*PXI_TRIG5	GND	*PXI_TRIG6	GND	
17	GND	*PXI_TRIG2	GND	PRST#	REQ6#	GNT6#	GND	
16	GND	*PXI_TRIG1	*PXI_TRIG0	DEG#	GND	*PXI_TRIG7	GND	
15	GND	*PXI_BRSVA15	GND	FAL#	REQ5#	GNT5#	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	*PXI_BRSVB4	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND	
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1 / J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	
12-14	KEY AREA							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z	A	B	C	D	E	F	

= long pins = short pins = medium length pins

*: Optional signals for PXI® star trigger signals

#: Low active

Note: GA[4...0] shall be used for geographic addressing on the backplane

Table 2-4. Connector Pin Assignments of P1 and P2 (Peripheral Slot)

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2 / J2 CONNECTOR
21	GND	*PXI_LBR0	GND	*PXI_LBR1	*PXI_LBR2	*PXI_LBR3	GND	
20	GND	*PXI_LBR4	*PXI_LBR5	*PXI_LBR0	GND	*PXI_LBR1	GND	
19	GND	*PXI_LBL2	GND	*PXI_LBL3	*PXI_LBL4	*PXI_LBL5	GND	
18	GND	*PXI_TRIG3	*PXI_TRIG4	*PXI_TRIG5	GND	*PXI_TRIG6	GND	
17	GND	*PXI_TRIG2	GND	PRST#	*PXI_STAR	*PXI_CLK10	GND	
16	GND	*PXI_TRIG1	*PXI_TRIG0	DEG#	GND	*PXI_TRIG7	GND	
15	GND	*PXI_BRSVA15	GND	FAL#	*PXI_LBL6	*PXI_LBR6	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	*PXI_BRSVB4	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	*PXI_LBR7	GND	*PXI_LBR8	*PXI_LBR9	*PXI_LBR10	GND	
2	GND	*PXI_LBR11	*PXI_LBR12	SYSEN#	*PXI_LBL7	*PXI_LBL8	GND	
1	GND	*PXI_LBL9	GND	*PXI_LBL10	*PXI_LBL11	*PXI_LBL12	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1 / J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	
12-14	KEY AREA							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z	A	B	C	D	E	F	

= long pins = short pins = medium length pins

*: Optional signals for PXI® star trigger signals

#: Low active

Note: GA[4...0] shall be used for geographic addressing on the backplane

Table 2-5. Connector Pin Assignments of 1-P3

	Z	A	B	C	D	E	F
19	GND	IDE2D3	IDE2D6	IDE2D2	IDE2D10	IDE2D14	GND
18	GND	IDE2D8	IDE2D5	IDE2D1	IDE2D11	IDE2D15	GND
17	GND	IDE2D9	IDE2D4	IDE2D0	IDE2D12	IDE2D13	GND
16	GND	IDE2D7	IDE2CS0-	IDE2IOR-	IDE2CS1-	IDE2RDY	GND
15	GND	IDE2DRQ	IDE2ACK-	IDE2SA2	IDE2IRQ	IDE2IOW-	GND
14	GND	N/C	N/C	IDE2SA1	GND	IDE2SA0	GND
13	GND	N/C	N/C	N/C	N/C	N/C	GND
12	GND	IDE1D0	IDE1D2	IDE1D4	IDE1D7	N/C	GND
11	GND	IDE1D1	IDE1D3	IDE1D8	IDE1D6	IDE1D12	GND
10	GND	IDE1D5	IDE1D9	IDE1D10	IDE1D11	IDE1D13	GND
9	GND	IDE1D15	IDE1D14	IDE1DRQ-	IDE1CS1-	IDE1IOR-	GND
8	GND	IRQ14	IDE1ACK-	VCC	IDE1SA2	IDE1IOW-	GND
7	GND	IDE1LED	GND	IDE1RST-	IDE1RDY	IDE1CS0-	GND
6	GND	+12V	VCC	GND	IDE1SA0	IDE1SA1	GND
5	GND	VCC	GPIO1	GPIO2	SDCLK	SDDAT	GND
4	GND	N/C	N/C	N/C	N/C	GND	GND
3	GND	DSKCHG-	MOTEA-	STEP-	SIDE1-	RDATA-	GND
2	GND	DRVA-	MOTEB-	DVSL-	WPT-	TK00	GND
1	GND	INDEX-	DRVB-	FDIR-	WGATE-	WDATA	GND

2.3 IDE Interface (CN1 and CN3)

The CN1 and CN3 connectors are routed to the 1-P3 connector for connection of IDE devices such as hard disk drives and CD-ROM drives. When using Advantech's 6U-sized processor module, users can connect IDE devices to the backplane, instead of direct cabling to the processor board. This shortens the MTTR (Mean Time To Repair) for replacing the processor board. The CN1 connector is for the primary IDE channel and the CN3 connector is for the secondary channel. Each channel can connect up to two IDE devices.

2.4 Floppy Disk Interface (CN4)

The CN4 connector is routed to the 1-P3 connector for connecting floppy disk drives. With Advantech's 6U-sized processor module, users can connect floppy disk drives to the backplane, instead of direct cabling to the processor board. This shortens the MTTR for replacing the processor board. Up to two floppy disk drives can be connected to CN4.

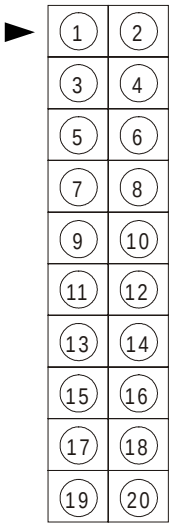
2.5 Alarm Board Interface (CN2)

The 20-pin connector CN2 is an interface for an external monitoring and alarm module, such as MIC-3920/MIC-3921, which monitors the system conditions. It contains bus voltages 3.3V, 5V, 12V and -12V, and utilizes four fan tachometer signals and an on-off control signal.

Table 2-6. CN2 Connector Pin Assignments

	Pin Assignment
20	FAN2
19	FAN1
18	FAN4
17	FAN3
16	N/C
15	POWER_FAIL#
14	SDCLK
13	GPI02
12	SDDAT
11	GPI01
10	N/C
9	PSON#
8	GND
7	GND
6	PRST#
5	+12V
4	-12V
3	+3.3V
2	+5V
1	+5V

#: Low active



CN2 Connector Pin Locations

2.6 Fan Module Connector (CN5)

The CN5 connector provides +12 V power for fan operation and accepts the tachometer output from the fans. It accepts up to four fan signals.

Table 2-7. CN5 Connector Pin Assignments

	Pin Assignment
6	+12V
5	GND
4	FAN1
3	FAN2
2	FAN3
1	FAN4

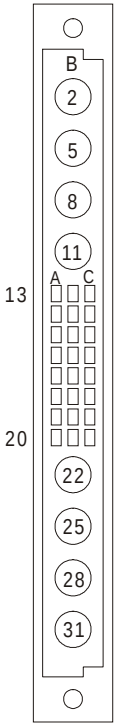
2.7 Power Connectors

2.7.1 Plug-in Power Module Connectors (CN6~CN9)(optional, upon request)

The CN7 and CN9 connectors accept two redundant, 3U high, 2-slot (8TE) wide power modules, or one 6U high power module.

In cases where users would like to install 3-slot (12TE) wide power modules, the modules can be mounted in the CN6 and CN8 connectors.

Upon customers request, two connectors can be mounted on either CN6 and CN8 or CN7 and CN9 position.



Power Module Connector Pin Locations

Table 2-8. Power Module Connector

	Name
Column A	
A13	SP
A14	INH#
A15	ISH
A16	5S-
A17	5S+
A18	3.3V
A19	+12V
A20	-12V
Column B	
B2	ACL
B5	ACN
B8	-
B11	CG
B13	3.3V
B14	3.3V
B15	3.3V
B16	3.3V
B17	3.3V
B18	3.3V
B19	+12V
B20	-12V
B22	5V
B25	GND
B28	+DC
B31	-DC
Column C	
C13	EN#
C14	DEG#
C15	FAL#
C16	3.3V
C17	3.3V
C18	3.3V
C19	+12V
C20	-12V

Note: Pin numbers illustrated are of the female backplane connector

2.7.2 ATX Power Connector (ATXPW1 and ATXPW2)

These connectors accept two standard ATX power supplies.

Note: Do not use ATX power supplies and plug-in power modules at the same time.

2.7.3 Power Connectors for Peripherals (CN11 and CN12)

The CN11 and CN12 connectors provide power to the peripherals, such as hard disk drives or floppy disk drives.

2.7.4 Power Inlet and Ground Screw Terminals (T1~T10)

These screw terminals accept AC or DC power input. T1 ~ T5 provides power to CN8 and CN9, and T6 ~ T10 provides power to CN6 and CN7. Depending on the input requirement (AC or DC) of the plug-in power modules intended for CN6~CN9, connect either AC or DC source power.

2.7.5 V I/O Voltage Selection (JP1)

This jumper is used to select the V I/O voltage. MIC-3451/ MIC-3451H allows V I/O to be set to either 5 V or 3.3 V. Connect the two pins labeled “+5 V” with a cap to set V I/O to 5 V, and connect the two pins labeled “+3.3 V” with a cap to set V I/O to 3.3 V. Since the MIC-3451/MIC-3451H default is configured for use with 5 V CompactPCI boards (blue keyed connectors), once the jumper is set to 3.3 V, the CompactPCI keys must be changed to 3.3 V at the same time (as yellow keyed connectors).

2.7.6 Power Switch (CN10)

This connector provides power on/off control of the ATX power supply or the plug-in power module.

2.7.7 Screw terminal for external power supply

Along the upper and lower edges of the MIC-3451/MIC-3451H are 20 power pads providing external power supply I/O. Pads S1~S20 facilitate input or output of the different powers and grounds. Contact Advantech for installation help.

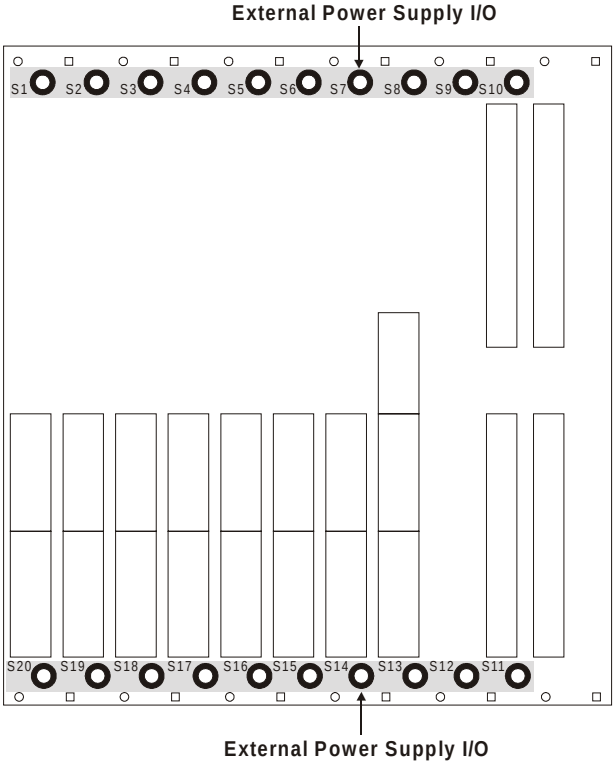


Figure 2-3 External Power Supply Terminal

Table 2-9. External Power Supply Terminal

	Name
S20	CHS_GND
S19	+5V
S18	GND
S17	+5V
S16	GND
S15	+3.3V
S14	GND
S13	-12V
S12	GND
S11	+12V
S10	CHS_GND
S9	+5V
S8	GND
S7	+3.3V
S6	GND
S5	+5V
S4	GND
S3	+5V
S2	GND
S1	+3.3V

2.8 Ground Configuration

Along the top and bottom of the MIC-3451/MIC-3451H are 24 mounting holes. The holes are arranged in an alternating pattern of chassis (frame) grounded pads and logic grounded pads. The square pad holes are connected to chassis ground, and the round pad holes are connected to logic ground. To isolate chassis and logic grounds, install mounting screws in only square pad mounting holes.

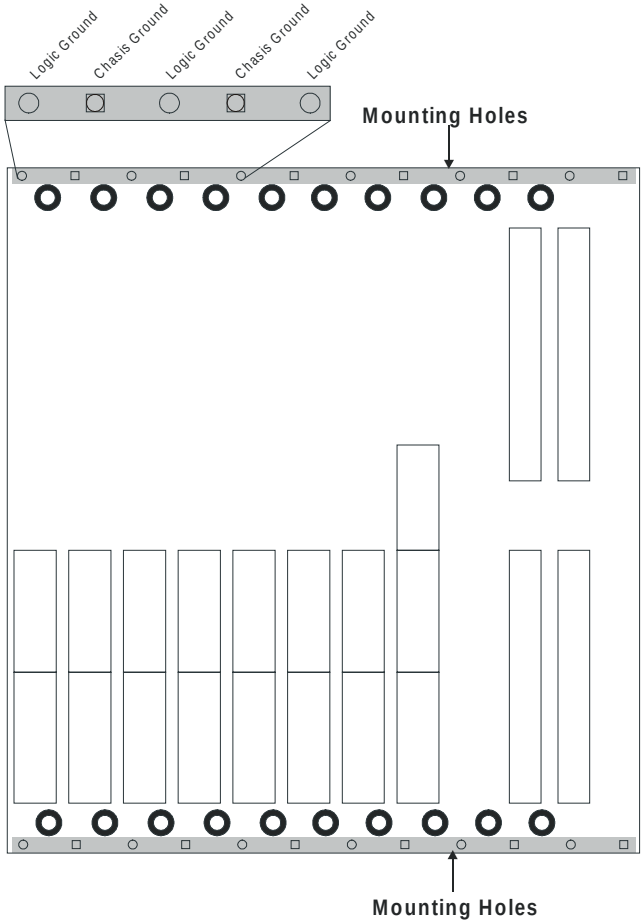


Figure 2-4. Mounting Holes Illustration

2.9 Clock Routing Configuration

Depending on the configuration option ordered (MIC-3451 or MIC-3451H), the backplane is compatible with individual clock CPUs or shared clock CPUs. The MIC-3451H is configured to comply with the clock routing specified in the CompactPCI Hot Swap Specification, PICMG 2.1, version 1.0. This Specification requires that each slot be independently clocked. By removing several 0 Ω resistors, the clock routing can be reconfigured to comply with the earlier CompactPCI Specification, PICMG 2.0, version 2.1. Reconfiguring the backplane to comply with this earlier specification allows the MIC-3451 to be backward compatible with CPUs using shared clocks.

Individual Clock CPUs (MIC-3451H)
Installed: R9, R11
Not Installed: R8, R10

Shared Clock CPUs (MIC-3451)
Installed: R8, R10
Not Installed: R9, R11

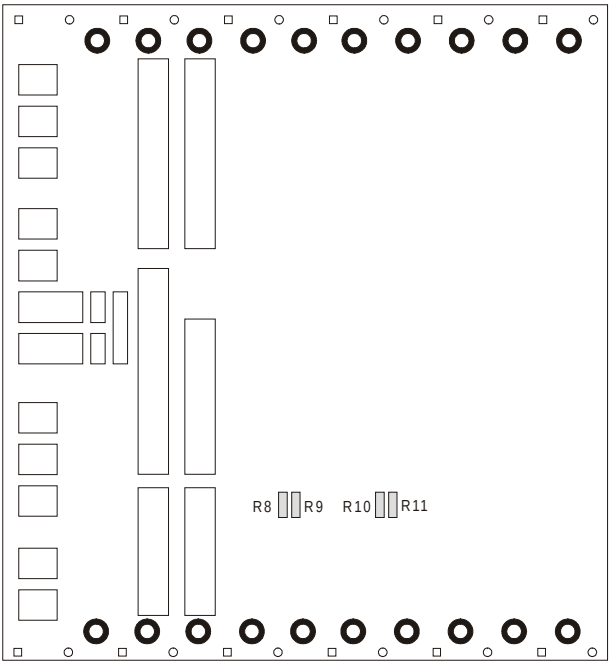


Figure 2-5. Configuration Resistors Locations