MIC-3401/MIC-3401H

3U-sized, 8-slot Backplane

for *CompactPCI* ®

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Packing List

Before installation, ensure that the following materials have been received:

* The MIC-3401/MIC-3401H backplane

* This user manual

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Technical Support and Sales Assistance

If you have any technical questions about the MIC-3401/MIC-3401H or any other Advantech products, please visit our support website at:

• **http://support.advantech.com.tw**

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CHAPTER **1**

Introduction

1.1　General Information

The MIC-3401/MIC-3401H is a 3U-sized general-purpose backplane that provides eight 32-bit or 64-bit (optional) CompactPCI slots. It accepts a 2-slot (8TE) or 3-slot (12TE) wide processor module and seven peripheral modules.

In order to provide users with a flexible system configuration, the MIC-3401/MIC-3401H includes one standard ATX power connector and an optional two IEC 603-2 (DIN 41612) connectors to accept one ATX power supply or two 3U size plug-in power modules.

The MIC-3401/MIC-3401H provides a 6-pin connector for connecting to up to 4 cooling fans. A 20-pin connector can be used for connecting an external alarm module (MIC-3920/MIC-3921) to detect system internal conditions, such as bus voltages and fan speed.

The MIC-3401H complies with PICMG 2.1 Hot-Swap Specification providing full hot-swapping capability. Users can build a hot-swap system using hot-swap plug-in boards and software.

1.2 Features

- Eight 32-bit CompactPCI slots (64-bit upon request)
- Supports hot-swappable modules (MIC-3401H)
- Accepts one ATX power supply or two plug-in power modules

  (optional, upon request)
- Alarm board interface
- Fan interface

1.3 Specification

- 8 CompactPCI slots (one system slot and 7 peripheral slots)
- Bus width: 32-bit (64-bit upon request)
- 8-layer PCB, 3.0 mm thick
- Separate power and ground planes
- Power connectors:
  - ➢ One ATX power connector for connecting standard ATX power supply
  - ➢ Screw terminals (on rear side) for external power inputs
  - ➢ Two IEC 603-2(DIN 41612) power connectors for two 2-slot wide plug-in power modules. (the connectors are upon reguest)
- 20-pin connector for MIC-3920/MIC-3921 alarm board signals
- Complies with CompactPCI Specification PICMG 2.0, Ver.2.1
- Complies with CompactPCI Hot Swap Specification PICMG 2.1, Ver.1.0 (MIC-3451H)
- V I/O Voltage: 3.3 V or 5 V, jumper selectable
- Supports PXI star trigger signals (optional)
- Logic Ground and Chassis Ground can be isolated or common
- Dimensions: 262.8 x 128.6 mm
- Operating temperature: -40 ~ 80°C (-40 ~ 176°F)

CHAPTER **2**

Hardware Configuration

2.1 Connector Locations
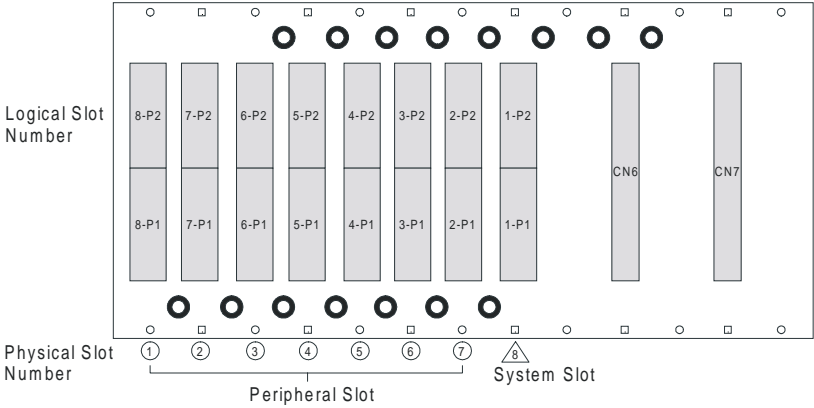
Figure 2-1. The connector locations on the front side
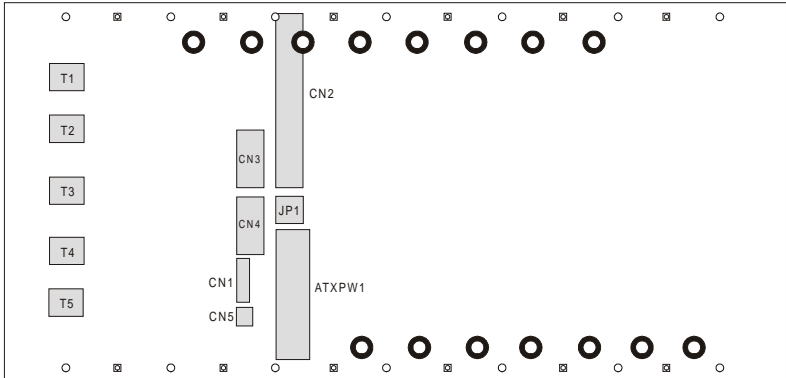
Figure 2-2. The connector locations on the rear side

Table 2-1. Connector Assignments

Name	Function
Slot 8	System Slot Connector
Slot 1~7	Peripheral Slot Connectors
CN2	Alarm Board Interface Connector
CN1	Fan Module Connector
CN6 and CN7	Plug-in Power Module Connectors
CN5	Power Switch Connector
CN3 and CN4	Peripheral Power Connectors
JP1	V I/O Voltage Selection Jumper
ATXPW1	ATX Power Connector
T1~T5	Power Inlet and Ground Screw Terminals

2.2 Slot Assignments

The CompactPCI specification defines slot numbering seperating for physical and logical slots. Each slot has a physical number and a logical number (refer to the CompactPCI specification version 2.0 R2.1 for further information on slot assignments). The physical numbers are printed on the backplane, enclosed in circles or triangles, below each slot. Slot 8, marked by a triangle, is the system slot and can only be used by a processor module. The other slots (slot 1~7) are peripheral slots and can be used by peripheral modules.

The logical number of each slot is defined according to the IDSEL signal and the associated address used to select the slot. Table 2-2 shows the system slot to peripheral slot relationships on the MIC-3401/MIC-3401H. Physical slot 8 (system slot) has a logical number 1, physical slot 7 has a logical number 2, physical slot 6 has a logical number 3, ..., and physical slot 1 has a logical number 8. The connectors in logical slot 1 are designated as 1-P1 and 1-P2. Nomenclature for connectors in other slots is similar, such as 2-P1, 2-P2, 3-P1, 3-P2, etc.

Connector 1-P1 is a keyed connector providing 32-bit CompactPCI busing between the system slot and the peripheral slots (2-P1~8-P1). Connector 1-P2 is an un-keyed connector providing 64-bit Compact-PCI busing between the system slot and the peripheral slots (2-P2~8-P2).

**Table 2-2. System to Peripheral Slot Signal Assignment**

Signal	Connector: Pin	Signal	Connector: Pin
System Slot 8, (Logical Slot 1):		Peripheral Slot 7, (Logical slot 2)	
CLK1	P2:A1	CLK	P1:D6
AD31	P1:E6	IDSEL	P1:B9
REQ0#	P1:A6	REQ#	P1:A6
GNT0#	P1:E5	GNT#	P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 6, (Logical slot 3)	
*CLK1(CLK6)	*P2:A1(P2:A21)	CLK	P1:D6
AD30	P1:A7	IDSEL	P1:B9
REQ1#	P2:C1	REQ#	P1:A6
GNT1#	P2:D1	GNT#	P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 5, (Logical slot 4)	
CLK0	P1:D6	CLK	P1:D6
AD29	P1:B7	IDSEL	P1:B9
REQ2#	P2:E1	REQ#	P1:A6
GNT2#	P2:D2	GNT#	P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 4, (Logical slot 5)	
*CLK0 (CLK5)	*P1:D6 (P2:A20)	CLK	P1:D6
AD28	P1:C7	IDSEL	P1:B9
REQ3#	P2:E2	REQ#	P1:A6
GNT3#	P2:C3	GNT#	P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 3, (Logical slot 6)	
CLK2	P2:A2	CLK	P1:D6
AD27	P1:E7	IDSEL	P1:B9
REQ4#	P2:D3	REQ#	P1:A6
GNT4#	P2:E3	GNT#	P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 2, (Logical slot 7)	
CLK3	P2:B2	CLK	P1:D6
AD26	P1:A8	IDSEL	P1:B9
REQ5#	P2:D15	REQ#	P1:A6
GNT5#	P2:E15	GNT#	P1:E5
System Slot 8, (Logical Slot 1):		Peripheral Slot 1, (Logical slot 8)	
CLK4	P2:A3	CLK	P1:D6
AD25	P1:D8	IDSEL	P1:B9
REQ6#	P2:D17	REQ#	P1:A6
GNT6#	P2:E17	GNT#	P1:E5

* MIC-3401H clock definitions and pin locations are in the parentheses. Please refer to section 2.7 Clock Routing Configuration.

Table 2-3. Connector Pin Assignments of P1 and P2 (System Slot)

Pin	Z	A	B	C	D	E	F	
22	GND	GA4	GA3	GA2	GA1	GA0	GND	
21	GND	CLK6	GND	RSV	RSV	RSV	GND	
20	GND	CLK5	GND	RSV	GND	RSV	GND	
19	GND	GND	RSV	RSV	RSV	RSV	GND	
18	GND	*PXI_TRIG3	*PXI_TRIG4	*PXI_TRIG5	GND	*PXI_TRIG6	GND	P2
17	GND	*PXI_TRIG2	GND	PRST#	REQ6#	GNT6#	GND	/
16	GND	*PXI_TRIG1	*PXI_TRIG0	DEG#	GND	*PXI_TRIG7	GND	J2
15	GND	*PXI_BRSVA15	GND	FAL#	REQ5#	GNT5#	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	C
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	O
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	N
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	N
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	E
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	C
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	T
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	O
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	R
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	*PXI_BRSVB4	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND	
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	P1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	/
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	J1
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	C
12-14				KEY AREA				O
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	N
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	E
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	C
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	T
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	O
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	R
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z	A	B	C	D	E	F	

� = long pins   □ = short pins   □ = medium length pins

*: Optional signals for PXI® star trigger signals

#: Low active

Note: GA[4...0] shall be used for geographic addressing on the backplane

Table 2-4. Connector Pin Assignments of P1 and P2 (Peripheral Slot)

Pin	Z	A	B	C	D	E	F	
22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2 / J2 CONNECTOR
21	GND	*PXI_LBR0	GND	*PXI_LBR1	*PXI_LBR2	*PXI_LBR3	GND	
20	GND	*PXI_LBR4	*PXI_LBR5	*PXI_LBR0	GND	*PXI_LBR1	GND	
19	GND	*PXI_LBL2	GND	*PXI_LBL3	*PXI_LBL4	*PXI_LBL5	GND	
18	GND	*PXI_TRIG3	*PXI_TRIG4	*PXI_TRIG5	GND	*PXI_TRIG6	GND	
17	GND	*PXI_TRIG2	GND	PRST#	*PXI_STAR	*PXI_CLK10	GND	
16	GND	*PXI_TRIG1	*PXI_TRIG0	DEG#	GND	*PXI_TRIG7	GND	
15	GND	*PXI_BRSVA15	GND	FAL#	*PXI_LBL6	*PXI_LBR6	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	*PXI_BRSVB4	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	*PXI_LBR7	GND	*PXI_LBR8	*PXI_LBR9	*PXI_LBR10	GND	
2	GND	*PXI_LBR11	*PXI_LBR12	SYSEN#	*PXI_LBL7	*PXI_LBL8	GND	
1	GND	*PXI_LBL9	GND	*PXI_LBL10	*PXI_LBL11	*PXI_LBL12	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1 / J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	
12-14				KEY AREA				
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z	A	B	C	D	E	F	

▒ = long pins   ▭ = short pins   ▢ = medium length pins

*: Optional signals for PXI® star trigger signals

#: Low active

Note: GA[4...0] shall be used for geographic addressing on the backplane

2.3 Alarm Board Interface (CN2)

The 20-pin connector CN2 is an interface for an external monitoring and alarm module, such as MIC-3920/MIC-3921, which monitors the system conditions. It contains bus voltages 3.3V, 5V, 12V and -12V, and utilizes four fan tachometer signals and an on-off control signal.

Table 2-5. CN2 Connector Pin Assignments

	Pin Assignment
20	FAN2
19	FAN1
18	FAN4
17	FAN3
16	N/C
15	POWER_FAIL#
14	N/C
13	N/C
12	N/C
11	N/C
10	N/C
9	PSON#
8	GND
7	GND
6	PRST#
5	+12V
4	-12V
3	+3.3V
2	+5V
1	+5V
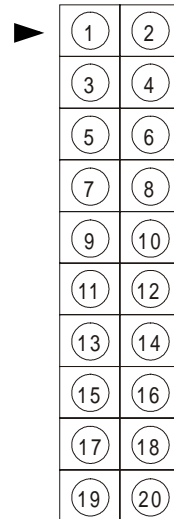
CN2 Connector Pin Locations

#: Low active

2.4 Fan Module Connector (CN1)

The CN1 connector provides +12 V power for fan operation and accepts the tachometer output from the fans. It accepts up to four fan signals.

Table 2-6. CN1 Connector Pin Assignments

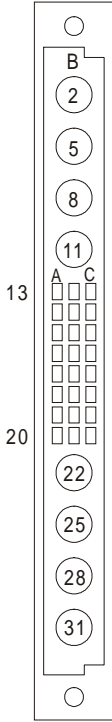|	Pin Assignment
6	+12V
5	GND
4	FAN1
3	FAN2
2	FAN3
1	FAN4

2.5 Power Connectors

2.5.1 Plug-in Power Module Connectors (CN6 and CN7)(optional, upon request)

The CN6 and CN7 connectors accept two redundant, 3U high, 2-slot (8TE) wide power modules.

Upon customers request, two connectors can be mounted on CN6 and CN7 .

Table 2-7. Power Module Connector

	Name
Column A	
A13	SP
A14	INH#
A15	ISH
A16	5S-
A17	5S+
A18	3.3V
A19	+12V
A20	-12V
Column B	
B2	ACL
B5	ACN
B8	-
B11	CG
B13	3.3V
B14	3.3V
B15	3.3V
B16	3.3V
B17	3.3V
B18	3.3V
B19	+12V
B20	-12V
B22	5V
B25	GND
B28	+DC
B31	-DC
Column C	
C13	EN#
C14	DEG#
C15	FAL#
C16	3.3V
C17	3.3V
C18	3.3V
C19	+12V
C20	-12V

**Power Module Connector
Pin Locations**

Note: Pin numbers illustrated are of the female backplane connector

2.5.2 ATX Power Connector (ATXPW1)

This connector accepts one standard ATX power supply.

Note: Do not use ATX power supplies and plug-in power modules at the same time.

2.5.3 Power Connectors for Peripherals (CN3 and CN4)

The CN3 and CN4 connectors provide power to the peripherals, such as hard disk drives or floppy disk drives.

2.5.4 Power Inlet and Ground Screw Terminals (T1~T5)

These screw terminals accept AC or DC power input. T1 ~ T5 provides power to CN6 and CN7. Depending on the input requirement (AC or DC) of the plug-in power modules intended for CN6 and CN7, connect either AC or DC source power.

2.5.5 V I/O Voltage Selection (JP1)

This jumper is used to select the V I/O voltage. MIC-3401/ MIC-3401H allows V I/O to be set to either 5 V or 3.3 V. Connect the two pins labeled "+5 V" with a cap to set V I/O to 5 V, and connect the two pins labeled "+3.3 V" with a cap to set V I/O to 3.3 V. Since the MIC-3401/MIC-3401H default is configured for use with 5 V CompactPCI boards (blue keyed connectors), once the jumper is set to 3.3 V, the CompactPCI keys must be changed to 3.3 V at the same time (as yellow keyed connectors). Please contact Advantech for detail.

2.5.6 Power Switch (CN5)

This connector provides power on/off control of the ATX power supply or the plug-in power module.

2.5.7 Screw terminal for external power supply

Along the upper and lower edges of the MIC-3401/MIC-3401H are 15 power pads providing external power supply I/O. Pads S1~S15 facilitate input or output of the different powers and grounds. Contact Advantech for installation help.
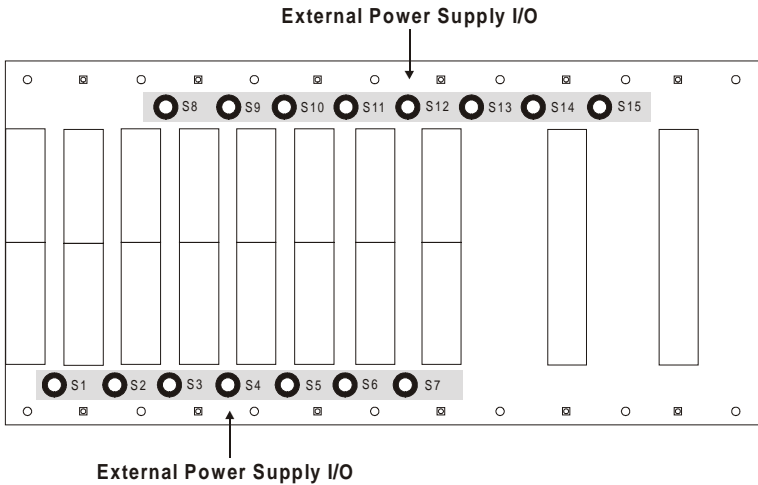

Figure 2-3 External Power Supply Terminal

Table 2-8. External Power Supply Terminal

	Name
S15	GND
S14	VCC
S13	GND
S12	VCC3
S11	GND
S10	VCC3
S9	GND
S8	CHS_GND
S7	CHS_GND
S6	+12V
S5	-12V
S4	VCC
S3	GND
S2	VCC
S1	GND

2.6 Ground Configuration

Along the top and bottom of the MIC-3401/MIC-3401H are 26 mounting holes. The holes are arranged in an alternating pattern of chassis (frame) grounded pads and logic grounded pads. The square pad holes are connected to chassis ground, and the round pad holes are connected to logic ground. To isolate chassis and logic grounds, install mounting screws in only square pad mounting holes.
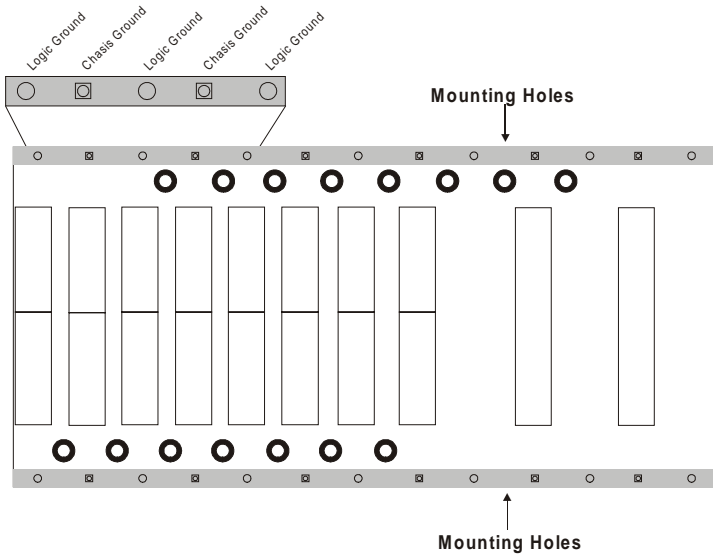
Figure 2-4. Mounting Holes Illustration

2.7 Clock Routing Configuration

Depending on the configuration option ordered (MIC-3401 or MIC-3401H), the backplane is compatible with individual clock CPUs or shared clock CPUs. The MIC-3401H is configured to comply with the clock routing specified in the CompactPCI Hot Swap Specification, PICMG 2.1, version 1.0. This Specification requires that each slot be independently clocked. By removing several 0 Ω resistors, the clock routing can be reconfigured to comply with the earlier CompactPCI Specification, PICMG 2.0, version 2.1. Reconfiguring the backplane to comply with this earlier specification allows the MIC-3401 to be backward compatible with CPUs using shared clocks.
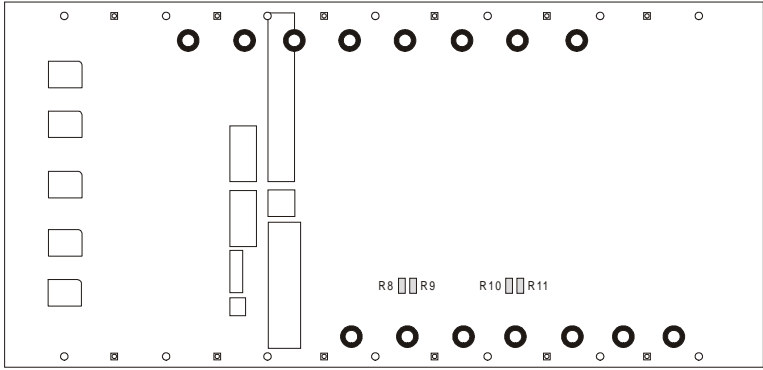
Individual Clock CPUs (MIC-3401H)
  Installed: R9, R11
  Not Installed: R8, R10

Shared Clock CPUs (MIC-3401)
  Installed: R8, R10
  Not Installed: R9, R11

Figure 2-5. Configuration Resistors Locations