EVA-X1610C

FAST ETHERNET RISC PROCESSOR

CONTENTS

1. Features 7

2. Block Diagram 8

3. Pin Description 9

3.1 PIN Placement 9
3.2 Functional Description 10
3.3 PIN Capacitance Description 16
3.4 PIN Pull-up/Pull-down Description 16

4. Oscillator Characteristics 18

4.1 Fundamental Mode 18
4.2 Third-Overtone Mode 18

5. Clock Unit 19

6. Execution UNIT 20

6.1 General Registers 20
6.2 Segment Registers 20
6.3 Instruction Pointer and Status Flags Registers 21
6.4 Address Generation 22

7. Peripheral Register List 24

7.1 Legacy Peripheral Registers (Base Address FF00h) 24
7.2 16550 UART Register Definitions (Base Address FF00h) 25
7.3 SDRAM Control Registers (Base Address FE00h) 25
7.4 Fast Ethernet MAC Control Registers (Base Address: MAC1 / FE00h) 25

8. Peripheral Control Block Registers 27

9. Reset 29

9.1 Power-up reset 29

10. Bus Interface UNIT 31

10.1 Slow Bus and Memory Shadow 31
10.2 Memory and I/O Interface 33
10.3 Data Bus....34
10.4 Wait States 35
10.5 Bus Width 36

11. Chip Select UNIT....37

11.1 UCS_n....37
11.2 LCS_n (Internal Signal)....38
11.3 PCSx_n 39

12. Refresh Control UNIT 41

13. Interrupt Controller UNIT 42

13.1 Master Mode and Slave Mode....43
13.2 Interrupt Vector, Type and Priority 44
13.3 Interrupt Requests....45
13.4 Interrupt Acknowledge 45
13.5 Programming the Registers....46

14. DMA UNIT 61

14.1 DMA Operation 61
14.2 External Requests 67
14.3 Serial Port/DMA Transfer....69

15. Timer Control UNIT....70

15.1 Timer/Counter Unit Output Mode 75
15.2 Watchdog Timer....75

16. 16550 UART Serial Port....78

16.1 Receiver Buffer Register and Transmitter Holding Register....79
16.2 Divisor Latch LS and MS Register....80
16.3 Interrupt Enable Register....81
16.4 Interrupt Identification Register 81
16.5 FIFO Control Register....83
16.6 Line Control Register 84
16.7 Modem Control Register 85

16.8 Line Status Register 86
16.9 Modem Status Register 88
16.10 Scratchpad Register 89
16.11 Programmable Baud Generator 89
16.12 FIFO Interrupt Mode Operation 90
16.13 FIFO Polled Mode Operation 91

17. PIO UNIT 92

17.1 PIO Multi-Functional Pins List Table 92

18. SDRAM Controller 96

18.1 SDRAM Arbiter Control Register 96
18.2 SDRAM Mode Set Register 97
18.3 SDRAM Control Register 98
18.4 SDRAM Timing Parameter Register 99

19. Fast Ethernet Controller 100

19.1 RX Descriptor Format 100
19.2 TX Descriptor Format 102
19.3 MCR0: MAC Control Register 0 (00h) 103
19.4 MCR1: MAC Control Register 1 (04h) 104
19.5 MBCR: MAC Bus Control Register (08h) 105
19.6 MTICR: TX Interrupt Control Register (0Ch) 106
19.7 MRICR: RX Interrupt Control Register (10h) 106
19.8 MTPR: TX Poll Command Register (14h) 107
19.9 MRBSR: RX Buffer Size Register (18h) 107
19.10 MRDCR: RX Descriptor Control Register (1Ah) 108
19.11 MLSR: MAC Last Status Register(1Ch) 108
19.12 MMDIO: MDIO Control Register (20h) 109
19.13 MMRD: MDIO Read Data Register (24h) 110
19.14 MMWD: MDIO Write Data Register (28h) 110
19.15 MTDSA0: TX Descriptor Start Address 0 (2Ch) 110
19.16 MTDSA1: TX Descriptor Start Address 1 (30h) 111
19.17 MRDSA0: RX Descriptor Start Address 0 (34h) 111
19.18 MRDSA1: RX Descriptor Start Address 1 (38h) 112
19.19 MISR: INT Status Register (3Ch) 112
19.20 MIER: INT Enable Register (40h) 113

19.21 MECISR: Event Counter INT Status Register(44h) 113
19.22 MECIER: Event Counter INT Enable Register (48h) 114
19.23 MRCNT: Successfully Received Packet Counter (50h) 115
19.24 MECNT0: Event Counter 0 (52H) 115
19.25 MECNT1: Event Counter 1 (54h) 116
19.26 MECNT2: Event Counter 2 (56h) 116
19.27 MCENT3: Event Counter 3 (58h) 116
19.28 MTCNT: Successfully Transmit Packet Counter (5Ah) 117
19.29 MCENT4: Event Counter 4 (5Ch) 117
19.30 MPCNT: Pause Frame Counter (5Eh) 118
19.31 MAR0 ~3: Hash Table Word 0 ~3 (60h, 62h, 64h, 66h) 118
19.32 MID0 (68h, 6Ah, 6Ch) 120
19.33 MID1 (70h, 72h, 74h) 121
19.34 MID2 (78h, 7Ah, 7Ch) 122
19.35 MID3 (80h, 82h, 84h) 123
19.36 MTSCF: The Configure of Test Mode (ACh) 124
19.37 MTSCR: The Control of Test Mode (AEh) 124
19.38 MTSTF: The TX FIFO RD/WR Data (B0h) 125
19.39 MTSRF: The RX FIFO RD/WR Data (B2h) 125
19.40 MTSRS: The RX Status in Test Mode (B4h) 126

20. DC Electrical Characteristics 127

20.1 Absolute Maximum Ratings (25°C) 127
20.2 Operating Temperature 127

21. AC Electrical Characteristics 128

21.1 Alphabetical Key to Switching Parameter Symbols 128
21.2 Numerical Key to Switching Parameter Symbols 128
21.3 CPU Bus 129
21.4 SDRAM Bus 133
21.5 CPU Reset 135
21.6 MDC/MDIO Timing 136
21.7 TX Transmit Timing Parameters 137
21.8 TX Transmit Timing Diagram 137
21.9 RX Receive Timing Parameters 137
21.10 RX Receive Timing Diagram 137

22. Instruction Set OP-Code and Clock Cycles 138

23. EVA-X1610C Execution Timing.....142

24. Package Information 143

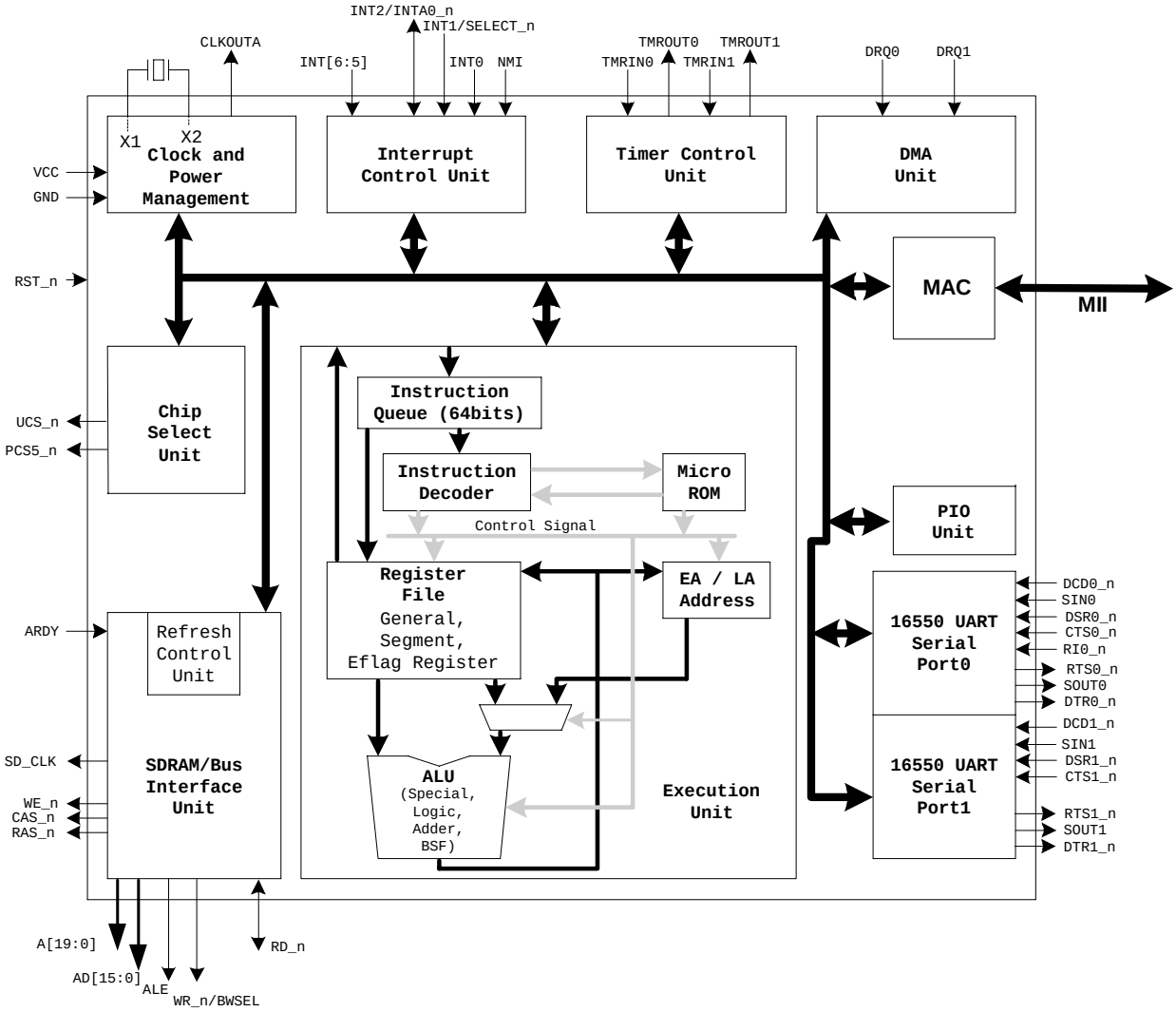
24.1 PQFP 128 pins 143

25. Revision History 144

1. Features

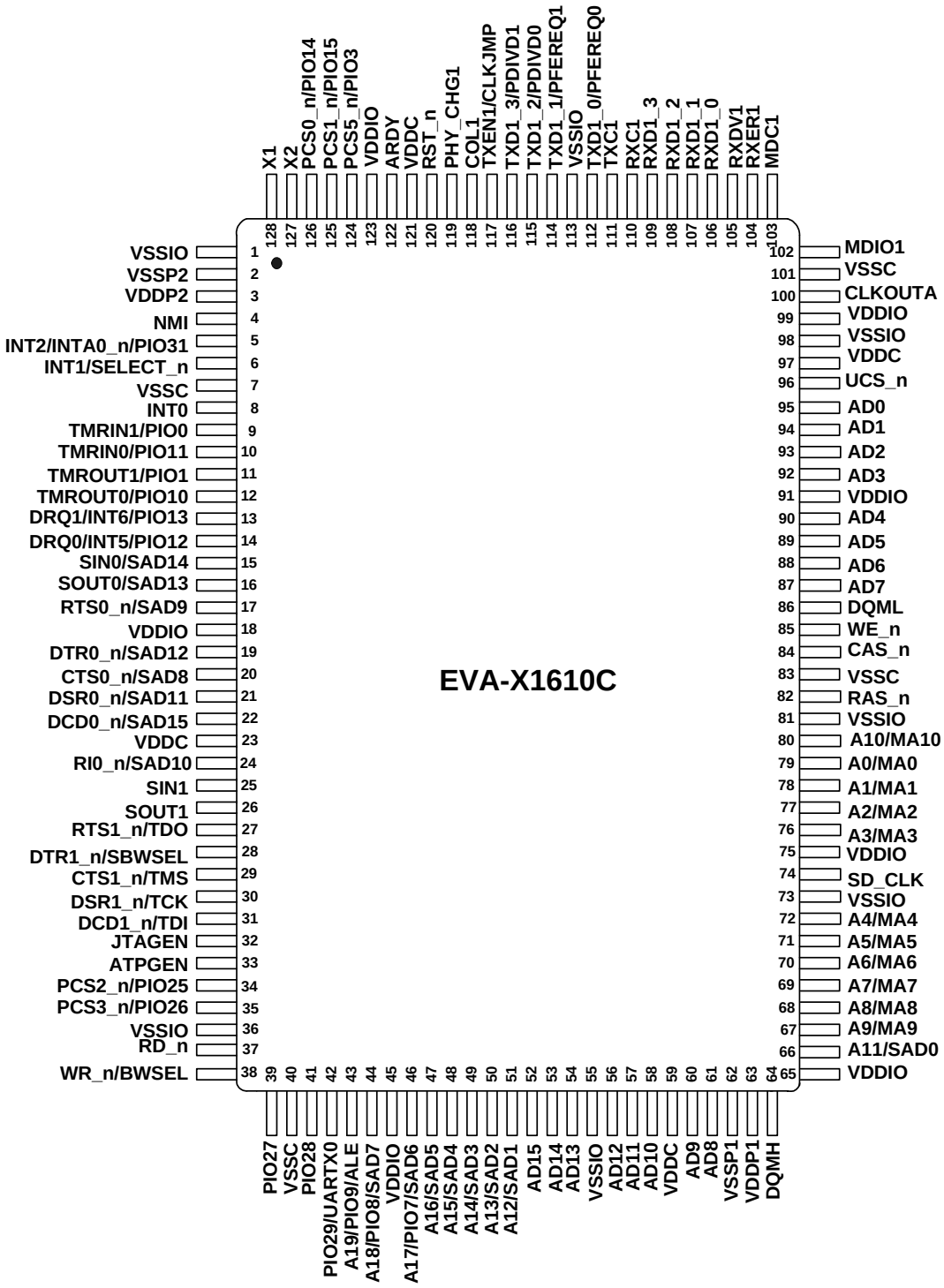
- Five-stage pipeline
- RISC architecture
- Bus interface
  - Multiplexed address and Data bus
  - Supports nonmultiplexed address bus A [19:0]
  - 8-bit or 16-bit external bus dynamic access
  - 1M-byte memory address space
  - 64K-byte I/O space
  - Supports an independent bus for slower I/O device
- Software is compatible with the 80C186 microprocessor
- Supports two 16550 UART serial channel with 16 bytes FIFO.
- Supports CPU ID
- Supports 18 PIO pins
- SDRAM control Interface
- Three independent 16-bit timers and one independent programmable watchdog timer
- The Interrupt controller with five maskable external interrupts and one non-maskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable wait-state generator
- With 8-bit or 16-bit Boot ROM bus size
- 1-Port Fast Ethernet MAC with MII interface
- With 25MHz input frequency and up to 4x25MHz maximum internal frequency.
- Compatible with 3.3V I/O.
- With 128-pin PQFP package type.

2. Block Diagram



3. Pin Description

3.1 PIN Placement



3.2 Functional Description

I = Input;

O = Output;

PU = Pull up 75KΩ;

PD = Pull down 75KΩ;

PU* = Pull up 75KΩ when the PIOn pin is used;

PD* = Pull down 75KΩ when the PIOn pin is used;

● CPU Core

PIN No.	Symbol	Type	Description
120	RST_n	I//PU	Reset input with Schimit Trigger. When RST_n is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and changes the address to the reset address FFFF0h.
128	X1	I	25MHz frequency input, within 100ppm tolerance, to the amplifier (oscillator).
127	X2	O	Frequency output from the inverting amplifier (oscillator).
100	CLKOUTA	O	The CLKOUTA output frequency is the same as the X1 input frequency. When high, the CLKOUTA is from Multiple-PLL. When low, the CLKOUTA is from X1.

Bus Interface			
PIN No.	**Symbol**	**Type**	**Description**
37	RD_n	O	Read Strobe. One active low signal indicates that the micro-controller is performing a memory or I/O read cycle. The RD_n floats during a bus hold or reset.
38	WR_n/BWSEL	O/PU	Write strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. WR_n is active during T2, T3, and Tw of any write cycle, floating during a bus hold or reset. BWSEL is used to decide the boot ROM bus width when RST_n goes from low to high. If BWSEL is with an external pull-low resistor (4.7k ohm), the boot ROM bus width is 8 bits. Otherwise the boot ROM bus width is 16 bits.
122	ARDY	I/PU	Asynchronous ready. This pin indicates to the micro-controller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge of input that is asynchronous to SD_CLK and is active high. However, the falling edge of ARDY must be synchronized to SD_CLK. Tie ARDY high, so the micro-controller is always asserted in the ready condition. Please note that the ARDY signal is internally pulled high.
43 44 46 47	A19/PIO9/ALE A18/PIO8/SAD7 A17/ PIO7/SAD6 A16/SAD5	O/I	Address bus. Non-multiplexed memory or I/O addresses. The address bus is one-half of a SD_CLK period earlier than the AD bus. The address bus is in a high-impedance state during a bus hold or reset.

48 49 50 51 66 80 67 68 69 70 71 72 76 77 78 79	A15/SAD4 A14/SAD3 A13/SAD2 A12/SAD1 A11/SAD0 A10/MA10 A9/MA9 A8/MA8 A7/MA7 A6/MA6 A5/MA5 A4MA4 A3/MA3 A2/MA2 A1/MA1 A0/MA0		SAD [7:0]: The combination pins with addresses and data. They are designed for slower peripheral bus. ALE: Address latch enable. Active high. This pin indicates an address output on the AD bus. Address is guaranteed to be valid on the trailing edge of ALE. MA [10:0]: The SDRAM raw and column address output.
95 94 93 92 90 89 88 87 61 60 58 57 56 54 53 52	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15	I/O	The multiplexed address and data bus for memory or I/O access. The address is present during the t1 clock phase, and the data bus phase is in t2-t4 cycle. The address phase of the AD bus can be disabled. See the description for WLB_n/ADEN_n. The AD bus is in a floating state during a bus hold or reset condition and this bus can also be used to load system configuration information (with pull-up or pull-low resistors) into the RESCON register when RST_n goes from low to high and the Watchdog timeout is reset.

Chip Select Unit Interface

PIN No.	Symbol	Type	Description
96	UCS_n	I/O/PU	Upper memory chip select/ONCE mode request 1. For UCS_n, this pin is active low when the system accesses the defined portion of the upper 512K bytes (80000h-FFFFFh) memory block. UCS_n defaulted active address region is from F0000h to FFFFFh after power-on reset. The address range for UCS_n is programmed by software.
124	PCS5_n/ PIO3	I/O/PU*	Peripheral chip selects/latched address bit. For PCS_n feature, these pins are active low when the microcontroller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address for PCS_n is programmable. These pins assert with the multiplexed AD address bus and do not float during bus hold conditions.
125 126	PCS1_n/PIO15 PCS0_n/PIO14	I/O/PU*	Peripheral chip selects. These pins are active low when the micro-controller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 1M-Byte memory address region. These pins assert with the

			multiplexed AD address bus and do not float during bus holds.
34 35	PCS2_n/PIO25 PCS3_n/PIO26	I/O/PU*	Peripheral chip selects. These pins are active low when the microcontroller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 1M-Byte memory address region. These pins assert with the multiplexed AD address bus and do not float during bus holds.
Interrupt Control Unit Interface			
PIN No.	**Symbol**	**Type**	**Description**
4	NMI	I/PD	Nonmaskable Interrupt. The NMI is the highest priority hardware interrupt and is nonmaskable. When this pin is asserted (NMI transition from low to high), the micro-controller always transfers the address bus to the location specified by the nonmaskable interrupt vector in the micro-controller interrupt vector table. The NMI pin must be asserted for at least one SD_CLK period to guarantee that the interrupt is recognized.
5	INT2/INTA0_n/PIO31	I/O/PU*	Maskable Interrupt Request 2/Interrupt Acknowledge 0. For INT2, it's active high. The interrupt input can be configured as either edge-triggered or level-triggered. The requesting device must hold the INT2 until the request is acknowledged to guarantee interrupt recognition.. For INTA0_n, in cascade mode or special fully-nested mode, this pin corresponds to the INT0.
6	INT1/SELECT_n	I/PD	Maskable Interrupt Request 1/slave select. For INT1, except the differences in the interrupt line and interrupt address vector, the function of INT1 is the same as that of INT2. For the SELECT_n feature, when the microcontroller is as a slave device, this pin is driven from the master interrupt controller decoding. This pin is activated to indicate that an interrupt appears on the address and data bus. The INT0 must be activated before the SELECT_n is activated when the interrupt type appears on the bus.
8	INT0	I/PD	Maskable interrupt request 0. Except the differences in the interrupt line and interrupt address vector, the function of INT0 is the same as that of INT2.
Timer Control Unit Interface			
PIN No.	**Symbol**	**Type**	**Description**
9 10	TMRIN1/PIO0 TMRIN0/PIO11	I/O/PU*	Timer input. These pins can be used as clock or control signal input, depending upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. **These pins must be pulled up if not being used.**
11 12	TMROUT1/PIO1 TMROUT0/PIO10	I/O/PD*	Timer output. Depending on timer mode select. These pins provide single pulse or continuous waveform. The duty cycle of the waveform is programmable. These pins float during a bus hold or reset.
DMA Unit Interface			
13 14	DRQ1/INT6/PIO13 DRQ0/INT5/PIO12	I/O/PU*	DMA request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals are not latched and must remain active until serviced.. For INT6/INT5: When the DMA function is not used, the INT6 and INT5 can be used as an additional external interrupt request.

			They share the corresponding interrupt type and register control bits. The INT6/5 are level-triggered only.

- **High Speed UART**

PIN No.	Symbol	Type	Description
15	SIN0/SAD14	I/O/PU	SIN0: Serial Input. Serial Data Input from the communications link. SAD14: The combination pin with Address and Data. It is for slower device bus.
16	SOUT0/SAD13	I/O/PU	SOUT0: Serial Output. Composite serial data output to the communications link. SAD13: The combination pin with Address and Data. It is for slower device bus.
17	RTS0_n/SAD9	I/O/PU	RTS0_n: Request To Send. When low, this indicates to MODEM or data set that URAT is ready to exchange data. SAD9: The combination pin with Address and Data. It is for slower device bus.
19	DTR0_n/SAD12	I/O/PU	DTR0_n: Data Terminal Ready. When low, this informs the MODEM or data set that UART is ready to establish a communication link. SAD12: The combination pin with Address and Data. It is for slower device bus.
20	CTS0_n/SAD8	I/O/PU	CTS0_n: Clear To Send. When low, this informs that MODEM or data set is ready to exchange data. SAD8: The combination pin with Address and Data. It is for slower device bus.
21	DSR0_n/SAD11	I/O/PU	DSR0_n: Data Set Ready. When low, this indicates that MODEM or data set is ready to establish the communication link with UART. SAD11: The combination pin with Address and Data. It is for slower device bus.
22	DCD0_n/SAD15	I/O/PU	DCD0_n: Data Carry Detection. When low, it indicates that the data carrier has been detected by the MODEM or data set. SAD15: The combination pin with Address and Data. It is for slower device bus.
24	RI0_n /SAD10	I/O/PU	RI0_n: Ring Indicator. This indicates that a telephone ringing signal has been received by the MODEM or data set. SAD10: The combination pin with Address and Data. It is for slower device bus.
25	SIN1	I	SIN1: Serial Data Input.
26	SOUT1	O/PU	SOUT1: Serial Data Output.
27	RTS1_n/TDO	O	RTS1_n: Request To Send. TDO: JTAG test data output pin.
28	DTR1_n/SBWSEL	I/O/PU	DTR1_n: Data Terminal Ready. SBWSEL is to decide the SAD bus width when the RST_n pin goes from low to high. If SBWSEL is with a pull-low resistor (4.7k ohm), the SAD bus width is 8 bits and 16550's Port 1 is active. Otherwise the SAD bus width is 16 bits and 16550 Port 1 is inactive.
29	CTS1_n/TMS	I/PU	CTS1_n: Clear To Send. JTAG Test mode select.
30	DSR1_n/TCK	I/PU	DSR1_n: Data Set Ready.

			TCK: JTAG test reset input.
31	DCD1_n/TDI	I/PU	DCD1_n: Carry Sense Detection. TDI: JTAG test data input port.

- **MII Interface**

PIN No.	Symbol	Type	Description
116 112 115 114	TXD1_3/PDIVD1 TXD1_0/PFEREQ0 TXD1_2/PDIVD0 TXD1_1/PFEREQ1	I/O/PU I/O/PD	Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal. PDIVD [1:0] & PFEREQ [1:0] are hardware configured pins during reset for Multiple PLL (see Chapter 5).
117	TXEN1/CLKJMP	I/PD	This pin functions as transmit enable. It indicates that a transmission to an external PHY device is active on the MII port. CLKJMP: It is a hardware configured pin, used to select the CLKOUTA output from internal Multiple PLL or X1. When high, the CLKOUTA is from Multiple PLL. When low, the CLKOUTA is from X1.
111	TXC1	I/PD	Supports the transmit clock supplied by the external PMD device. This clock should always be active.
110	RXC1	I/PD	Supports the receive clock supplied by the external PMD device. This clock should always be active.
109 108 107 106	RXD1_3 RXD1_2 RXD1_1 RXD1_0	I/PU* I/PD* I/PD	Four parallel receive data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
105	RXDV1	I/PD	Data valid is asserted by an external PHY when the received data is present on the RXD1 [3:0] lines and is de-asserted at the end of the packet.
104	RXER1	I/PD	Receiver error shall be asserted to indicate to MAC that an error was detected. This signal should be synchronized with the RXC signal.
118	COL1	I/PD	This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
103	MDC1	O	MII management data clock is sourced by the EVA-X1610C to the external PHY device as a timing reference for the transfer of information on the MDIO signal.
102	MDIO1	I/O/PD	MII management data input/output transfers control information and status between the external PHY and the EVA-X1610C.
119	PHY_CHG1	I/O/PD	To indicate that the PHY status has been changed.

- **JTAG /SCAN Chain Enable Pin**

PIN No.	Symbol	Type	Description
32	JTAGEN	I/PD	JTAGE function enable. Default is pulled low and disabled.
33	ATPGEN	I/PD	Scan chain functions enable. Default is pulled low and disabled.

- **SDRAM Interface**

PIN No.	Symbol	Type	Description
74	SD_CLK	O	SDRAM clock output. This clock output is from internal De-skew PLL. It can be one to four multiple of input clock X1, depending

			on the setting of PFEREQ [1:0] during power-on resets.
85	WE_n	O	SDRAM write enable.
84	CAS_n	O	SDRAM column address selector.
82	RAS_n	O	SDRAM raw address selector.
86	DQML	O	Input/Output mask.
64	DQMH	O	Input/Output mask.

● GPIO Interface

PIN No.	Symbol	Type	Description
39	PIO27	I/O/PU*	General purpose PIN.
41	PIO28	I/O/PU*	General purpose PIN.
42	PIO29/UARTX0	I/O/PD*	General purpose PIN. UARTX0: URAT0 transmission indication for observation.

● Power PINs

PIN No.	Symbol	Type	Description
18,45,65,75, 91,99,123	VDDIO	I	I/O power pin, pure 3.3V.
1,36,55,73, 81,98,113	VSSIO	I	I/O ground pin.
23,59,97, 121	VDDC	I	Core power pin, pure 3.3V.
7,40,83,101	VSSC	I	Core ground pin.
63	VDDP1	I	De-skew PLL power pin, pure 3.3V.
62	VSSP1	I	De-skew PLL ground pin.
3	VDDP2	I	Multiple PLL power pin, pure 3.3V.
2	VSSP2	I	Multiple PLL ground pin.

Notes:

1. When the PIO Data register is enabled, the 18 MUX definition pins can be used as a PIO pin. For example, the PCS0_n/PIO14 (Pin 126) can be used as a PIO14 when the PIO Data register is enabled.
2. The PIO status during Power-On reset:

   (1) PIO1 and PIO10 are inputs with pull-down resistors.

   (2) PIO7, PIO8 and PIO9 are normal operations.

   (3) Other PIOs are inputs with pull-up resistors.
3. In Slow Bus Mode (Bus Mode 0):

   I/O bus is mapped to SAD [15:0] or SAD [7:0]. It depends on the hardware setting of DTR1_n/SBWSEL Pin (Pin 28) during power-on reset to select 16-bit mode or 8-bit mode.

   Memory bus is mapped to A [10:0]/AD [15:0].
4. In Normal Bus Mode (Bus Mode 1):

I/O bus and Memory bus are all mapped to A [19:0] and AD [15:0]. The SAD [15:0] bus is inactive in this mode.

5. Change Bus Mode 0 and Bus Mode 1 by means of setting the internal Bus Control Register. This action must be initialized by software.
6. All pins are 3.3V.

3.3 PIN Capacitance Description

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance		2.8		pF
C_{OUT}	3.3V Output Capacitance	2.7		4.9	pF
C_{BID}	3.3V Bi-directional Capacitance	2.7		4.9	pF

3.4 PIN Pull-up/Pull-down Description

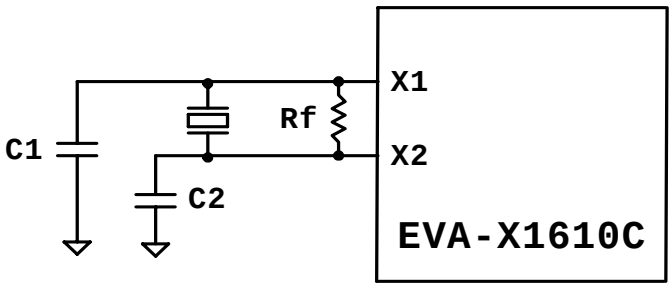
PIN Name	Pin No.	Pull-up	Pull-down	Schmitt Trigger	Description
RST_n ARDY	120 122	1	0	1	
NMI INT0 INT1/SELECT_n	4 8 6	0	1	0	
WR_n/BWSEL	38	1	0	0	
TMROUT0 TMROUT1 /PIO	12 11	0	PIO10 PIO1	0	When set in normal operation, these two pins are with neither pull-up nor pull-down resistors. However, when set in PIO, they are input with pull-down resistors.
UCS_n	96	1	0	1	
PIO27 PIO28	39 41	PIO27 PIO28	0	0	
PIO29/UARTX0	42	0	PIO29	0	
INT2/INTA0_n PCS0_n PCS1_n PCS2_n PCS3_n PCS5_n TMRIN0 TMRIN1 DRQ0/INT5 DRQ1/INT6 /PIO	5 126 125 34 35 124 10 9 14 13	PIO31 PIO14 PIO15 PIO25 PIO26 PIO3 PIO11 PIO0 PIO12 PIO13	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	When set in normal operation, these pins are with neither pull-up nor pull-down resistors. However, when set in PIO, they are input with pull-up, pull-down, or schimitt trigger as listed in the left table.

DCD0_n SIN0 SOUT0 DTR0_n DSR0_n RI0_n RTS0_n CTS0_n /SAD15-8	23 16 17 20 22 25 18 21	1	0	0	
SOUT1 DSR1_n/TCK DCD1_n/TDI CTS1_n/TMS	26 30 31 29	1	0	0	
DTR1_n /SBWSEL	28	1	0	0	
TXC1 RXC1	111 110	0	1	1	
RXD1_3 RXD1_2 RXD1_1 RXD1_0 RXDV1 RXER1 COL1	109 108 107 106 105 104 118	0	1	0	
TXD1_3/PDIVID1 TXD1_0/PFREQ0	116 112	1	0	0	
TXD1_2/PDIVID0 TXD1_1/PFREQ1 TXEN1/CLKJMP	115 114 117	0	1	0	
MDIO1	102	0	1	0	
JTAGEN ATPGEN	32 33	0	1	1	
PHY_CHG1	119	0	1	0	

Note: The pins never in the pull-up, pull-down, and schimitt trigger status are not shown in the above table

4. Oscillator Characteristics

4.1 Fundamental Mode



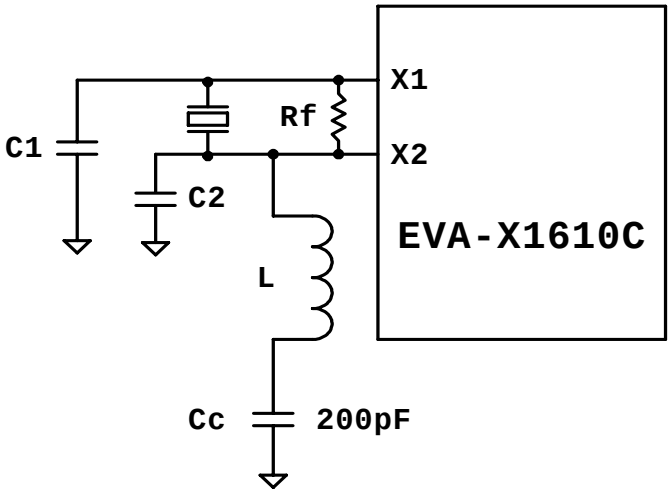
C1 ---------- 20pF ± 20%

C2 ---------- 20pF ± 20%

Rf ---------- 1 mega-ohm

4.2 Third-Overtone Mode

Normally, high frequency use for third overtone mode can get price advantage, but additional L and Cc are needed.



Typical value suggestions are as follows:

C1 ---------- 20pF ± 20%

C2 ---------- 20pF ± 20%

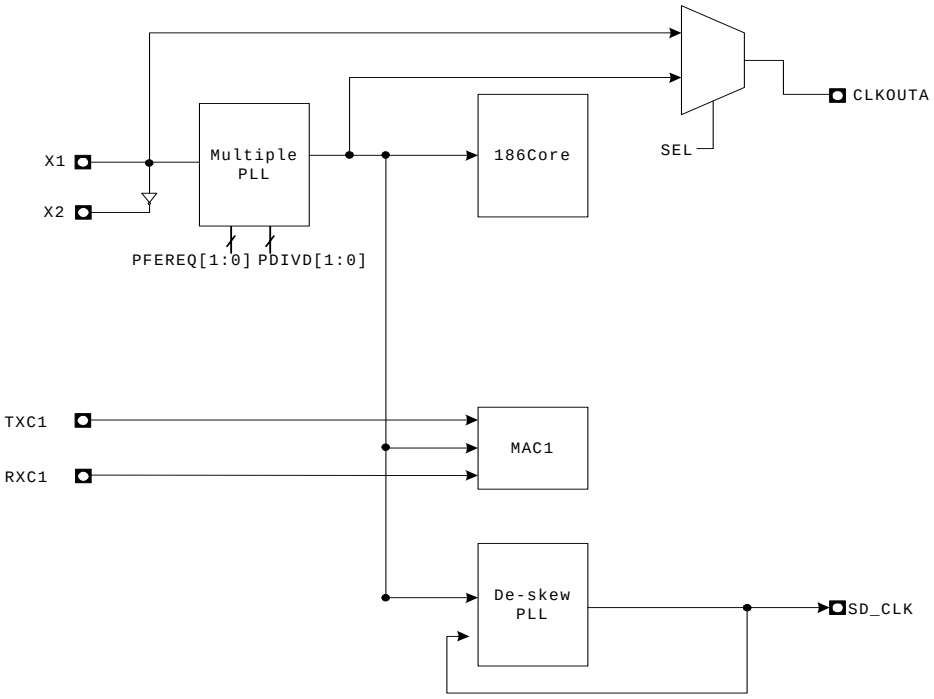
Cc ---------- 200pF± 20%

Rf ---------- 1 Mega-Ohm

L ---------- 4.7uH, 6.8uH, 8.2uH, 10uH (25MHz)

Note: X1 input clock must be within + - 100ppm tolerance.

5. Clock Unit



PLL Configuration Table:

Input Clock Range (Mhz)	PFEREQ[1:0]	PDIVD[1:0]		Multiple	Output Clock (Mhz)
16 - 20	00	0	0	1	16 – 20
		0	1	2	32 – 40
		1	0	3	46 –60
		1	1	4	64 –80
20.001 - 25	01	0	0	1	20 –25
		0	1	2	40 – 50
		1	0	3	60 – 75 (default)
		1	1	4	80 – 100
25.001 - 33	10	0	0	1	25 –33
		0	1	2	50 – 66
		1	0	3	75 - 99
		1	1	4	100 – 132
33.001 - 40	11	0	0	1	33 – 40
		0	1	2	66 – 80
		1	0	3	99 – 120
		1	1	4	132 - 160

For example: If input clock =25 Mhz , then set PFEREQ[1:0]=10b.

If PDIVD[1:0]=00b, then PLL output clock =25 Mhz

If PDIVD[1:0]=01b, then PLL output clock =50 Mhz

If PDIVD[1:0]=10b, then PLL output clock =75 Mhz

If PDIVD[1:0]=11b, then PLL output clock =100 Mhz

6. Execution UNIT

6.1 General Registers

The EVA-X1610C has eight 16-bit general registers. And the AX, BX, CX, and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH, and DL). The functions of these registers are described as follows:

AX: Word Divide, Word Multiply, Word I/O operation.

AH: Byte Divide, Byte Multiply, Byte I/O, Decimal Arithmetic, Translate operation.

AL: Byte Divide, Byte Multiply operation.

BX: Translate operation.

CX: Loops, String operation

CL: Variable Shift and Rotate operation.

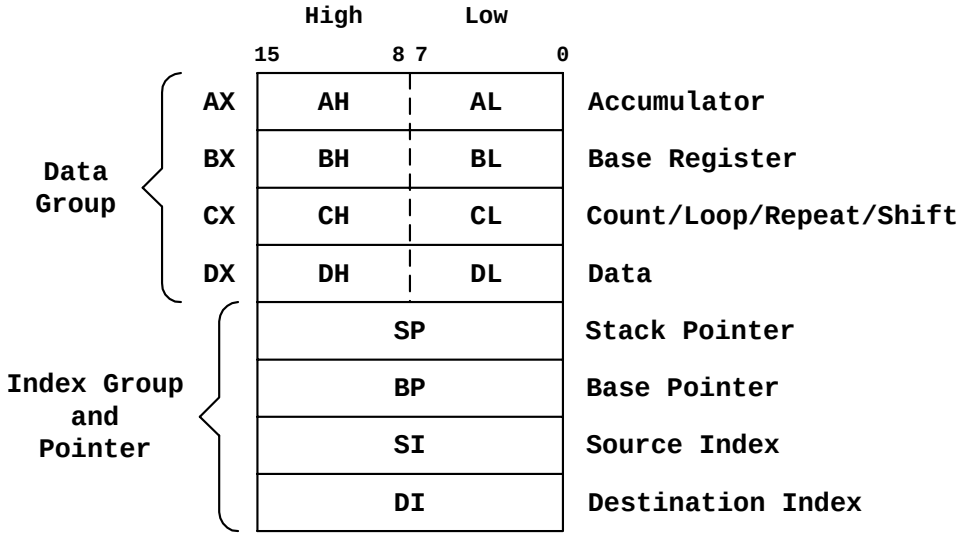
DX: Word Divide, Word Multiply, Indirect I/O operation

SP: Stack operations (POP, POPA, POPF, PUSH, PUSHA, PUSHF)

BP: General-purpose registers which can be used to determine offset address of operands in Memory.

SI: String operations

DI: String operations



GENERAL REGISTERS

6.2 Segment Registers

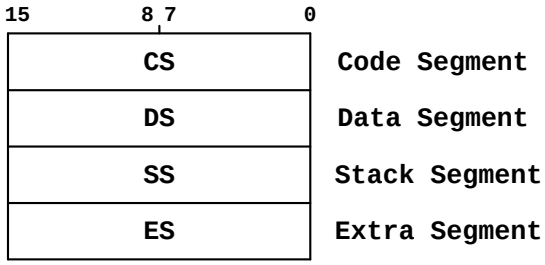
EVA-X1610C has four 16-bit segment registers: CS, DS, SS, and ES. The segment registers contain the base addresses (starting location) of these memory segments, and they are immediately addressable for code (CS), data (DS & ES), and stack (SS) memory.

CS (Code Segment): The CS register points to the current code segment, which contains instruction to be fetched. The default location memory space for all instructions is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment): The DS register points to the current data segment, which generally contains program variables. The DS register is initialized to 0000H.

SS (Stack Segment): The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000H.

ES (Extra Segment): The ES register points to the current extra segment, which is typically for data storage, such as large string operations and large data structures. The ES register is initialized to 0000H.



SEGMENT REGISTERS

6.3 Instruction Pointer and Status Flags Registers

IP (Instruction Pointer): The IP is a 16-bit register and it contains the offset of the next instruction to be fetched. The IP register cannot be directly accessed by software. This register is update by the bus interface unit. It can be changed, saved or restored as a result of program execution. The IP register is initialized to 0000H and the starting execution address for CS:IP is at 0FFFF0H.

Register Name: Processor Status Flags Register

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Rsvd	AF	Rsvd	PF	Rsvd	CF

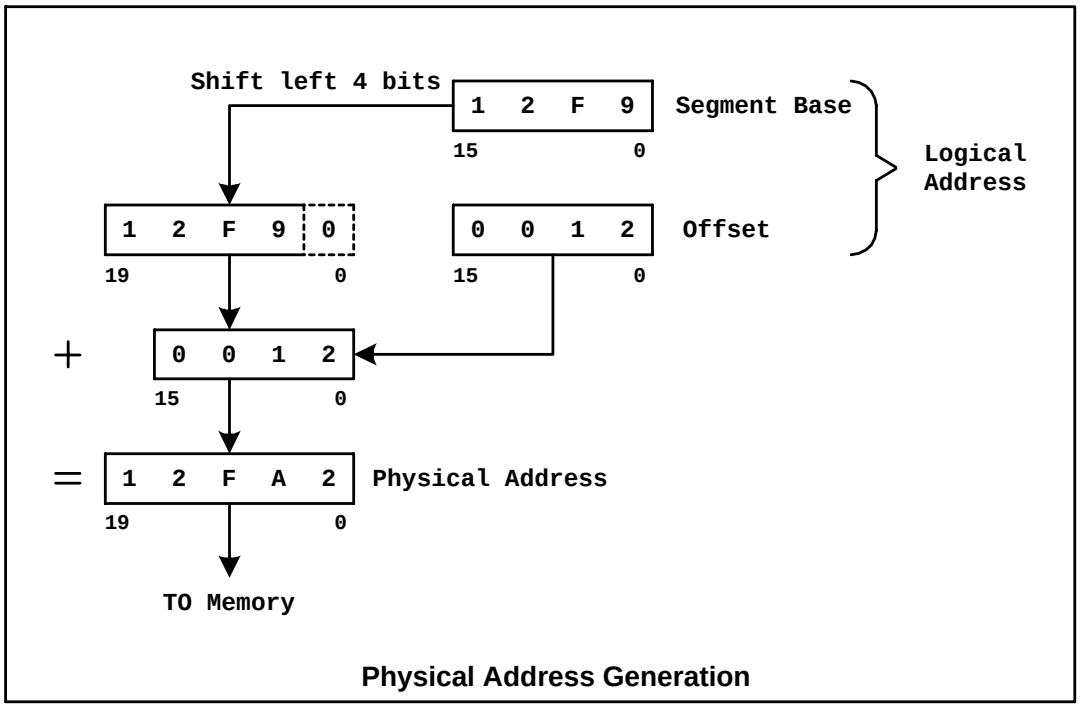
These flags reflect the status after the Execution Unit is executed.

Bit	Name	Description
15-12	Rsvd	Reserved.
11	OF	Overflow Flag. If an arithmetic overflow occurs, this flag will be set.
10	DF	Direction Flag. If this flag is set, the string instructions are in the process of incrementing address. If DF is cleared, the string instructions are in the process of decrementing address. Refer to the STD and CLD instructions for how to set and clear the DF flag.
9	IF	Interrupt-Enable Flag. Refer to the STI and CLI instructions for how to set and clear the IF flag.

		Set to 1: The CPU enables the maskable interrupt request. Set to 0: The CPU disables the maskable interrupt request.
8	TF	Trace Flag. Set to enable single-step mode for debugging; Clear to disable the single-step mode. If an application program sets the TF flag with POPF or IRET instruction, a debug exception is generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.
7	SF	Sign Flag. If this flag is set, the high-order bit of the result of an operation will be 1, indicating the state of being negative.
6	ZF	Zero Flag. If this flag is set, the result of operation will be zero.
5	Rsvd	Reserved
4	AF	Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low nibble of the AL general-purpose register. It is used in BCD operation.
3	Rsvd	Reserved
2	PF	This flag will be set if the result of the low-order 8 bits operation has even parity.
1	Rsvd	Reserved
0	CF	Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

6.4 Address Generation

The Execution Unit generates a 20-bit physical address to Bus Interface Unit by the Address Generation. Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



Physical Address Generation

7. Peripheral Register List

The Peripheral Control Block can be mapped into either Memory or I/O space by programming the Peripheral Control Block Relocation Register (FEh). After reset, the default Legacy Peripheral Control Block offset is located at FF00h in I/O space, the SDRAM Control Register is located at FE00h in I/O space, and Ethernet Control Register is located at FD00h and FE00h in I/O space.

The following table lists are all the definitions of the Peripheral Control Block Registers, and the detailed descriptions will be arranged on the related Block Unit.

7.1 Legacy Peripheral Registers (Base Address FF00h)

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	27	66	Timer 2 Mode/Control Register	74
F8	Processor Extended ID Register	28	62	Timer 2 Maxcount Compare A Register	75
F6	Reset Configuration Register	30	60	Timer 2 Count Register	75
F4	Processor Release Level Register	27	5E	Timer 1 Mode/Control Register	72
F2	Auxiliary configuration Register	36	5C	Timer 1 Maxcount Compare B Register	74
EA	Bus Control Register	33	5A	Timer 1 Maxcount Compare A Register	73
E6	Watchdog Timer Control Register	76	58	Timer 1 Count Register	73
E4	Enable RCU Register	41	56	Timer 0 Mode/Control Register	70
E2	Clock Prescaler Register	41	54	Timer 0 Maxcount Compare B Register	71
DA	DMA 1 Control Register	64	52	Timer 0 Maxcount Compare A Register	71
D8	DMA 1 Transfer Count Register	66	50	Timer 0 Count Register	71
D6	DMA 1 Destination Address High Register	66	44	Serial Port 0 interrupt control register	47
D4	DMA 1 Destination Address Low Register	66	42	Serial Port 1 interrupt control register	47
D2	DMA 1 Source Address High Register	67	40	MAC Interrupt Control Register	48
D0	DMA 1 Source Address Low Register	67	3C	INT2 Control Register	48
CA	DMA 0 Control Register	62	3A	INT1 Control Register	49
C8	DMA 0 Transfer Count Register	62	38	INT0 Control Register	50
C6	DMA 0 Destination Address High Register	63	36	DMA1/INT6 Interrupt Control Register	51
C4	DMA 0 Destination Address Low Register	63	34	DMA0/INT5 Interrupt Control Register	51
C2	DMA 0 Source Address High Register	63	32	Timer Interrupt Control Register	52
C0	DMA 0 Source Address Low Register	64	30	Interrupt Status Register	53
A8	Peripheral Chip Select Register 1	39	2E	Interrupt Request Register	53
A4	Peripheral Chip Select Register 0	38	2C	Interrupt In-service Register	55
A0	Upper Memory Chip Select Register	37	2A	Interrupt Priority Mask Register	56
88	(See 7.2)	25	28	Interrupt Mask Register	57
86	(See 7.2)	25	26	Interrupt Poll Status Register	58
84	(See 7.2)	25	24	Interrupt Poll Register	59
82	(See 7.2)	25	22	Interrupt End-of-Interrupt	59
80	(See 7.2)	25	20	Interrupt Vector Register	60
7A	PIO Data 1 Register	93	18	(See 7.2)	25
78	PIO Direction 1 Register	93	16	(See 7.2)	25
76	PIO Mode 1 Register	94	14	(See 7.2)	25

74	PIO Data 0 Register	94	12	(See 7.2)	25
72	PIO Direction 0 Register	94	10	(See 7.2)	25
70	PIO Mode 0 Register	95			

7.2 16550 UART Register Definitions (Base Address FF00h)

Offset (HEX)	Register Name	Mnemonic	Page
80h	UART0 Receiver Buffer Register (when DLAB=0 & Read)	**RBR0**	79
	UART0 Transmitter Holding Register (when DLAB=0 & Write)	**THR0**	80
	UART0 Divisor Latch [Low Byte] (when DLAB=1)	**DLL0**	80
82h	UART0 Interrupt Enable Register (when DLAB=0)	**IER0**	81
	UART0 Divisor Latch [High Byte] (when DLAB=1)	**DLM0**	80
84h	UART0 Interrupt Identification Register (when Read)	**IIR0**	82
	UART0 FIFO Control Register (when Write)	**FCR0**	83
86h	UART0 Line Control Register	**LCR0**	84
88h	UART0 MODEM Control Register	**MCR0**	85
8Ah	UART0 Line Status Register	**LSR0**	86
8Ch	UART0 MODEM Status Register	**MSR0**	88
8Eh	UART0 Scratch Register	**SCR0**	89
10h	UART1 Receiver Buffer Register (when DLAB=0 & Read)	**RBR1**	79
	UART1 Transmitter Holding Register (when DLAB=0 & Write)	**THR1**	80
	UART1 Divisor Latch [Low Byte] (when DLAB=1)	**DLL1**	80
12h	UART1 Interrupt Enable Register (when DLAB=0)	**IER1**	81
	UART1 Divisor Latch [High Byte] (when DLAB=1)	**DLH1**	80
14h	UART1 Interrupt Identification Register (when Read)	**IIR1**	82
	UART1 FIFO Control Register (when Write)	**FCR1**	83
16h	UART1 Line Control Register	**LCR1**	84
18h	UART1 MODEM Control Register	**MCR1**	85
1Ah	UART1 Line Status Register	**LSR1**	86
1Ch	UART1 MODEM Status Register	**MSR1**	88
1Eh	UART1 Scratch Register	**SCR1**	89

7.3 SDRAM Control Registers (Base Address FE00h)

Offset (HEX)	Register Name	Mnemonic	Page
F0h	SDRAM Arbiter Control Register	**SDRAMACR**	96
F2h	SDRAM Mode Set Register	**SDRAMMSR**	97
F4h	SDRAM Control Register	**SDRAMCR**	98
F6h	SDRAM Timing Parameter Register	**SDRAMTPR**	99

7.4 Fast Ethernet MAC Control Registers (Base Address: MAC1 / FE00h)

Offset (HEX)	Register Name	Mnemonic	Page
00h	MAC Control Register 0	**MCR0**	103
04h	MAC Control Register 1	**MCR1**	104
08h	MAC Bus Control Register	**MBCR**	105
0Ch	TX Interrupt Control Register	**MTICR**	106

10h	RX Interrupt Control Register	**MRICR**	106
14h	TX Poll Command Register	**MTPR**	107
18h	RX Buffer Size Register	**MRBSR**	107
1Ah	RX Descriptor Control Register	**MRDCR**	108
1Ch	MAC Last Status Register	**MLSR**	108
20h	MAC MDIO Control Register	**MMDIO**	109
24h	MAC MII Read Data Register	**MMRD**	110
28h	MAC MII Write Data Register	**MMWD**	110
2Ch	MAC TX Descriptor Start Address Register 0	**MTDSA0**	110
30h	MAC TX Descriptor Start Address Register 1	**MTDSA1**	111
34h	MAC RX Descriptor Start Address Register 0	**MRDSA0**	111
38h	MAC RX Descriptor Start Address Register 1	**MRDSA1**	113
3Ch	MAC INT Status Register	**MISR**	113
40h	MAC INT Enable Register	**MIER**	113
44h	MAC Event Counter INT Status Register	**MECISR**	113
48h	MAC Event Counter INT Mask Register	**MECIER**	114
50h	MAC Successfully Received Packet Counter	**MRCNT**	115
52h	MAC Event Counter 0 Register	**MECNT0**	115
54h	MAC Event Counter 1 Register	**MECNT1**	116
56h	MAC Event Counter 2 Register	**MECNT2**	116
58h	MAC Event Counter 3 Register	**MECNT3**	116
5Ah	MAC Successfully Transmit Packet Counter Register	**MTCNT**	117
5Ch	MAC Event Counter 4 Register	**MECNT4**	117
5Eh	MAC Pause Frame Counter Register	**MPCNT**	118
60h	MAC Hash Table Word 0	**MAR0**	118
62h	MAC Hash Table Word 1	**MAR1**	118
64h	MAC Hash Table Word 2	**MAR2**	119
66h	MAC Hash Table Word 3	**MAR3**	119
68h	MAC Multicast Address first two bytes Register	**MID0L**	120
6Ah	MAC Multicast Address second two bytes Register	**MID0M**	120
6Ch	MAC Multicast Address last two bytes Register	**MID0H**	120
70h	MAC Multicast Address first two bytes Register	**MID1L**	121
72h	MAC Multicast Address second two bytes Register	**MID1M**	121
74h	MAC Multicast Address last two bytes Register	**MID1H**	121
78h	MAC Multicast Address first two bytes Register	**MID2L**	122
7Ah	MAC Multicast Address second two bytes Register	**MID2M**	122
7Ch	MAC Multicast Address last two bytes Register	**MID2H**	122
80h	MAC Multicast Address first two bytes Register	**MID3L**	123
82h	MAC Multicast Address second two bytes Register	**MID3M**	123
84h	MAC Multicast Address last two bytes Register	**MID3H**	123

The following registers are for internal Ethernet special function testing.

Offset (HEX)	Register Name	Mnemonic	Page
ACh	The Configure of Test Mode	**MTSCF**	124
AEh	For Test Mode Control	**MTSCR**	124
B0h	TX FIFO RD/WR in Test Mode	**MTSTF**	125
B2h	RX FIFO RD/WR in Test Mode	**MTSRF**	125
B4h	The RX Status in Test Mode	**MTSRS**	126

8. Peripheral Control Block Registers

The peripheral control block can be mapped into either memory or I/O space by programming the Peripheral Control Block Registers (FEh Registers). It starts at FF00h in I/O space after reset.

Register Offset: FEh
Register Name: Peripheral Control Block Relocation Register
Reset Value : 20FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	S/M_n	Rsvd	M/IO_n	R [19:8]											

The Peripheral Control Block (PCB) is mapped into either memory or I/O space by programming this register. When the other chip selects (PCSx_n) are programmed to zero wait-states and ignore the external ready, PCSx_n can overlap the control block.

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14	S/M_n	R/W	Slave/Master – Configures the interrupt controller. Set 0: Master mode. Set 1: Slaved mode.
13	Rsvd	RO	Reserved
12	M/IO_n	R/W	Memory/IO space. At reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space. Set 1: The PCB is located in memory space. Set 0: The PCB is located in I/O space. (Default)
11-0	R[19:8]	R/W	Relocation Address Bits. The upper address bits of the PCB base address. The lower eight bits are defaulted to 00h. When the PCB is mapped into the I/O space, the R[19:16] must be programmed to 0000b.

Register Offset: F4h
Register Name: Processor Release Level Register
Reset Value : 10D9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	1	1	0	1	1	0	0	1

The read only registers specify the processor release version and identification number.

Bit	Name	Attribute	Description

15-12	PRL	RO	4'b0001
11-8	PV	RO	Processor version. 0h: version A.
7-0	ID	RO	Identification number 2'hD9.

Register Offset: F8h
Register Name: Processor Extended ID Register
Reset Value : 3030h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEID															

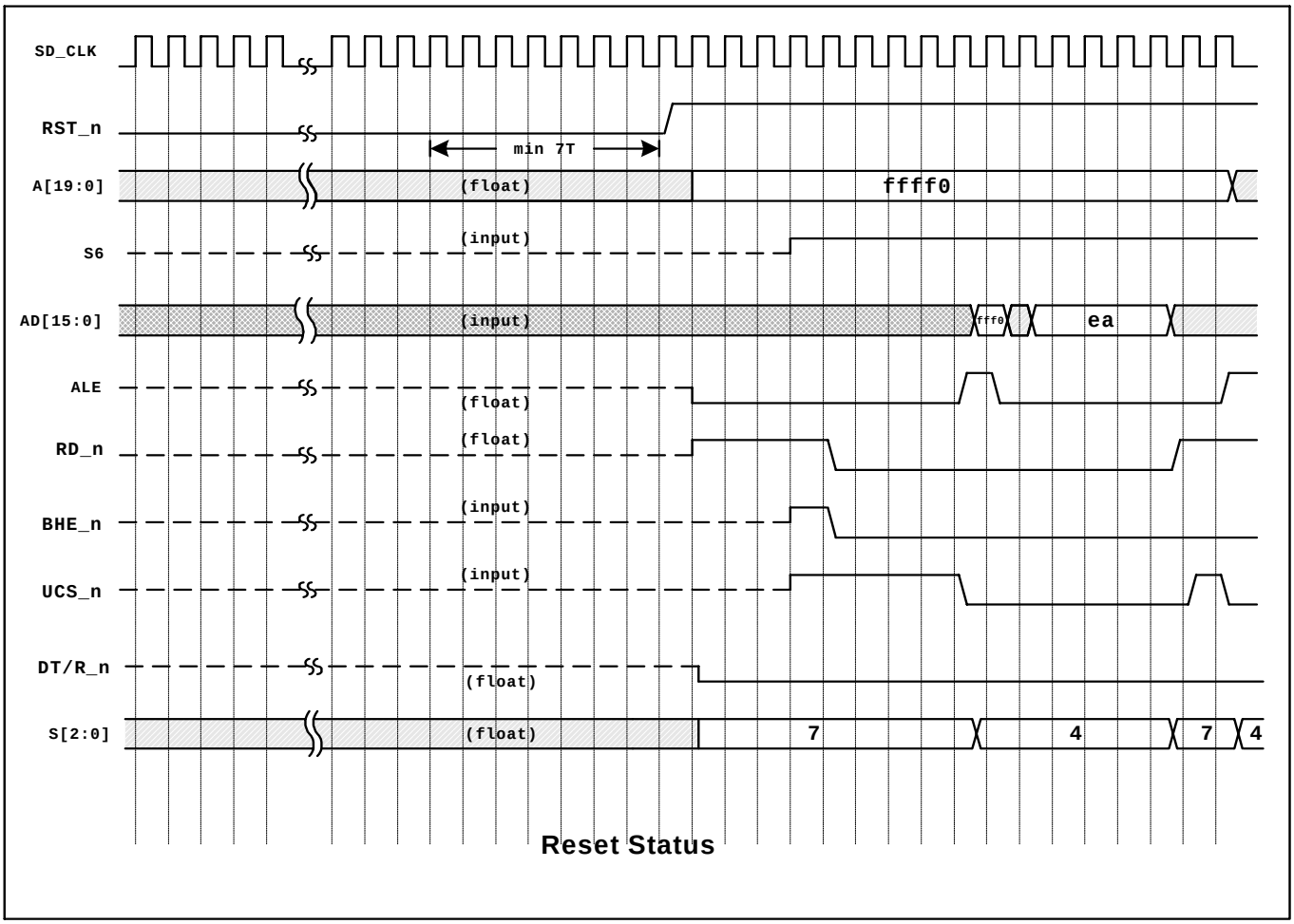
Bit	Name	Attribute	Description
15-0	PEID	RO	This read only register specifies the identification extended number.

9. Reset

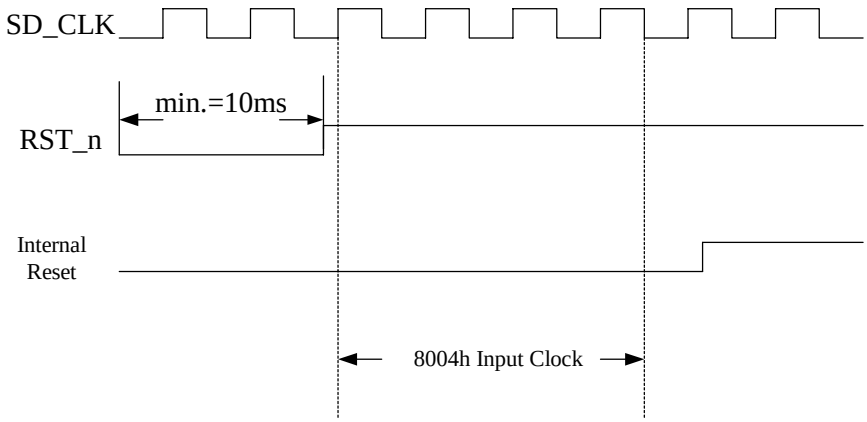
Processor initialization is accomplished with activation of the RST_n pin. To reset the processor, this pin should be held low for at least seven oscillator periods. The Reset Status Figure shows the status of the RST_n pin and the other related pins.

When RST_n goes from low to high, the state of input pins (with weak pull-up or pull-down resistors) will be latched, and each pin will perform the individual function. The AD [15:0] will be latched into the register F6h.

9.1 Power-up reset



Reset Status



Power-up Reset Timing

After watchdog timeout is processed, the system will be reset and the EVA-X1610C will re-latch AD[15:0] into the RESCON register. Unfortunately, sometimes it latches the wrong data in the RESCON register. To avoid this problem, programs can be used to check WTCR (Watchdog Timer Control Register) bit13. When the system is a cold boot, WTCR bit13 is “0” and the RESCON register can be processed by programs. When the system is re-started by the watchdog timeout, WTCR bit13 is “1” and the RESCON check can be skipped by programs.

Register Offset: F6h
Register Name: Reset Configuration Register
Reset Value : AD [15:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC															

Bit	Name	Attribute	Description
15-0	RC	RO	Reset Configuration AD [15:0]. The AD [15:0] must be with weak pull-up or pull-down resistors to correspond the contents when they are latched into this register as the RST_n signal goes from low to high. The value of the reset configuration register provides the system information when the software reads this register. This register is read only and the contents remain valid until next processor reset.

10. Bus Interface UNIT

10.1 Slow Bus and Memory Shadow

10.1.1 Normal Bus and Slow Bus

There are two kinds of buses, called "**normal bus**" and "**slow bus**", in EVA-X1610C. In order to use slow bus, users may set BMOD bit to "0" in Bus Control Register [15].

In **normal bus**, EVA-X1610C uses the same pin to process Memory and I/O access to external devices. A [19:0] pins are used for address and AD [15:0] for data. In order to let the CPU access to the I/Os and the MAC Controller access to the SDRAM work at the same time, the powerful EVA-X1610C provides another bus called "**slow bus**" to separate SDRAM and I/O access via different pins.

In **slow bus**, the MAC controller access to the SDRAM and the CPU access to the external IO devices can work at the same time via different pins. In this bus mode, SDRAM accesses via MA [10:0] for address and AD [15:0] for data (Check the pin out). I/O accesses external devices via pin SAD [15:0] under 16-bit mode or via pin SAD [7:0] under 8-bit mode. Only byte access is allowed if 8-bit mode is selected. 16-bit mode or 8-bit mode is configured by hardware trapping at power on reset via SBWSEL (pin 29).

10.1.2 Normal Operation, DMA Operation, and Shadow Operation Mode

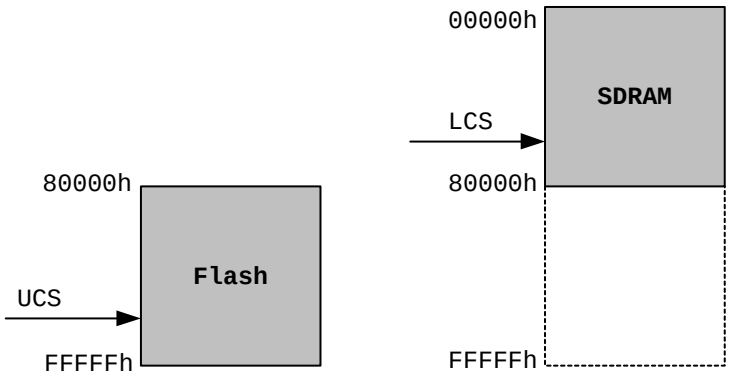
In order to improve the code fetch speed, EVA-X1610C provides one shadow memory operation, called **shadow mode**. Users can fetch codes from the SDRAM instead of the Flash/ROM to increase system performance after moving the codes from the Flash/ROM to the SDRAM. During shadow mode, the LCS_n space can extend from 512K Bytes to 1M Bytes to access the SDRAM and can fetch codes from the SDRAM. The following describes how the memory shadow works.

(a) Normal Operation Mode

The default operation mode after reset is normal operation mode. The CPU fetches code from the Flash/ROM. These two bits, SHADMOD [1:0] in Bus Control Register (EAh), will be 2'b00 as default.

LCS_n is used for accessing the SDRAM and its space is from 0 to 512K Bytes.

UCS_n is used for accessing the Flash/ROM and its space is from 80000h to FFFFFh Bytes.



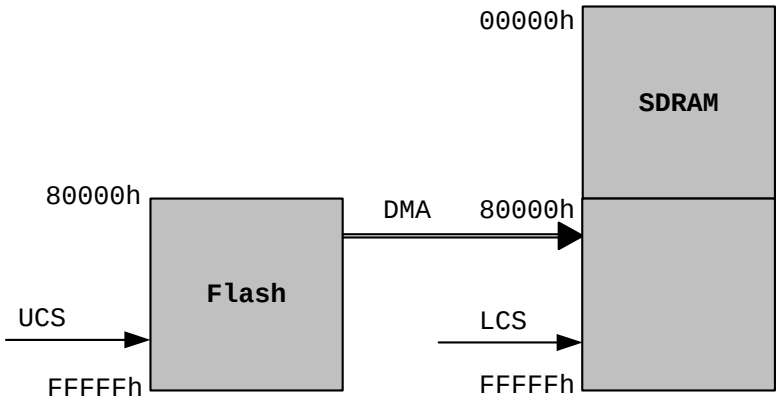
Note: LCS_n is an internal signal.

(b) DMA Operation Mode

This mode is provided to move codes from the Flash/ROM to the SDRAM at the same address. Set these two bits of SHADMOD [1:0], in Bus Control Register, to 2'b01, followed by a DMA instruction to tell the CPU to do DMA transfer. The DMA transfer is a read from the Flash/ROM followed by a write to the SDRAM at the same address.

LCS_n is used for accessing the SDRAM and its space is from 0 to 1M Bytes.

UCS_n is used for accessing the Flash/ROEM and its space is from 512K Bytes to 1M Bytes.

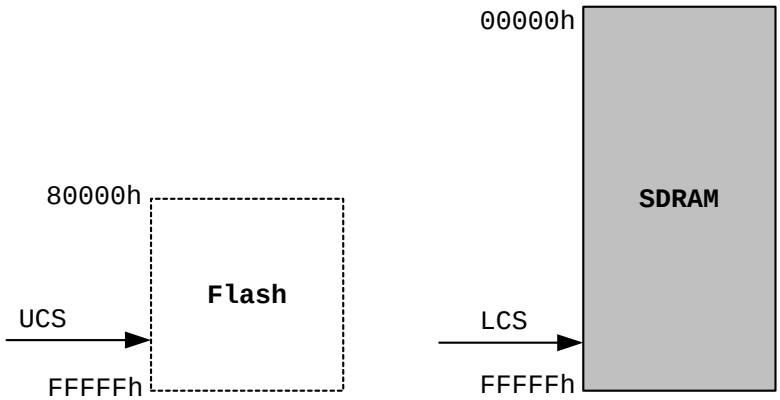


(c) Shadow Operation Mode

Under this mode, the CPU fetches code from the SDRAM instead of from the Flash/ROM. Setting SHADMOD [1:0], in Bus Control Register, to 2'b10 or 2'b11 will enable shadow operation mode.

LCS_n is used for accessing SDRAM and its space is from 0 to 1M Bytes.

UCS_n is not used.



10.1.3 A user guide to use shadow memory

(a) Set Bus Control Register [1:0] (EAh)= 01b (DMA mode).

(b) Configure the DMA source address to be the DMA destination address.

(c) Configure the DMA Transfer Count

(d) Register according to the transfer size you need.

(e) After DMA is transferred, set Bus Control Register [1:0] (EAh) to 2'b10 (Shadow mode).

(f) If the system is 8-bit boot mode, the code fetch from SDRAM is always 16-bit mode.

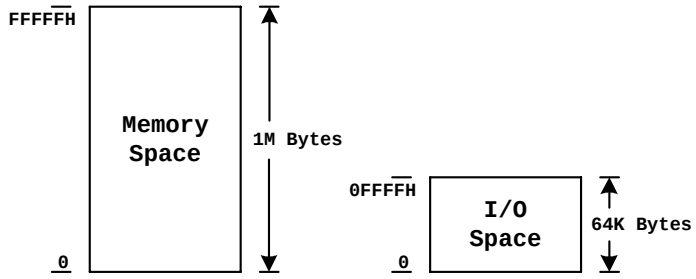
Register Offset: EAh
Register Name: Bus Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMOD														SHAD MOD1	SHAD MOD0

Bit	Name	Attribute	Description
15	BMOD	R/W	Bus Mode Select bit. Set 0: Slow bus mode. When the PCS regions are accessed, the bus cycle is mapped to SAD [15:0] or SAD [7:0]. Set 1: Normal bus mode. When the PCS regions are accessed, the bus cycle is mapped to A [19:0] and D [15:0].
1-0	SHADMOD	R/W	Memory Shadow Operation Mode. 00: Normal Operation Mode. 01: DMA Operation Mode. 10: Shadow Operation Mode. The CPU fetches code from the SDRAM.

10.2 Memory and I/O Interface

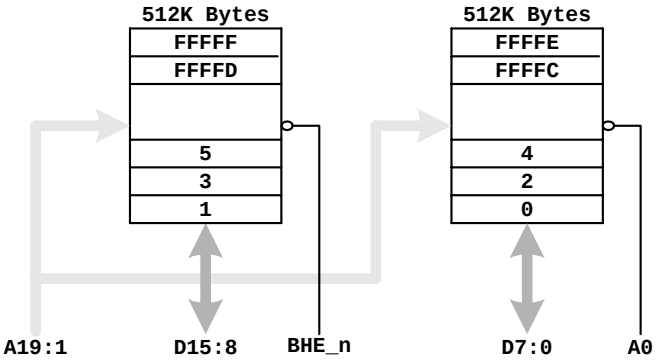
The memory space consists of 1M bytes (512k 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instruction can access I/O address space, and information must be transferred between the peripheral devices and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64k bytes I/O address space can be accessed indirectly, through the DX register. I/O instructions always force address A[19:16] to low level.



Memory and I/O Space

10.3 Data Bus

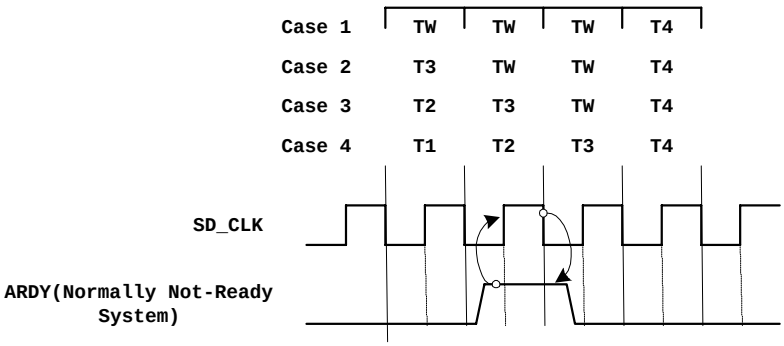
The memory address space data bus is physically implemented by dividing the address space into two banks of up to 512k bytes. Each bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0). The other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). A0 and BHE_n determine whether one bank or both banks participate in the data transfer.



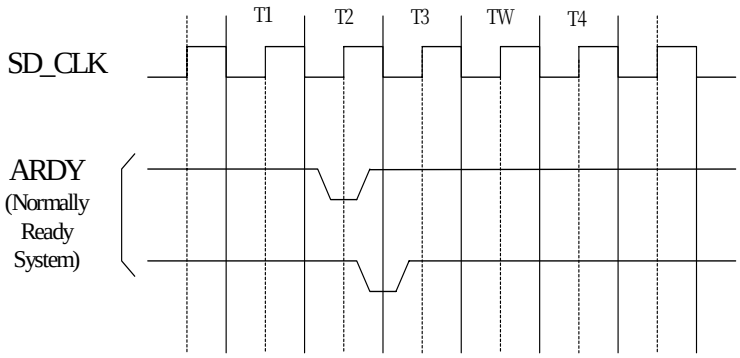
Physical Data Bus Models

10.4 Wait States

Wait states extend the data phase of the bus cycle. The ARDY input with low level will insert wait states. To avoid wait states, ARDY must be high within a specified setup time prior to phase 2 of T2. To insert wait states, ARDY must be driven low within a specified setup time prior to phase 2 of T2 or phase 1 of T3. When the SDRAMEN bit in the SDRAM Control Register (FEF4h) is set to 1, the external ready ARDY and internal wait states are ignored while accessing the SDRAMs.



Asynchronous Ready Waveforms



Asynchronous Ready Waveforms

10.5 Bus Width

The EVA-X1610C default is 16-bit bus access and the bus can be programmed as 8-bit or 16-bit access during memory or I/O access is located in the LCS_n or PCSx_n address space. The UCS_n code- fetched selection can be 8-bit or 16-bit bus width, which is decided by the BWSEL pin (pin38) input status when the RST_n pin goes from low to high. When the BWSEL pin is with a pull-low resistor, the bus width for the code-fetched selection is 8 bits. The SDRAM bus width is unchangeable 16 bits. If the EVA-X1610C has been set as 16-bit mode, it cannot be changed to 8-bit mode.

Register Offset: F2h
Register Name: Auxiliary Configuration Register
Reset Value : 0080 or 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								USIZ	0	0	0	0	Rsvd	MSIZ	IOSIZ

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	USIZ	R/W	Boot code bus width. This bit reflects the BWSEL pin input status when the RST_n pin goes from low to high. Set0: 16-bit bus width booting when the BWSEL pin is **without a pull-low** resistor. (Default: It is an internal pull-high pin.) Set1: 8-bit bus width booting when the BWSEL pin is with 4.7k ohm external pull-low resistor. If the EVA-X1610C has been set as 16-bit mode, it cannot be changed to 8-bit mode. If the EVA-X1610C has been set as 8-bit mode, it can be changed to 16-bit mode.
2	Rsvd	RO	Reserved.
1	MSIZ	R/W	Memory Space Data Bus Size selection. This bit determines the width of the data bus for all memory accesses on PCS_n space. Set 1: 8-bit data bus access. Set 0: 16-bit data bus access.
0	IOSIZ	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. Set 1: 8-bit data bus access. Set 0: 16-bit data bus access.

11. Chip Select UNIT

The Chip Select Unit provides 12 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through four peripheral control registers (A0h, A2h, A4h, and A8h) and all of the chip selects can insert wait states by programming the peripheral control registers.

11.1 UCS_n

The UCS_n default is active on reset for Code access. The active memory range is upper 512k (80000h – FFFFFh), which is programmable. And the defaulted active memory range of UCS_n is 64k (F0000h – FFFFFh). The UCS_n will drive low within four SD_CLK cycles when active if no wait state is inserted. There are fifteen wait states inserted to UCS_n active cycle on reset.

Register Offset: A0h
Register Name: Upper Memory Chip Select Register
Reset Value : F03Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB [2:0]			0	0	0	0	DA	0	1	1	R3	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-12	LB[2:0]	R/W	**LB[2:0]**, Memory block size selection for UCS_n chip select pin. The active region of the UCS_n chip select pin can be configured by LB2-LB0. The default memory block size is from F0000h to FFFFFh. **LB2, LB1, LB0** ---- **Memory Block size** , **Start address**, **End Address** 1 , 1 , 1 ---- 64k , F0000h , FFFFFh 1 , 1 , 0 ---- 128k , E0000h , FFFFFh 1 , 0 , 0 ---- 256k , C0000h , FFFFFh 0 , 0 , 0 ---- 512k , 80000h , FFFFFh
11-8	Rsvd	RO	Reserved
7	DA	R/W	Disable Address. If the ADEN_n pin is held high on the rising edge of RST_n, then the DA bit is valid to enable/disable the address phase of the AD bus. If the ADEN_n pin is held low on the rising edge of RST_n, the AD bus always drives the address and data. Set 1: Disable the address phase of the AD[15:0] bus cycle when UCS_n is asserted. Set 0: Enable the address phase of the AD[15:0] bus cycle when UCS_n is asserted.
6-4	Rsvd	RO	Reserved
3	R3	R/W	See Bit[1:0].

2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for the UCS_n chip select. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit3, Bit 1-0: R3, R1-R0**, Wait-State value. EVA-X1610C can insert wait states for an access to the UCS_n memory cycle. The reset value for (R3, R1, R0) is (1, 1, 1). **R3, R1, R0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 2 0, 1, 1 -- 3 1, 0, 0 -- 5 1, 0, 1 -- 7 1, 1, 0 -- 9 1, 1, 1 -- 15

11.2 LCS_n (Internal Signal)

LCS_n means the lower memory region chip selects. The active memory range is not programmable. Its defaulted size is 1M-(upper memory block size) bytes. The LCS_n signal is not active on reset, but any read or write access to the A2h register activates this signal.

Register Offset: A2h
Register Name: Low Memory Chip Select Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DA	0	1	1	1	1	1	1

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	DA	R/W	Disable Address. If the ADEN_n pin is held high or floating on the rising edge of RST_n, then the DA bit is valid to enable/disable the address phase of the AD bus. If the ADEN_n pin is held low on the rising edge of RST_n, the AD bus always drives the address and data. Set 1: Disable the address phase of the AD[15:0] bus cycle when LCS_n is asserted. Set 0: Enable the address phase of the AD[15:D0] bus cycle when LCS_n is asserted.
6	Rsvd	RO	1'b0
5-0	Rsvd	RO	Reserved

11.3 PCSx_n

In order to define these pins, the peripheral or memory chip selects are programmed through A4h and A8h registers. The base address memory block can be located anywhere within the 1M bytes memory space, exclusive of the areas associated with LCS_n and UCS_n. If the chip selects are mapped to I/O space, the access range is 64k bytes. PCS5_n can be configured from (0 to 11wait states) + (0 to 3 wait states). PCS3_n – PCS0_n can be configured from (0 to 11 wait states) + (0 to 15 wait states). The PCSx_n pins are not active on reset. The PCSx_n pins are activated as chip selects by writing to the peripheral chip select register 0 and 1.

Register Offset: A4h
Register Name: Peripheral Chip Select Register 0
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA [19:12]								0	W2	W1	W0	R3	R2	R1	R0

Bit	Name	Attribute	Description
15-8	BA[19:12]	R/W	Base Address. BA[19:12] corresponds to Bit [19:12] of the 1M-Byte (20-bits) programmable base address of the PCS_n chip select block. When the PCS_n chip selects are mapped to I/O space, BA[19:16] must be written to 0000b because the I/O address bus is only 64K bytes (16 bits) wide. **PCSx_n address range:** PCS0_n : Base Address - Base Address+255 PCS1_n : Base Address+256 - Base Address+511 PCS2_n : Base Address+512 - Base Address+767 PCS3_n : Base Address+768 - Base Address+1023 PCS5_n : Base Address+1280 - Base Address+1535
6-4	W[2:0]	R/W	Wait-State Value. W[2:0] determine the number of wait states inserted into T1 of PCS5_n and the PCS3_n – PCS0_n access. **W2, W1, W0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 2 0, 1, 1 -- 3 1, 0, 0 -- 5 1, 0, 1 -- 7 1, 1, 0 -- 9 1, 1, 1 -- 11
3	R3	R/W	See Bit[1:0].
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the ready mode for the PCS3_n – PCS0_n chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 3, Bit 1-0: R3, R1, R0**, Wait-State Values. R3, R1, and R0 determine the number of wait states inserted into T3 of the PCS3_n – PCS0_n access.

			R3,	**R1,**	**R0**	**--**	**Wait States**
			0,	0,	0	--	0
			0,	0,	1	--	1
			0,	1,	0	--	2
			0,	1,	1	--	3
			1,	0,	0	--	5
			1,	0,	1	--	7
			1,	1,	0	--	9
			1,	1,	1	--	15

Register Offset: A8h
Register Name: Peripheral Chip Select Register 1
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Rsvd	MS	1	1	1	R2	R1	R0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	Rsvd	RO	Reserved
6	MS	R/W	IO space selector. This bit determines whether the PCS_n pins are active during IO bus cycle. Set 0: PCS_n is only active for IO cycle.
2	R2	R/W	Ready Mode. This bit only applies to the PCS5_n chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	Wait-State Values. The R[2:0] determine the number of wait states inserted into T3 of PCS5_n. **R1, R0 -- Wait States** 0, 0, -- 0 0, 1, -- 1 1, 0, -- 2 1, 1, -- 3

12. Refresh Control UNIT

The Refresh Control Unit (RCU) automatically generates refresh bus cycle. After a period of time, the RCU generates a memory read request to the bus interface unit.

A user guide to program SDRAM:

(1) Configure Lower Memory Chip Select Register (A2h) to set SDRAM space. The suggestion value is 7F38h.

(2) Set Clock Prescaler Register (E2h) and enable RCU Register (E4h) to enable SDRAM refresh.

Register Offset: E2h
Register Name: Clock Prescaler Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RC [14:0]														

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-0	RC[14:0]	RW	Refresh Counter Reload Value. It contains the value of the desired clock count interval between refresh cycles. The counter value should not be set to less than 12h, otherwise there would never be sufficient bus cycle available for the processor to execute code. For Example: SDRAM specification specifies to refresh 1 time every 15.6 u sec and system clock is 25Mhz. The Refresh Counter Reload Value = 15.6us*25Mhz = 15.6us / 40ns = 390.

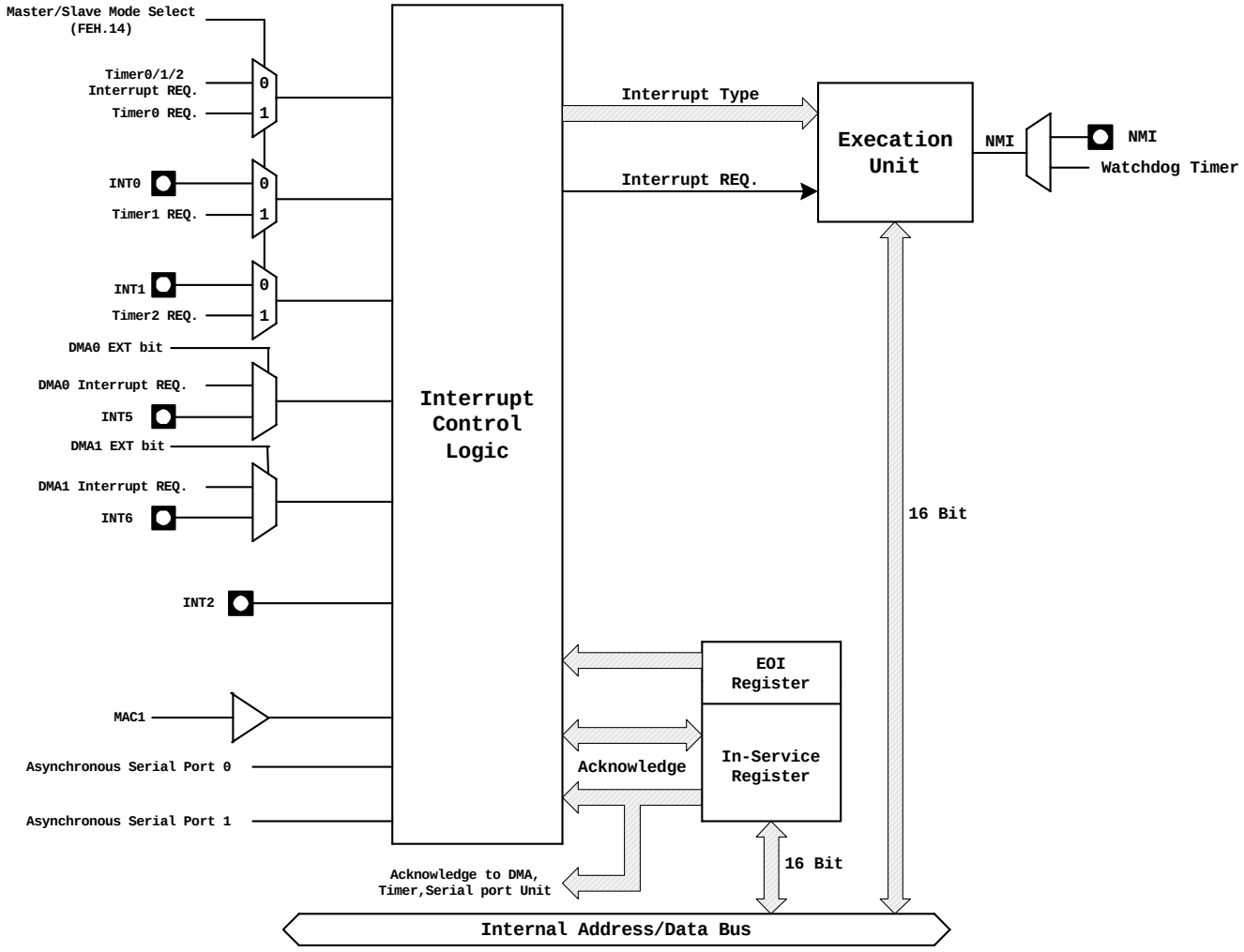
Register Offset: E4h
Register Name: Enable RCU Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	T[14:0]														

Bit	Name	Attribute	Description
15	E	RW	Enable RCU Set 1: Enable the refresh counter unit. Set 0: Clear the refresh counter and stop refresh requests, but will not reset the refresh address.
14-0	T[14:0]	RO	Refresh Count. This read-only field contains the present value of the down counter which triggers refresh requests.

13. Interrupt Controller UNIT

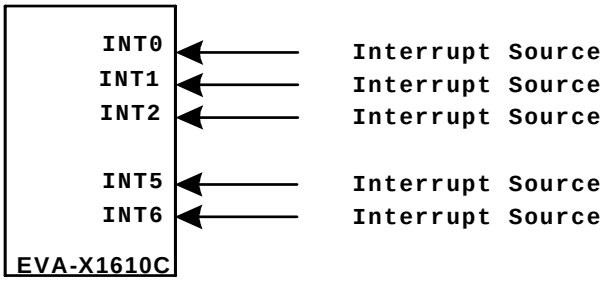
There are 15 interrupt request sources connected to the controller: 5 maskable interrupt pins (INT[0:2], INT5, INT6); 2 non-maskable interrupts (NMI, WDT); 8 internal unit request sources (Timer 0, 1, 2; DMA 0, 1; MAC 1; Asynchronous Serial Port 0, 1).



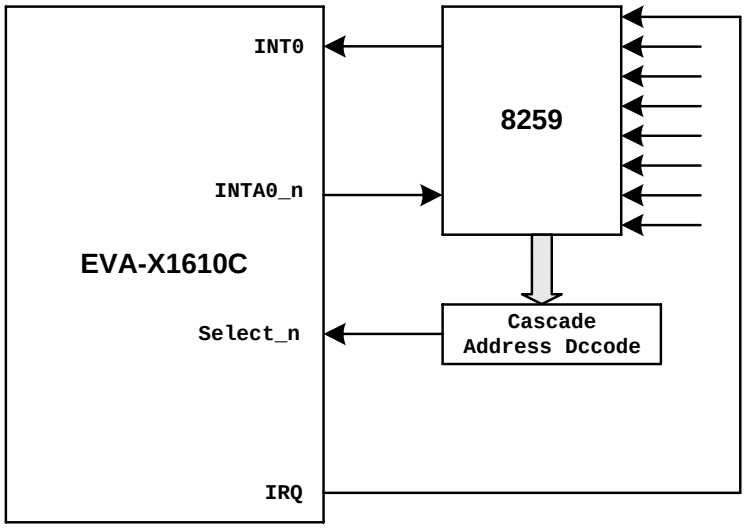
Interrupt Control Unit Block Diagram

13.1 Master Mode and Slave Mode

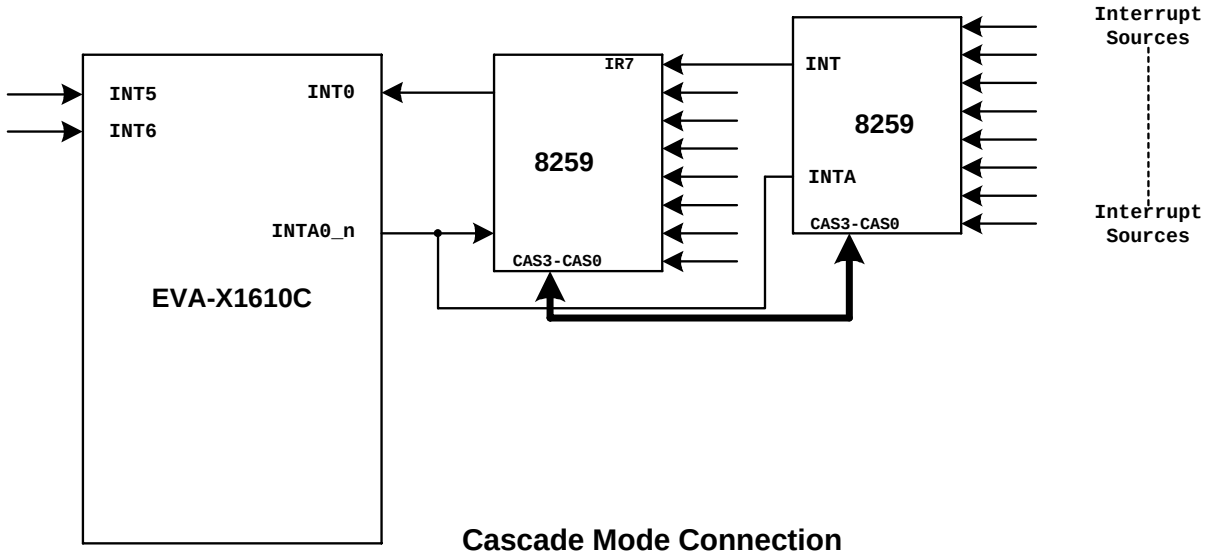
The interrupt controller can be programmed as a master or slave mode. (To program FEh [14]), the master mode has two connections: Fully Nested Mode connection or Cascade Mode connection.



Fully Nested Mode Connections



Slave Mode Connection



Cascade Mode Connection

13.2 Interrupt Vector, Type and Priority

The following table shows the interrupt vector address, type and the priority. The maskable interrupt priority can be changed by programming the priority registers. The vector address for each interrupt was fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Opcode Exception	06h	18h		1	
ESC Opcode Exception	07h	1Ch		1	
Timer 0	08h	20h	08	2-1	*/**
Reserved	09h				
DMA 0/INT5	0Ah	28h	0A	3	**
DMA 1/INT6	0Bh	2Ch	0B	4	**
INT0	0Ch	30h	0C	5	
INT1	0Dh	34h	0D	6	
INT2	0Eh	38h	0E	7	
MAC	10h	40h	10	9	
Asynchronous Serial port 1	11h	44h	11	9	
Timer 1	12h	48h	08	2-2	*/**
Timer 2	13h	4Ch	08	2-3	*/**
Asynchronous Serial port 0	14h	50h	14	9	
Reserved	15h-1Fh				

Note *: When the interrupt occurs in the same time, the priority is (1-1 > 1-2); (2-1> 2-2 > 2-3)

Note **: The interrupt types of these sources are programmable in slave mode.

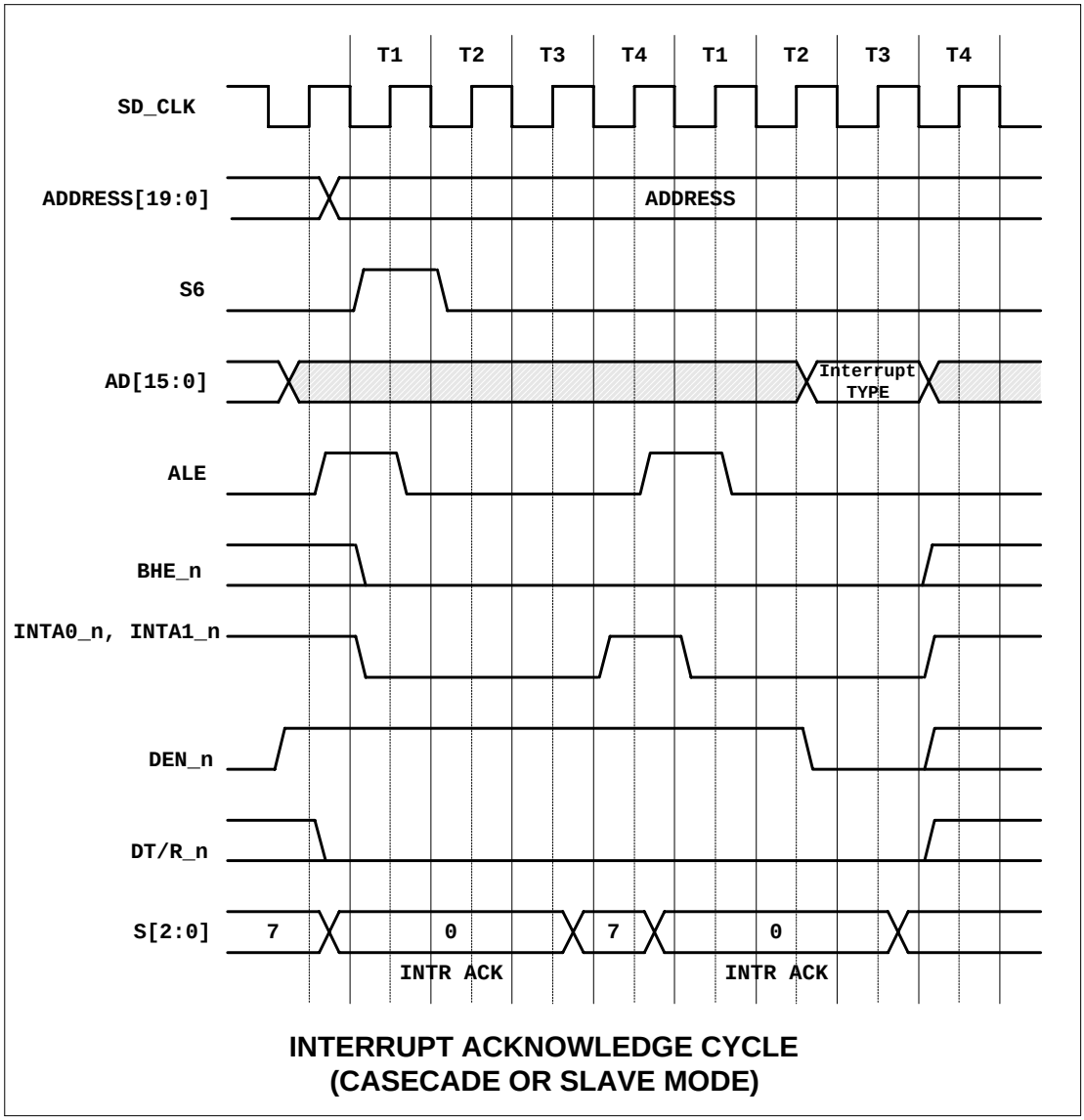
13.3 Interrupt Requests

When an interrupt is requested, the internal interrupt controller verifies the interrupt is enabled (the IF flag is enabled and the MSK bit is not set) and that there are no higher priority interrupt requests being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-trigger) to request the interrupt controller service, the INT pins must be held till the microcontroller entering the interrupt service routine. There is no interrupt-acknowledge output when running in fully nested mode, so it should use PIO pin to simulate the interrupt-acknowledge pin if necessary.

13.4 Interrupt Acknowledge

The processor requires the interrupt type as an index into the interrupt table. The interrupt type can be provided by an internal or external interrupt controller. The internal interrupt controller provides the interrupt type to the processor without external bus cycles generation. When an external interrupt controller is providing the interrupt type, the processor generates two acknowledge bus cycles, and the interrupt type is written to the AD7-AD0 lines by the external interrupt controller.



INTERRUPT ACKNOWLEDGE CYCLE (CASECADE OR SLAVE MODE)

13.5 Programming the Registers

Software is programmed through the registers (**Master mode:** 44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h and 22h; **Slave Mode:** 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 22h and 20h) to define the interrupt controller operation.

Register Offset: 44h
Register Name: Serial Port 0 Interrupt Control Register
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 0. Set 0: Enable the serial port 0 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals. **The priority selection:** **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 42h
Register Name: Serial Port 1 Interrupt Control Register
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 1. Set 0: Enable the serial port 1 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals.

			The priority selection: **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 40h
Register Name: MAC Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set to 1 and bit 4 is cleared to 0, an interrupt is triggered by edge from MAC1, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by the high active level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of MAC. Set 0: Enable the MAC interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 3Ch
Register Name: INT2 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the high active level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT2. Set 0: Enable the INT2 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 3Ah
Register Name: INT1 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enables. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT1
5	C	R/W	Cascade Mode. Set this bit to 1 to enable the cascade mode for INT1.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the high active level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT1. Set 0: Enable the INT1 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

(Slave Mode)

This register is for **Timer 2 interrupt control.** Its **reset value** is 000Fh.

Bit	Name	Attribute	Description

15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of Timer 2. Set 0: Enable the Timer 2 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 38h
Register Name: INT0 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT0
5	C	R/W	Cascade Mode. Set this bit to 1 to enable the cascade mode for INT0.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the high active level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT0. Set 0: Enable the INT0 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

(Slave Mode)

For **Timer 2 Interrupt Control Register,** the **reset value** is 000Fh.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of Timer 1. Set 0: Enable the Timer 1 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 36h
Register Name: DMA1/INT6 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA1 controller. Set 0: Enable the DMA1 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

(Slave Mode)

The **reset value** is 000Fh.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA1 controller. Set 0: Enable the DMA1 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 34h
Register Name: DMA0/INT5 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA0 controller. Set 0: Enable the DMA0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

(Slave Mode)

The **reset value** is 000Fh.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA0 controller. Set 0: Enable the DMA0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 32h

Register Name: Timer Interrupt Control Register

Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the timer controller. Set 0: Enable the timer controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

(Slave Mode)

The **reset value** is 000Fh.

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the timer 0 controller. Set 0: Enable the timer 0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 30h
Register Name: Interrupt Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved									MAC1	Reserved		TMR2	TMR1	TMR0

(Master Mode)

The **reset value** is not defined.

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-maskable interrupts occur. Set 0: When an IRET instruction is executed.
14-6	Rsvd	RO	Reserved
5	MAC1	R/W	Indicate that the corresponding MAC controller has an interrupt request while set to 1.
4-3	Rsvd	RO	Reserved
2-0	TMR[2:0]	R/W	Indicate that the corresponding timer has an interrupt request pending while set to 1.

(Slave Mode)

The **reset value** is 0000h.

Bit	Name	Attribute	Description
15	DHLT	R/W	DMA Halt. Set 1: Halt any DMA activity when non-maskable interrupts occur. Set 0: when an IRET instruction is executed.
2-0	TMR[2:0]	R/W	Indicate that the corresponding timer has an interrupt request pending while set to 1.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	MAC	Rsvd	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

(Master Mode)

The Interrupt Request register is a read-only register. For internal interrupts (SP0, SP1, D1/I6, D0/I5, MAC, and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT2-INT0 external interrupts, the corresponding bits (I2-I0) reflect the current values of the external signals.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	RO	Serial Port 0 Interrupt Request. Indicates the interrupt status of the serial port 0.
9	SP1	RO	Serial Port 1 Interrupt Request. Indicates the interrupt status of the serial port 1.
8	MAC	RO	MAC Interrupt Request. Indicates the interrupt status of the MAC1.
7	Rsvd	RO	Reserved
6-4	I[2:0]	RO	Interrupt Requests. Set 1: The corresponding INT pin has an interrupt pending.
3-2	D1/I6 – D0/I5	RO	DMA Channel or INT Interrupt Request. Set 1: The corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved
0	TMR	RO	Timer Interrupt Request. Set 1: The timer control unit has an interrupt pending.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/I6	D0/I5	Rsvd	TMR0

(Slave Mode)

The Interrupt Request register is a read-only register. For internal interrupts (D1/I6, D0/I5, TMR2, TMR1, and TMR0), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge.

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5-4	TMR[2:1]	RO	Timer2/Timer1 Interrupt Request. Set 1: Indicates the state of any interrupt requests form the associated timer.
3-2	D1/I6 – D0/I5	RO	DMA Channel or INT Interrupt Request. Set 1: Indicates the corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved
0	TMR0	RO	Timer 0 Interrupt Request. Set 1: Indicates the state of an interrupt request from Timer 0.

Register Offset: 2Ch
Register Name: Interrupt In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	MAC	Rsvd	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

(Master Mode)

These bits in this Register are set by the interrupt controller when the interrupt is taken. Each bit in the register is cleared by writing the corresponding interrupt type to the EOI register.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	R/W	Serial Port 0 Interrupt In-Service. Set 1: the serial port 0 interrupt is currently being serviced.
9	SP1	R/W	Serial Port 1 Interrupt In-Service. Set 1: the serial port 1 interrupt is currently being serviced.
8	MAC	R/W	MAC In_Service. Indicates the MAC1 interrupt is currently being serviced.
7	Rsvd	RO	Reserved
6-4	I[2:0]	R/W	Interrupt In-Service. Set 1: the corresponding INT interrupt is currently being serviced.
3-2	D1/I6 – D0/I5	R/W	DMA Channel or INT Interrupt In-Service. Set 1: the corresponding DMA channel or INT interrupt is currently being serviced.
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt In-Service. Set 1: the timer interrupt is currently being serviced.

Register Offset: 2Ch
Register Name: Interrupt In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/16	D0/15	Rsvd	TMR0

(Slave Mode)

The interrupt controller sets these bits in the In-Service register when the interrupt is taken. Writing related interrupt type to the EOI register clears these in-service bits.

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5-4	TMR[2:1]	R/W	Timer2/Timer1 Interrupt In-Service. Set 1: the corresponding timer interrupt is currently being serviced.

3-2	D1/I6 – D0/I5	R/W	DMA Channel or INT Interrupt In-Service. Set 1: the corresponding DMA Channel or INT Interrupt is currently being serviced.
1	Rsvd	RO	Reserved
0	TMR0	R/W	Timer 0 Interrupt In-Service. Set 1: the Timer 0 interrupt is currently being serviced.

Register Offset: 2Ah
Register Name: Priority Mask Register
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Master Mode)

It determines the minimum priority level at which maskable interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved
2-0	PRM[2:0]	R/W	Priority Field Mask, determining the minimum priority that is required in order for a maskable interrupt source to generate an interrupt. **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

(Slave Mode)

It determines the minimum priority level at which maskable interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved
2-0	PRM[2:0]	R/W	Priority Field Mask, determining the minimum priority that is required in order for a maskable interrupt source to generate an interrupt. **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2

			011	3
			100	4
			101	5
			110	6
			111	(Low) 7

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	MAC	Rsvd	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

(Master Mode)

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	R/W	Serial Port 0 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 0 interrupt is masked.
9	SP1	R/W	Serial Port 1 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 1 interrupt is masked.
8	MAC	R/W	MAC Interrupt Mask. When set 1, this bit indicates that the MAC1 interrupts are masked.
7	Rsvd	RO	Reserved
6-4	I[2:0]	R/W	External Interrupt Mask. When set 1, I3-I0 bits indicate that the corresponding interrupts are masked.
3-2	D1/I6 – D0/I5	R/W	DMA Channel or INT Interrupt Masks. When set 1, these bits indicate that the corresponding interrupts are masked.
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt Mask. When set 1, this bit indicates that the Timer controller interrupt is masked.

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : 003Dh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/I6	D0/I5	Rsvd	TMR0

(Slave Mode)

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5-4	TMR[2:1]	R/W	Timer 2/Timer1 Interrupt Mask. Set 1: Timer2 or Timer1 has its interrupt requests masked.
3-2	D1/I6 – D0/I5	R/W	DMA Channel or INT Interrupt Masks. Set 1: D1/I6 –D0/I5 has its interrupt requests masked.
1	Rsvd	RO	Reserved
0	TMR0	R/W	Timer 0 Interrupt Mask. When set 1, this bit indicates that the Timer controller interrupt is masked.

Register Offset: 26h
Register Name: Interrupt Poll Status Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved											S[4:0]			

(Master Mode)

The Poll Status (POLLST) register mirrors the current state of the Poll register. The POLLST register can be read without affecting the current interrupt requests.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

Register Offset: 24h
Register Name: Interrupt Poll Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

(Master Mode)

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S4-S0 field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

Register Offset: 22h
Register Name: End-of-Interrupt
Reset Value : Write Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSPEC	Reserved										S[4:0]				

(Master Mode)

Bit	Name	Attribute	Description
15	NSPEC	R/W	Non-Specific EOI. Set 1: indicates non-specific EOI. Set 0: indicates the specific EOI interrupt type in S4-S0.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	WO	Source EOI Type. It specifies the EOI type of the interrupt that is currently being processed.

Register Offset: 22h
Register Name: End-of-Interrupt
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	L2	L1	L0

(Slave Mode)

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved
2-0	L[2:0]	WO	Interrupt Type. The encoded value indicates the priority of the IS-bit (interrupt service) to reset. Write these bits cause an EOI issued for the interrupt type in slave mode.

Register Offset: 20h
Register Name: Interrupt Vector Register
Reset Value : 0000h

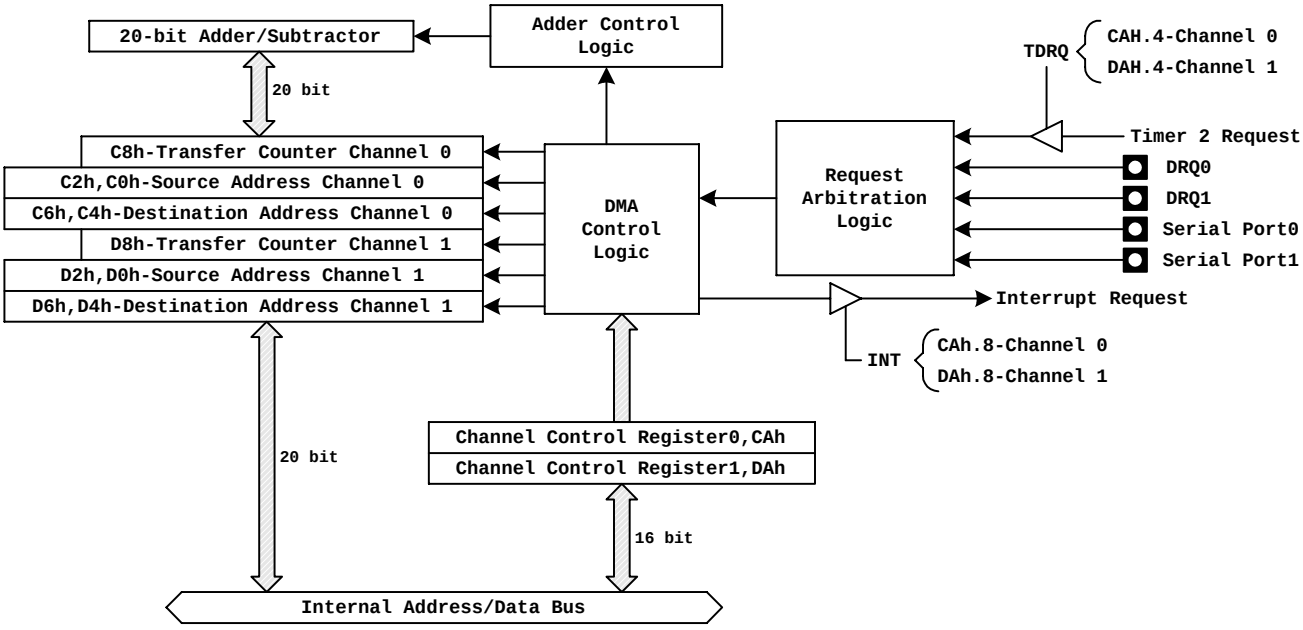
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	T[4:0]					0	0	0

(Slave Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-3	T[4:0]	R/W	Interrupt Types. They set the five bits of the interrupt types for the internal interrupt type. The interrupt controller itself provides the lower three bits of the interrupt types. The following interrupt types of slave mode can be programmed. Timer 2 interrupt controller: (T4, T3, T2, T1, T0, 1, 0, 1) b. Timer 1 interrupt controller: (T4, T3, T2, T1, T0, 1, 0, 0) b. DMA 1 interrupt controller: (T4, T3, T2, T1, T0, 0, 1, 1) b. DMA 0 interrupt controller: (T4, T3, T2, T1, T0, 0, 1, 0) b. Timer 0 interrupt controller: (T4, T3, T2, T1, T0, 0, 0, 0) b.
2-0	Rsvd	RO	Reserved

14. DMA UNIT

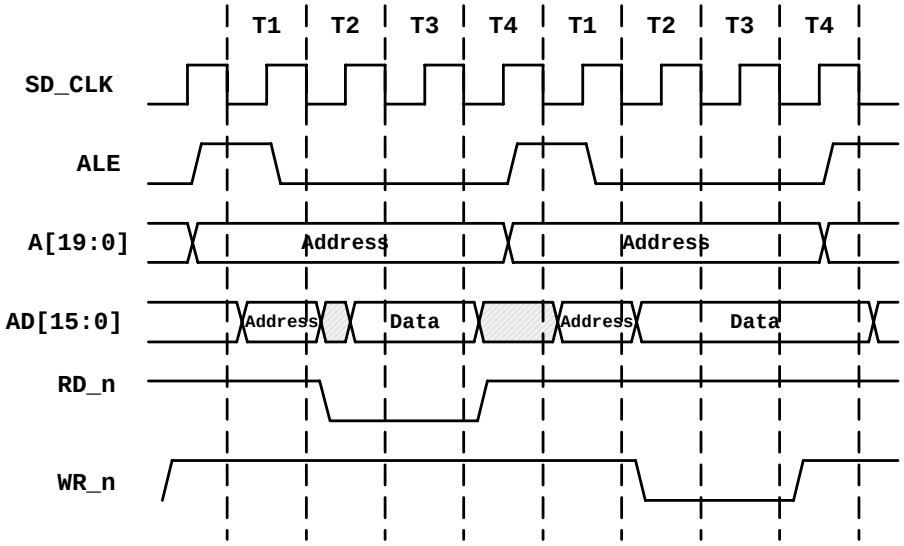
The DMA controller provides the data transfer between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA requests from one of three sources: external pins (DRQ0 for channel 0 or DRQ1 for channel 1), serial ports (port 0 or port 1), or Timer 2 overflow. The data transfer from sources to destinations can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (read from sources and write to destinations) for each data transfer.



DMA Unit Block

14.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfer) and the two bus cycles cannot be separated by a bus hold request, a refresh request, or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h, and D0h) are used to configure and operate the two DMA channels.



Typical DMA Trarsfer

Register Offset: CAh (DMA0)
Register Name: DMA Control Registers
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

The definitions of Bit [15:0] for DMA0 are the same as those of Bit [15:0] of Register DAh for DMA1.

Register Offset: C8h (DMA0)
Register Name: DMA Transfer Count Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 0 Transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: C6h (DMA0)
Register Name: DMA Destination Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DDA[19:16]	R/W	High DMA 0 Destination Address. These bits are mapped to A[19:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

Register Offset: C4h (DMA0)
Register Name: DMA Destination Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: C2h (DMA0)
Register Name: DMA Source Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DSA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DSA[19:16]	R/W	High DMA 0 Source Address. These bits are mapped to A[19:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b

Register Offset: C0h (DMA0)
Register Name: DMA Source Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: DAh (DMA1)
Register Name: DMA Control Registers
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	DM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

Bit	Name	Attribute	Description
15	DM/IO_n	R/W	Destination Address Space Select. Set 1: The destination address is in memory space. Set 0: The destination address is in I/O space.
14	DDEC	R/W	Destination Decrement. Set 1: The destination address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decrement value which is by 1 or 2 when both DDEC and DINC bits are set to 1 or 0. The address remains constant. Set 0: Disable the decrement function.
13	DINC	R/W	Destination Increment. Set 1: The destination address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the decrement function.
12	SM/IO_n	R/W	Source Address Space Select. Set 1: The Source address is in memory space. Set 0: The Source address is in I/O space.
11	SDEC	R/W	Source Decrement. Set 1: The Source address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decremented value is by 1 or 2 when both SDEC and SINC bits are set to 1 or 0. The address remains constant. Set 0: Disable the decrement function.
10	SINC	R/W	Source Increment. Set 1: The Source address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2.

			Set 0: Disable the decrement function.
9	TC	R/W	Terminal Count. Set 1: The synchronized DMA transfer is terminated when the DMA Transfer Count Register reaches 0. Set 0: The synchronized DMA transfer is not terminated when the DMA Transfer Count Register reaches 0. Unsynchronized DMA transfer is always terminated when the DMA Transfer Count register reaches 0, regardless of the setting of this bit.
8	INT	R/W	Interrupt. Set 1: DMA unit generates an interrupt request when the transfer count is completed. The TC bit must be set to 1 to generate an interrupt.
7-6	SYN[1:0]	R/W	Synchronization Type Selection. **SYN1 , SYN0 -- Synchronization Type** 0 , 0 -- Unsynchronized 0 , 1 -- Source synchronized 1 , 0 -- Destination synchronized 1 , 1 -- Reserved
5	P	R/W	Priority. Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred in the same time.
4	TDRQ	R/W	Timer Enable/Disable Request. Set 1: Enable the DMA requests from timer 2. Set 0: Disable the DMA requests from timer 2.
3	EXT	R/W	This bit enables the external interrupt functionality of the corresponding DRQ pin. Set 1: the external pin is an INT pin and requests on the pin are passed to the interrupt controller. Set 0: The pin functions as a DRQ pin.
2	CHG	R/W	Changed Start Bit. This bit must be set to 1 when the ST bit is modified.
1	ST	R/W	Start/Stop DMA channel. Set 1: Start the DMA channel Set 0: Stop the DMA channel
0	B_n/W	R/W	Byte/Word Select. Set 1: The address is incremented or decremented by 2 after each transfer. Set 0: The address is incremented or decremented by 1 after each transfer. Only byte transfer is supported if either source or destination bus width is 8 bit.

Register Offset: D8h (DMA1)
Register Name: DMA Transfer Count Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 1 transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: D6h (DMA1)
Register Name: DMA Destination Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DDA[19:16]	R/W	High DMA 1 Destination Address. These bits are mapped to A[19:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

Register Offset: D4h (DMA1)
Register Name: DMA Destination Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 1 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: D2h (DMA1)
Register Name: DMA Source Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DSA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DSA[19:16]	R/W	High DMA 1 Source Address. These bits are mapped to A[19:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

Register Offset: D0h (DMA1)
Register Name: DMA Source Address Low Register
Reset Value : ——

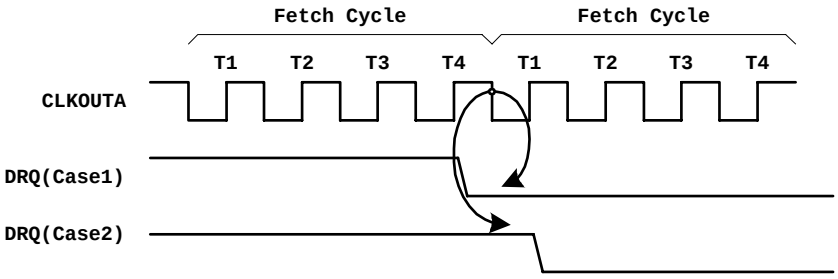
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 1 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA[19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

14.2 External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of SD_CLK. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. And no DMA acknowledge is provided, since the chip-selects (PCSx_n) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

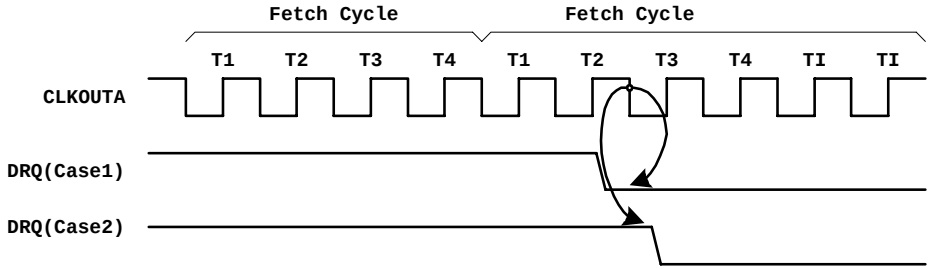
DMA transfer can be either source- or destination-synchronized, and it can also be unsynchronized. The Source-Synchronized Transfer figure shows the typical source-synchronized transfer, which provides the source device at least three clock cycles from the time it is acknowledged to dessert its DRQ line.



NOTES:
Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current source synchronized transfer will be immediately followed by antoher DMA transfer.

Source-Synchronized Transfers

The Destination-Synchronized Transfer figure shows the typical destination-synchronized transfer, which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



NETES:
Case1 : Current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current destination synchronized transfer will be immediately followed by another DMA transfer.

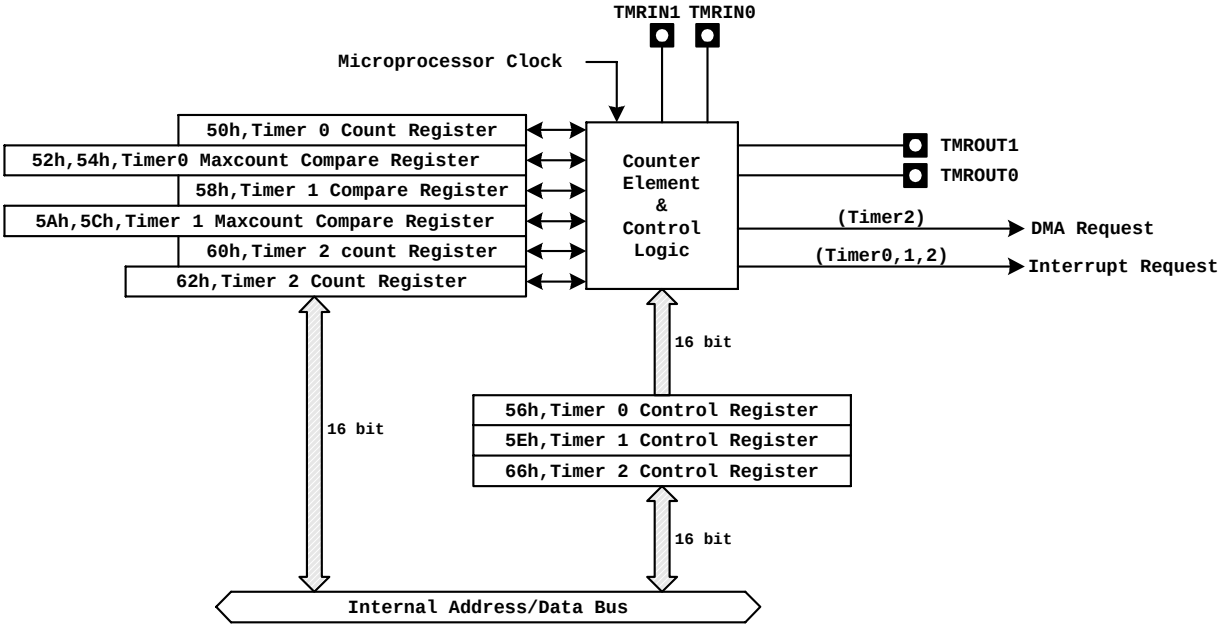
Destination-Synchronized Transfers

14.3 Serial Port/DMA Transfer

The serial port data can be DMA transfer to or from memory or I/O space. And the B_n/W bit of the DMA Control Register must be set to 0 for byte transfer. The map address of the Transmit Data Register is written to the DMA Destination Address Register and the memory or I/O address is written to the DMA Source Address Register, when the data are transmitted. The map address of the Receive Data Register is written to the DMA Source Address Register and the memory or I/O address is written to the DMA Destination Address Register, when the data are received.

The software is programmed through the Serial Port Control Register to perform the serial port/ DMA transfer. When a DMA channel is in use by a serial port, the corresponding external DMA request signal is deactivated. For DMA to the serial port, the DMA channel should be configured as being destination-synchronized. For DMA from the serial port, the DMA channel should be configured as source-synchronized.

15. Timer Control UNIT



Timer / Counter Unit Block

There are three 16-bit programmable timers in the EVA-X1610C. The timer operation is independent of the CPU. These three timers can be programmed as a timer element or as a counter element. Timer 0 and 1 are each connected to two external pins (TMRIN0, TMROUT0, TMRIN1, TMROUT1), which can be used to count or time external events, or used to generate variable-duty-cycle waveforms. Timer 2 is not connected any external pins. It can be used as a prescaler to Timer 0 and Timer 1 or as a DMA request source.

Register Offset: 56h
Register Name: Timer 0 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

These bit definitions for timer 0 are the same as those of register 5Eh for timer 1.

Register Offset: 50h
Register Name: Timer 0 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Count Value. This register contains the current count of Timer 0. The count is incremented by one every **8** internal processor clocks, or prescaled by Timer 2, or incremented by one every 8 external clock which is configured the external clock select bit to refer to the TMRIN1 signal.

Register Offset: 52h
Register Name: Timer 0 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare A Value.

Register Offset: 54h
Register Name: Timer 0 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare B Value.

Register Offset: 5Eh
Register Name: Timer 1 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: The timer 1 is enabled. Set 0: The timer 1 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n bit and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n bit and EN bit must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time the count reaches Max-Count A or Max-Count B. Set 0: Timer 1 will not issue interrupt request.
12	RIU	R/W	Register in Use Bit. Set 1: The Maxcount Compare B Register of timer 1 is being used. Set 0: The Maxcount Compare A Register of timer 1 is being used.
11-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set as each time either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the EN bit (offset 5Eh [15]).
4	RTG	R/W	Re-trigger Bit. This bit defines the control function by the input signal of TMRIN1 pin. When EXT=1 (5Eh.2), this bit is ignored. Set 1: Timer1 Count Register (58h) counts internal events; Reset the counting on every TMRIN1 input signal going from low to high (rising edge trigger). Set 0: Low input holds the timer 1 Count Register (58h) value; High input enables the counting which counts the internal events. **The definition of setting the (EXT, RTG)** (0 , 0) – Timer1 counts the internal events. If the TMRIN1 pin remains high. (0 , 1) -- Timer1 counts the internal events; count register resets on every rising transition on the TMRIN1 pin. (1 , x) -- TMRIN1 pin input acts as a clock source and timer1 count register is incremented by one every 8 external clocks.
3	P	R/W	Prescaler Bit. This bit and EXT bit (5Eh [2]) define the timer 1 clock source. **The definition of setting the (EXT, P)** (0 , 0) – Timer1 Count Register is incremented by one every 8 internal processor clocks. (0 , 1) – Timer1 Count Register is incremented by one which is prescaled by Timer 2. (1 , x) -- TMRIN1 pin input acts as a clock source and Timer1 Count Register is incremented by one every 8 external clocks.
2	EXT	R/W	External Clock Bit. Set 1: Timer 1 clock source from external.

			Set 0: Timer 1 clock source from internal.
1	ALT	R/W	Alternate Compare Bit. This bit controls whether the timer runs in single or dual maximum count mode. Set 1: Specify dual maximum count mode. In this mode, the timer counts to Maxcount Compare A, then resets the count register to 0. The timer counts to Maxcount Compare B, then resets the count register to 0 again, and starts over with Maxcount Compare A. Set 0: Specify single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and reset to 0, and then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer runs continuously. Set 0: The timer will halt after each counting to the maximum count and EN bit will be cleared.

Register Offset: 58h

Register Name: Timer 1 Count Register

Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every 8 internal processor clocks, prescaled by Timer 2, or incremented by one every 8 external clocks which is configured as the external clock select bit to refer to the TMRIN1 signal.

Register Offset: 5Ah

Register Name: Timer 1 Maxcount Compare A Register

Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare A Value.

Register Offset: 5Ch
Register Name: Timer 1 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare B Value.

Register Offset: 66h
Register Name: Timer 2 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: Timer 2 is enabled. Set 0: Timer 2 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n and EN bit must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. Set 0: Timer 2 will not issue interrupt request.
12-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the EN bit (66h.15).
4-1	Rsvd	RO	Reserved
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer is continuously running when it reaches the maximum count. Set 0: The EN bit (66h [15]) is cleared and the timer is held after each timer count reaches the maximum count.

Register Offset: 60h
Register Name: Timer 2 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Count Value. This register contains the current count of Timer 2. The count is incremented by one every 8 internal processor clocks.

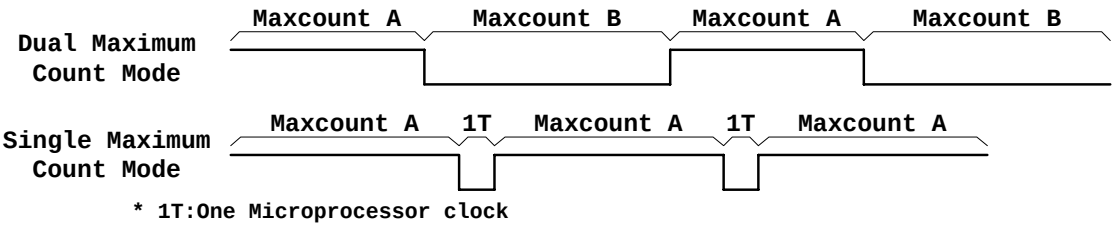
Register Offset: 62h
Register Name: Timer 2 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Compare A Value.

15.1 Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count values. Timer 2 can use only one maximum count value. Timer 0 and Timer1 can be configured to be a single or dual maximum count mode, the TMROUT0 or TMROUT1 signals can be used to generate waveforms of various duty cycles.



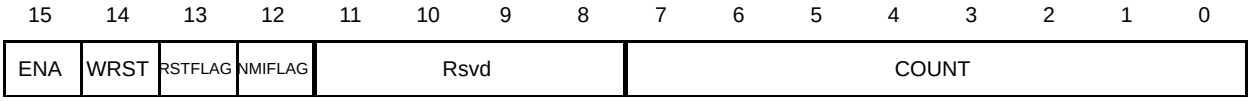
Timer/Counter Unit Output Modes

15.2 Watchdog Timer

The EVA-X1610C has one independent watchdog timer, which is programmable. **The watchdog timer is active after reset** and the timeout count with a maximum count value. The keyed sequence (3333h, CCCCh) must be written to the register (E6h) first, then the new configuration to the Watchdog Timer Control Register. It is a single write, so every writing to the Watchdog Timer Control Register must follow this rule.

When the watchdog timer activates, an internal counter is counting. If this internal count is over the watchdog timer duration, the watchdog timeout happens. The keyed sequence (AAAAh, 5555h) must be written to the register (E6h) to reset the internal count and prevent the watchdog timeout. The internal count should be reset before the Watchdog Timer timeout period is modified to ensure that an immediate timeout will not occur.

Register Offset: E6h
Register Name: Watchdog Timer Control Register
Reset Value : C080h



Bit	Name	Attribute	Description
15	ENA	R/W	Enable Watchdog Timer. Set 1: Enable Watchdog Timer. Set 0: Disable Watchdog Timer.
14	WRST	R/W	Watchdog Reset. Set 1: WDT generates a chip's internal reset when WDT timeout count is reached. Set 0: WDT generates an NMI interrupt when WDT timeout count is reached if the NMIFLAG bit is 0. If the NMIFLAG bit is 1, the WDT will generate a chip's internal reset when timeout.
13	RSTFLAG	R/W	Reset Flag. When watchdog timer reset event has occurred, hardware will set this bit to 1. This bit will be cleared by any keyed sequence write to this register or external reset. This bit is 0 after an external reset or 1 after a watchdog timer reset.
12	NMIFLAG	R/W	NMI Status Flag Value = 1: WDT generates a chip's internal reset when WRST (Bit 14) equals to 0 and WDT timeout count is reached. Value = 0: WDT generates an NMI interrupt and this bit will be set to 1 when WRST (Bit 14) equals to 0 and timeout counter is reached. This bit can't be set by software. After WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequence written to this register.
11-8	Rsvd	RO	Reserved

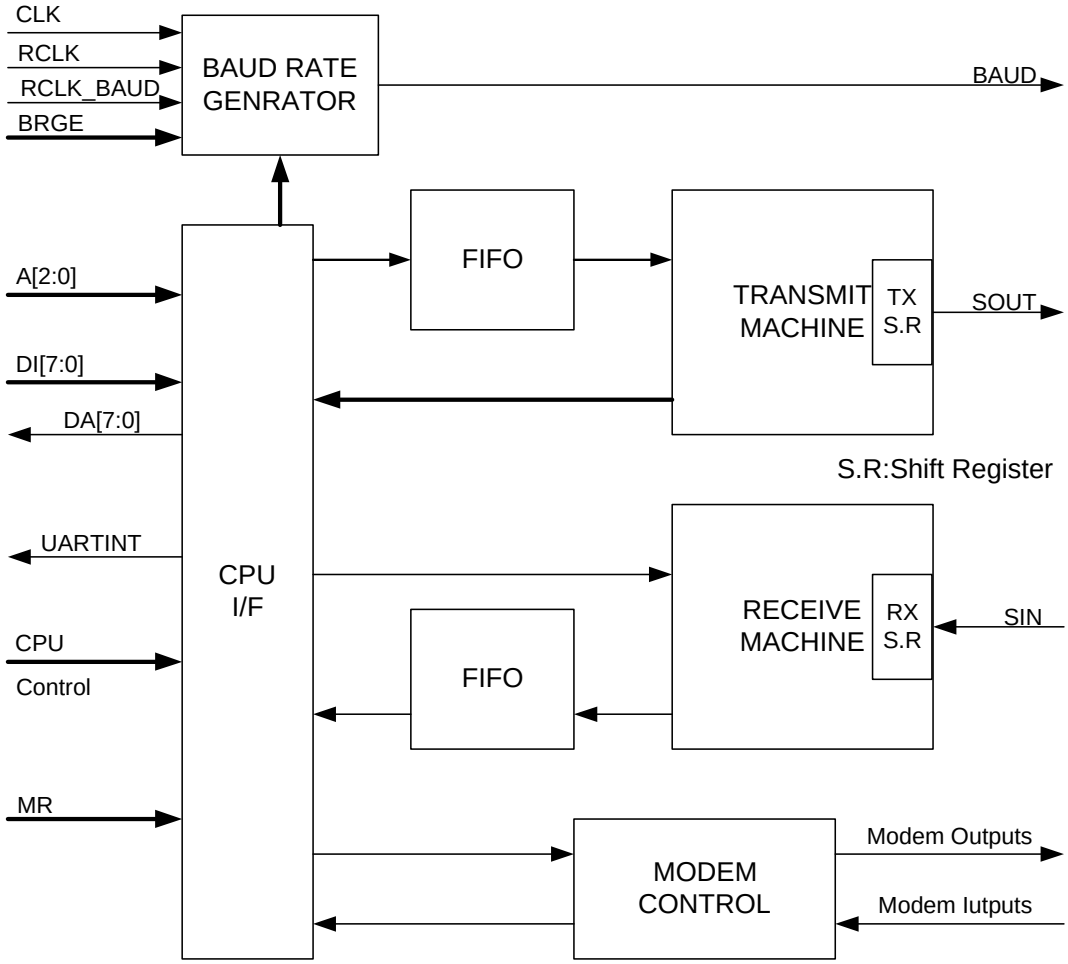
<table>
<tr>
<td>7-0</td>
<td>COUNT</td>
<td>R/W</td>
<td>Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.
a. The duration equation: Duration =(2^{Exponent}) / (Frequency/2)
b. The Exponent of the COUNT setting:
(Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, Bit 0) = (Exponent)
(0 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (N/A)
(x , x , x , x, x , x , x , 1) = (10)
(x , x , x , x, x , x , 1 , 0) = (20)
(x , x , x , x, x , 1 , 0 , 0) = (21)
(x , x , x , x, 1 , 0 , 0 , 0) = (22)
(x , x , x , 1, 0 , 0 , 0 , 0) = (23)
(x , x , 1 , 0, 0 , 0 , 0 , 0) = (24)
(x , 1 , 0 , 0, 0 , 0 , 0 , 0) = (25)
(1 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (26)
c. Watchdog timer Duration reference table:
For example: System clock =100Mhz and frequency exponent=10, then
Duration = 2^{10} / (100Mhz / 2) = 2048 / 100Mhz = 20.48 us
<table>
<tr><th>Frequency\ Exponent</th><th>10</th><th>20</th><th>21</th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th></tr>
<tr><td>75 MHz</td><td>27.3 us</td><td>28 ms</td><td>55.9 ms</td><td>111.8 ms</td><td>223.7 ms</td><td>447.4 ms</td><td>894.8 ms</td><td>1.79 s</td></tr>
<tr><td>100 MHz</td><td>20.5 us</td><td>21 ms</td><td>41.9 ms</td><td>83.9 ms</td><td>167.8 ms</td><td>335.5 ms</td><td>671 ms</td><td>1.34 s</td></tr>
</table>
</td>
</tr>
</table>

16. 16550 UART Serial Port

The system programmer may access any of the UART registers summarized in the following Table via the CPU. These registers control the UART operation in which the transmission and reception of data and status are included, and each register bit in the Table has its own name.

Register Address	Register Name	Mnem.	Bit No.									Note.
			15-8	7	6	5	4	3	2	1	0	
80h/10h	Receiver Buffer Register	**RBR**	0	RBR[7]	RBR[6]	RBR[5]	RBR[4]	RBR[3]	RBR[2]	RBR[1]	RBR[0]	DLAB=0 & read only
	Transmitter Holding Register	**THR**	0	THR[7]	THR[6]	THR[5]	THR[4]	THR[3]	THR[2]	THR[1]	THR[0]	DLAB=0 & write only
	Divisor Latch(LS)	**DLL**	0	DL[7]	DL[6]	DL[4]	DL[4]	DL[3]	DL[2]	DL[1]	DL[0]	DLAB=1
82h/12h	Interrupt Enable Register	**IER**	0	0	0	0	0	EMSI	ERLSI	ETHREI	ERDAI	DLAB=0
	Divisor Latch(MS)	**DLM**	0	DL[15]	DL[14]	DL[13]	DL[12]	DL[11]	DL[10]	DL[9]	DL[8]	DLAB=1
84h/14h	Interrupt Identified Register	**IIR**	0	FIFO Enabled (Note)	FIFO Enabled (Note)	0	0	IID[2]	IID[1]	IID[0]	IP	Read Only
	FIFO Control Register	**FCR**	DMACTL2-0	RCVR Trigger Level (MSB)	RCVR Trigger Level (LSB)	Reserved	Reserved	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled	Write Only
86h/16h	Line Control Register	**LCR**	0	DLAB	SB	SP	EPS	PEN	STB	WLS[1]	WLS[0]	
88h/18h	MODEM Control Register	**MCR**	0	0	0	0	Loop	LDCD	LRI	RTS	DTR	
8Ah/1Ah	Line Status Register	**LSR**	0	Error in RCVR FIFO (Note)	TEMT	THRE	BI	FE	PE	OE	DR	
8Ch/1Ch	MODEM Status Register	**MSR**	0	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS	
8Eh/1Eh	Scratch Register	**SCR**	0	SCR[7]	SCR[6]	SCR[5]	SCR[4]	SCR[3]	SCR[2]	SCR[1]	SCR[0]	

Note: These bits are always 0 in the 16450 mode.



UART Block Diagram

16.1 Receiver Buffer Register and Transmitter Holding Register

Register Offset: 80h
Register Name: UART0 Receiver Buffer Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								RBR [7:0]							

This register is Receiver Buffer Register when DLAB=0 and the read function is operated.

Register Offset: 80h
Register Name: UART0 Transmitter Holding Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								THR [7:0]							

This register is Transmitter Holding Register when DLAB=0 and the write function is operated.

16.2 Divisor Latch LS and MS Register

The divisor value, DLL[15:0], is the host clock / 16 / Baud Rate.

For example:

Host Clock=75Mhz, and Baud Rate=57600, then

Divisor=75Mhz/16/57600=81.3 ➔ 81

Register Offset: 80h
Register Name: UART0 Divisor Latch (LS) Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [7:0]							

This register is Divisor Latch (LS) Register when DLAB=1.

Register Offset: 82h
Register Name: UART0 Divisor Latch (MS) Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [15:8]							

This register is Divisor Latch (MS) Register when DLAB=1.

16.3 Interrupt Enable Register

This Interrupt Enable Register (IER) enables the four types of UART interrupts. Each interrupt can individually activate the interrupt output signal (UARTINT). It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, setting the relative bit of the IER register to 1 will enable the selected interrupt(s). Disabling an interrupt prevents it from being indicated as being active in the IIR and from activating the UARTINT output signal. All other system functions operate in their normal manners, including the setting of the Line Status and MODEM Status Registers. The details of each bit for the IER are described as below:

Register Offset: 82h
Register Name: UART0 Interrupt Enable Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	BMSI	ERLSI	ETHREI	ERDAI

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved and always 0.
3	EMSI	R/W	The MODEM Status Interrupt bit. Set to 1 to enable the MODEM Status Interrupt.
2	ERLSI	R/W	The Enable Receiver Line Status Interrupt bit. Set to 1 to enable the Receiver Line Status Interrupt.
1	ETHREI	R/W	The Enable Transmitter Holding Register Empty Interrupt bit. Set to 1 to enable the Transmitter Holding Register Empty Interrupt.
0	ERDAI	R/W	The Enable Received Data Interrupt bit. Set to 1 to enable the Received Data Available Interrupt (and timeout interrupts in the FIFO mode).

16.4 Interrupt Identification Register

This is a read only register. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register (IIR). The four levels of interrupt conditions in priority order are Receiver Line Status, Received Data Ready, Transmitter Holding Register Empty, and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. The details of each bit of Interrupt Identification Register are described as below.

Register Offset: 84h
Register Name: UART0 Interrupt Ident. Register (Read Only)
Reset Value : XX01h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								FIFOs Enabled	FIFOs Enabled	0	0	IID2	IID1	IID0	IP

Bit	Name	Attribute	Description
7-6	FIFOs Enabled	R/W	These two bits are set when FCR [0]=1.
5-4	Rsvd	RO	Reserved and always 0.
3	IID2	R/W	The Interrupt ID indicator. In the NS16450 Mode, this bit is 0. In the FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
2-1	IID[1:0]	R/W	The Interrupt ID indicator. These two bits are used to identify the highest priority interrupt pending as indicated in the following table:
0	IP	R/W	The Interrupt Pending indicator**.** This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending or not. Set 1: Indicate that no interrupt is pending. Set 0: Indicate that an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

Interrupt Control Function:

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Rest Control
0	0	0	1	—	None	none	—
0	1	1	0	Highest	Receiver Line Status	overrun error, parity error, framing error, or break interrupt	reading the line status register
0	1	0	0	Second	Received Data Available	received data available or trigger level reached	reading the receiver buffer register or the FIFO dropping below the trigger level
1	1	0	0	Second	Character Timeout Indication	no character has been removed from or input to the RCVR FIFO during the last 4 characters times and there is at least 1 character in it during this time	reading the receiver buffer register
0	0	1	0	Third	Transmitter Holding Register Empty	transmitter holding register empty	reading the IIR register (if the source of interrupt is available) or writing into the

							transmitter holding register
0	0	0	0	Fourth	MODEM Status	clear to send, data set ready, ring indicator, or data carrier detect	reading the modem status register

16.5 FIFO Control Register

The FIFO Control Register (write only) is at the same location as the Interrupt Identification Register (read only). This register is used to enable the FIFO, clear the FIFO, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Register Offset: 84h
Register Name: UART0 FIFO Control Register (Write Only)
Reset Value : X000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					DMACTL[2:0]			RCVR Trigger (MSB)	RCVR Trigger (LSB)	Rsvd		DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled

Bit	Name	Attribute	Description
10-8	DMACTL [2:0]	R/W	With the DMA transfers listed as follows, users can configure these bits for UART Port. **DMACTL [2:0] --- Receive --- Transmit** (0, 0, 0) --- No DMA --- No DMA (0, 0, 1) --- DMA 0 --- DMA 1 (0, 1, 0) --- DMA 1 --- DMA 0 (0, 1, 1) --- Reserved --- Reserved (1, 0, 0) --- DMA 0 --- No DMA (1, 0, 1) --- DMA 1 --- No DMA (1, 1, 0) --- No DMA --- DMA 0 (1, 1, 1) --- No DMA --- DMA 1
7-6	RCVRTL [1:0]	R/W	RCVR Trigger. These two bits are used to set the trigger level for the RCVR FIFO interrupt. **RCVRTL[1:0] – RCVR FIFO Trigger Level (Bytes)** 0 0 -- 01 Bytes 0 1 -- 04 Bytes 1 0 -- 08 Bytes 1 1 -- 14 Bytes
5-4	Rsvd	RO	Reserved
3	DMA Mode Select	R/W	DMA Mode Select. Setting FCR0[3]=1 will cause the UART to change from mode 0 to mode 1 if FCR0[0]=0.
2	XMIT FIFO	R/W	XMIT FIFO Reset. Writing a 1 to FCR0[2] clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to

	Reset		this bit position is self-clearing.
1	RCVR FIFO Reset	R/W	RCVR FIFO Reset. Writing a 1 to FCR0[1] clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
0	FIFO Enabled	R/W	FIFO Enable. Writing a 1 to FCR0 enables both the XMIT and RCVR FIFO. Resetting FCR0[0] will clear all bytes in both FIFO. When changing from FIFO Mode to NS16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when written to other FCR bits or they will not be programmed.

16.6 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The detailed contents of each bit of LCR register is as follows:

Register Offset: 86h
Register Name: UART0 Line Control Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLAB	Set Break	Stick Parity	EPS	PEN	STB	WSL1	WSL0

Bit	Name	Attribute	Description
7	DLAB	RW	Divisor Latch Access bit. Set 1: To access the Divisor Latches of the Baud Generator during a Read or Write operation. Set 0: To access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register
6	SB	R/W	Break Control bit. It causes a break condition to be transmitted to the receiving UART. Set 1: the serial output (SOUT) is forced to the Spacing (logic 0) state. Set 0: the Break is disabled. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. ***Note:*** *This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.* *1.Load an all Os, pad character, in response to THRE.* *2.Set break after the next THRE.* *3.Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.*

			During the break, the Transmitter can be used as a character timer to accurately establish the break duration.
5	SP	R/W	Stick Parity bit. Set Bit 5=1, Bit 4=1, & Bit 3=1, the Parity bit is transmitted and checked as logic 0. Set Bit 5=1, Bit 4=0, & Bit 3=1, the Parity bit is transmitted and checked as logic 1. Set Bit 5=0, Stick Parity is disabled.
4	EPS	R/W	Even Parity Select bit. Set Bit 4=0 & Bit 3=1, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. Set Bit 4=1 & Bit 3=1, an even number of logic 1s is transmitted or checked.
3	PEN	R/W	Parity Enable bit. Set 1: A Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)
2	STB	R/W	Stop bit. This bit specifies the number of Stop bits transmitted and received in each serial character. Set 0: One Stop bit is generated in the transmitted data. Set 1: One and a half stop bits are generated for a 5-bit word length characters. Two stop bits are generated for either 6-, 7-, or 8-bit word length characters. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
1-0	WLS[1:0]	R/W	These two specify the number of bits in each transmitted or received serial character. **WLS[1:0] -- Character Length** 0 0 -- 5 bits character 0 1 -- 6 bits character 1 0 -- 7 bits character 1 1 -- 8 bits character

16.7 Modem Control Register

This Modem Control Register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The details are described as below:

Register Offset: 88h
Register Name: UART0 MODEM Control Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	Loop	LDCD	LRI	RTS	DTR

Bit	Name	Attribute	Description
7-5	Rsvd	RO	Reserved and always 0.
4	Loop	R/W	This bit provides a local loop back feature for diagnostic testing of the UART. Set to 1, the following occur:

			The transmitter Serial Output (SOUT) is set to the Marking (logic 1) state. The receiver Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input. The four MODEM Control inputs (CTS_n, DSR_n, RI_n, and DCD_n) are disconnected, and the 2 MODEM Control outputs (DTR_n and RTS_n) are internally connected to the two MODEM Control inputs (DSR_n, CTS_n), and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted are immediately received. This feature allows the processor to verify the transmitted and received data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the sources of the interrupts are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
3, 2	LDCD, LRI	R/W	Bit3: The bit controls DCD_n signal internal if loopback mode is enabled. Bit2: The bit controls RI_n signal internal if loopback mode is enabled.
1	RTS	R/W	The Request To Send bit. This bit controls the Request To Send (RTS_n) output. Set 1: the RTS_n output is forced to logic 0. Set 0: the RTS_n output is forced to logic 1.
0	DTR	R/W	The Data Terminal Ready indicator. This bit controls the Data Terminal Ready (DTR_n) output. Set 1: the DTR_n output is forced to logic 0. Set 0: the DTR_n output is forced to logic 1. ***Note:*** *The DTR_n output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.*

16.8 Line Status Register

This register provides status information to the part of the CPU processing data transfer. The contents of each Bit of the Line Status Register are described as below.

Register Offset: 8Ah
Register Name: UART0 Line Status Register
Reset Value : XX60h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Error in RCVR (Note 2)	TEMT	THRE	BI	FE	PE	OE	DR

Bit	Name	Attribute	Description
7	Error in RCVR (Note 2)	R/W	Error in Receive FIFO. In the NS16450 Mode, this is a 0. In the FIFO mode, LSR [7] is set to 1 when there is at least one parity error, framing error or break indication in the FIFO. LSR [7] is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO. ***Note:*** *The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.*
6	TEMT	R/W	The Transmitter Empty indicator. Set 1: This bit is set to 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty.

			Set 0: This bit is reset to 0 whenever either the Transmitter Holding Register or the Transmitter Shift Register contains a data character. In the FIFO mode, this bit is set to one whenever the transmitter FIFO and shift register are both empty.
5	THRE	R/W	The Transmitter Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt Enable is set high. Set 1: This bit will be set to 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. Set 0: This bit is reset to 0 upon the CPU loading character to the Transmitter Holding Register. In the FIFO mode, this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.
4	BI	R/W	Break Interrupt indicator. Set 1: This bit will be set to 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + Data Bits + Parity Bit + Stop Bit). Set 0: This bit will be reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit. ***Note:*** *Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.*
3	FE	R/W	Framing Error indicator. This bit indicates that the received characters don't have a valid Stop Bit. Set 1: This bit will be set to 1 whenever the Stop Bit follows the last data bit or Parity bit is detected as a logic 0 bit (Spacing level). Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error occurs. To do this, it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".
2	PE	R/W	Parity Error indicator. This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit. Set 1: This bit will be set upon detection of a parity error. Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.
1	OE	R/W	Overrun Error indicator. This bit indicates that the data in the Receiver Buffer Register were not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. Set 1: Indicate OE indicator is set to logic 1 upon detection of an overrun condition. Set 0: Automatic reset to 0 whenever the CPU reads the contents of the Line Status

			Register. If the data in the FIFO mode continue to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
0	DR	R/W	Data Ready indicator. Set 1: Indicate whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Set 0: Automatic set to 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

16.9 Modem Status Register

This Modem Status Register (MSR) provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to logic 1 whenever a control input from the MODEM changes its state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register. The contents of the MSR register are described as below.

Register Offset: 8C
Register Name: UART0 MODEM Status Register
Reset Value : XXX0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

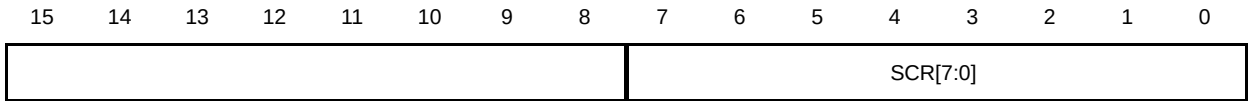
Bit	Name	Attribute	Description
7	DCD	R/W	Data Carrier Detect. This bit is the complement of the Data Carrier Detect (DCD_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT2 in the MCR.
6	RI	R/W	Ring Indicator. This bit is the complement of the Ring Indicator (RI_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	DSR	R/W	Data Set Ready. This bit is the complement of the Data Set Ready (DSR_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	CTS	R/W	Clear To Send. This bit is the complement of the Clear to Send (CTS_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	DDCD	R/W	Delta Data Carrier Detect. This bit indicates that the DCD_n input has changed the state. ***Note:*** *Whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status Interrupt is generated.*
2	TERI	R/W	Trailing Edge Ring Indicator. This bit indicates that the RI_n input has changed from a low to a high state.

1	DDSR	R/W	Delta Data Set Ready. This bit indicates that the DSR_n input has changed the state since the last time it was read by the CPU.
0	DCTS	R/W	Delta Clear To Send. This bit indicates that the CTS_n input has changed the state since the last time it was read by the CPU.

16.10 Scratchpad Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Register Offset: 8E
Register Name: UART0 Scratch Register
Reset Value : ——



16.11 Programmable Baud Generator

The UART contains a programmable Baud Generator that is divided by any divisor from 2 to 2^{16}-1.. The output frequency of the Baud Generator is 16 times the Baud [divisor # = (CPU frequency)/(baud rate*16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Baud Rates	CPUCLK=75MHz				CPUCLK=100MHz			
	DLM	DLL	Baud	Dev.(%)	DLM	DLL	Baud	Dev.(%)
1200	0Fh	42h	1200	0	14h	58h	1200	0
2400	07h	A1h	2400	0	0Ah	2Ch	2400	0
4800	03h	D1h	4798	0.04	05h	16h	4800	0
9600	01h	E8h	9606	0.06	02h	8Bh	9601	0
19200	0h	F4h	19211	0.06	01h	46h	19171	0.15
38400	0h	7Ah	38422	0.06	0h	A3h	38344	0.15
57600	0h	51h	57870	0.5	0h	6Dh	57339	0.45
115200	0h	29h	114329	0.76	0h	36h	115741	0.47
230400	0h	14h	234375	1.73	0h	1Bh	231481	0.47
460860	0h	0Ah	468750	1.71	0h	0Eh	446428	3.13

16.12 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR [0]=1, IER [0]=1), RCVR interrupt will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
C. The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.
D. The data ready bit (LSR [0]) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:
   —at least one character is in the FIFO.
   —the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
   —the most recent CPU read of the FIFO was longer than 4 continuous character times ago.
   This will cause a maximum character received to interrupt issued delay of 160 ms at 300 BAUD with a 12-bit character.
B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
C. When a timeout interrupt has occurred: It is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
D. When a timeout interrupt has not occurred: The timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR [0]=1, IER [1]=1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data

available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

16.13 FIFO Polled Mode Operation

With FCR [0]=1, resetting IER [0], IER [1], IER [2], IER [3] or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR [0] will be set as long as there is one byte in the RCVR FIFO.

LSR [1] to LSR [4] will specify which error(s) has occurred.

Character error status is handled the same way as in the interrupt mode, the IIR is not affected since IER2=0.

LSR [5] will indicate when the XMIT FIFO is empty.

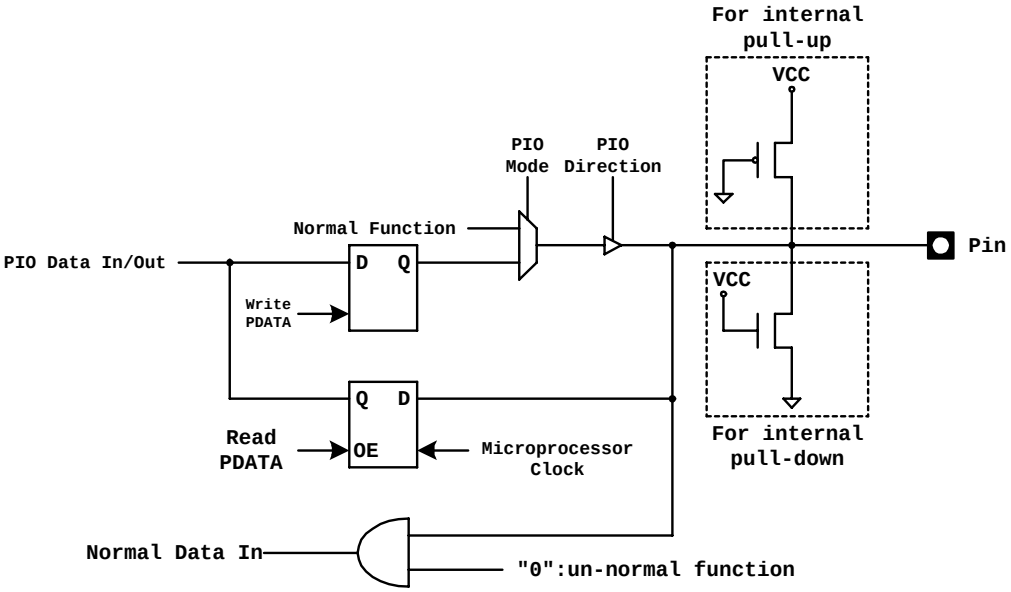
LSR [6] will indicate that both the XMIT FIFO and Shift Register are empty.

LSR [7] will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

17. PIO UNIT

The EVA-X1610C provides 32 programmable I/O signals, which are multi-functional pins with other signals of normal functions. Software must be used to configure these multi-functional pins as PIOs or normal functions by means of programming through these registers (7Ah, 78h, 76h, 74h, 72h, and 70h).



PIO pin Operation Diagram

17.1 PIO Multi-Functional Pins List Table

PIO No.	Pin No.(PQFP)	Multi Function	Reset status/PIO internal resister
0	9	TMRIN1	PIO/ Input with 75K pull-up
1	11	TMROUT1	PIO/ Input with 75K pull-down
3	124	PCS5_n	PIO/ Input with 75K pull-up
7	46	A17/SAD6	Normal operation/ Input with 75K pull-up
8	44	A18/SAD7	Normal operation/ Input with 75K pull-up
9	43	A19/ALE	Normal operation/ Input with 75K pull-up
10	12	TMROUT0	PIO/ Input with 75K pull-down
11	10	TMRIN0	PIO/ Input with 75K pull-up
12	14	DRQ0/INT5	PIO/ Input with 75K pull-up
13	13	DRQ1/INT6	PIO/ Input with 75K pull-up
14	126	PCS0_n	PIO/ Input with 75K pull-up
15	125	PCS1_n	PIO/ Input with 75K pull-up
25	34	PCS2_n	PIO/ Input with 75K pull-up
26	35	PCS3_n	PIO/ Input with 75K pull-up
27	39		PIO/ Input with 75K pull-up
28	41		PIO/ Input with 75K pull-up
29	42	UARTX0	PIO/ Input with 75K pull-down
31	5	INT2/INTA0_n	PIO/ Input with 75K pull-up

PIO Mode	PIO Direction	Pin Function
0	0	Normal Operation
0	1	PIO input with pull-up/pull-down
1	0	PIO output
1	1	PIO input without pull-up/pull-down

Register Offset: 7Ah
Register Name: PIO Data 1 Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA [31:16]															

Bit	Name	Attribute	Description
15-0	PDATA [31:16]	R/W	PIO Data Bits. These bits PDATA[31:16] are mapped to the PIO[31:16], which indicate to the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 78h
Register Name: PIO Direction 1 Register
Reset Value : FF9Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR [31:16]															

Bit	Name	Attribute	Description
15-0	PDIR[31:16]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

Register Offset: 76h
Register Name: PIO Mode 1 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE [31:16]															

Bit	Name	Attribute	Description
15-0	PMODE [31:16]	R/W	PIO Mode Bit. The definitions of PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually. The definitions (PIO Mode, PIO Direction) for the functions of PIO pins: (0 , 0) – Normal operation , (0 , 1) – PIO input with pull-up/pull-down (1 , 0) – PIO output , (1 , 1) -- PIO input without pull-up/pull-down

---

Register Offset: 74h
Register Name: PIO Data 0 Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA [15: 0]															

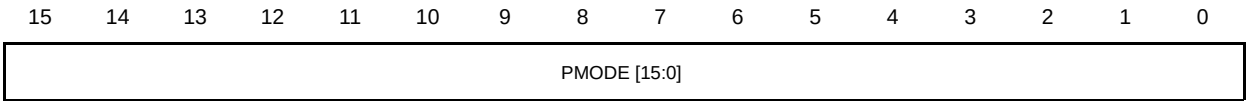
Bit	Name	Attribute	Description
15-0	PDATA [15:0]	R/W	PIO Data Bus. These bits PDATA[15:0] are mapped to the PIO[15:0], which indicate to the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 72h
Register Name: PIO Direction 0 Register
Reset Value : FC4Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR [15:0]															

Bit	Name	Attribute	Description
15-0	PDIR[15:0]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

Register Offset: 70h
Register Name: PIO Mode 0 Register
Reset Value : 0000h



Bit	Name	Attribute	Description
15-0	PMODE[15:0]	R/W	PIO Mode Bus.

18. SDRAM Controller

18.1 SDRAM Arbiter Control Register

Register Offset: F0h
Register Name: SDRAM Arbiter Control Register
Reset Value : 00C0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RWIR	IFBE	WFE	RC[4:0]				

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	RWIR	R/W	Read/Write Instruction Re-order. If the write and read data instructions were relative, the read instructions could be read first.
6	IFBE	R/W	Instruction Fetch Burst Enable. Setting this bit will cause code fetch in burst mode. (Default is 0)
5	WFE	R/W	Write FIFO Enable. Setting this bit will enable the Post-Write function. The 'IN' or 'OUT' instruction must be executed prior to each DMA moved data. **Don't enable the function if DAM was control by Timer2 or DRQs' pin.**
4-0	RC[4:0]	R/W	Refresh Priority Counter.

Note. The suggestion value is 0021h, which means enabling the R/W reorder and the code pre-fetch.

18.2 SDRAM Mode Set Register

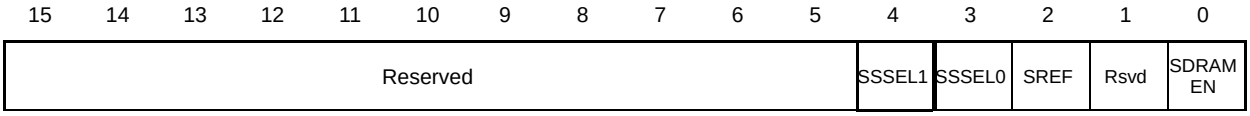
Register Offset: F2h
Register Name: SDRAM Mode Set Register
Reset Value : 0020h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								0	LAT [2:0]			0	BL [2:0]		

Bit	Name	Attribute	Description
15-7	Rsvd	RO	Reserved
6-4	LAT[2:0]	R/W	CAS_n Latency Select. Refer to the following table: **LAT [2:0]** — **CAS_n Latency** 0 0 0 — Reserved 0 0 1 — Reserved 0 1 0 — 2 (Default) 0 1 1 — 3 1 0 0 — Reserved 1 0 1 — Reserved 1 1 0 — Reserved
3	Rsvd	RO	1’b0.
2-0	BL[2:0]	RO	Burst Length.

18.3 SDRAM Control Register

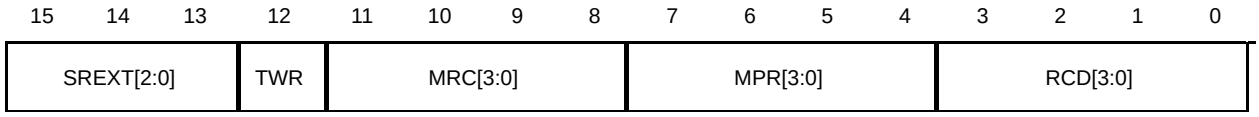
Register Offset: F4h
Register Name: SDRAM Control Register
Reset Value : 0001h



Bit	Name	Attribute	Description
15-5	Rsvd	RO	Reserved
4-3	SSSEL[1:0]	R/W	The SDRAM Size Select bit. (Default is 2'b0) **SSEL[1:0] -------- SDRAM Size Select** 0 0 -------- 1Mx16 bits 0 1 -------- 4Mx16 bits 1 0 -------- Reserved 1 1 -------- Reserved
2	SREF	R/W	Self-Refresh Enable. Set 1: Enable Self-Refreshed when SDRAM is in power mode. Set 0: Disable Self-Refreshed. (Default)
1	Rsvd	RO	Reserved
0	SDRAMEN	R/W	SDRAM Enable. Set 1: Enable SDRAM. (Default) Set 0: Disable SDRAM.

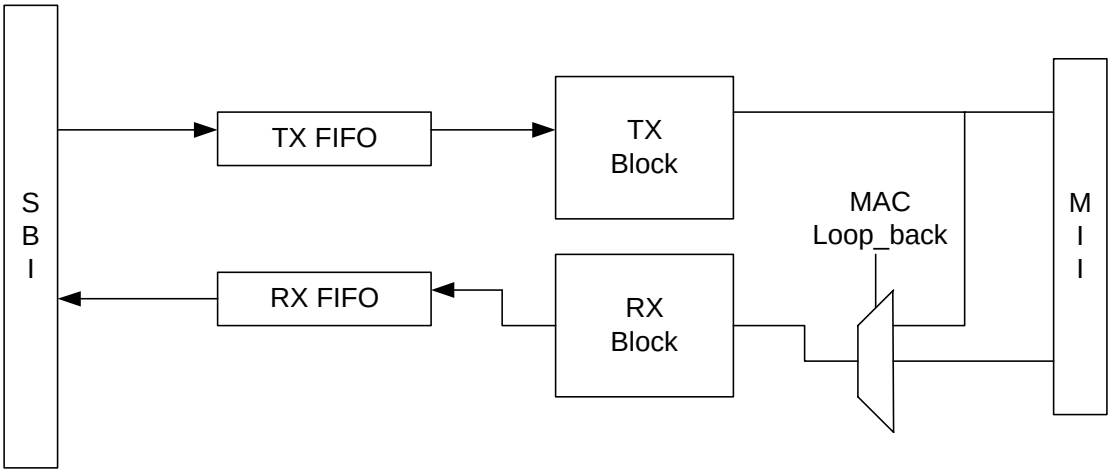
18.4 SDRAM Timing Parameter Register

Register Offset: F6h
Register Name: SDRAM Timing Parameter Register
Reset Value : F933h



Bit	Name	Attribute	Description
15-13	SREXT[2:0]	R/W	Self-Refresh Exit Time (t_{SREX}). The Self-Refresh Exit Time can be programmed from 0 to 15 Clocks.
12	TWR	R/W	Write Recovery Time. 1: 1 Clock cycle. 0: 2 Clocks cycle.
11-8	MRC[3:0]	R/W	Min Row Cycle Time (t_{RC},). It can be programmed from 0 to 15 Clocks.
7-4	MPR[3:0]	R/W	Min Pre-charge Time (t_{RP},). It can be programmed from 0 to 15 Clocks.
3-0	RCD[3:0]	R/W	Row to Column Delay time ($t_{RCD)}$. It can be programmed from 0 to 15 Clocks.

19. Fast Ethernet Controller



SBI : System Bus Interface

MAC Block Diagram

19.1 RX Descriptor Format

15														3	2	1	0
O	DRST [14:0]																
DRLEN [15:0]																	
DRBP [15:2]																0	0
DRBP [19:16]																	
DRNX[15:2]																0	0
DRNX [19:16]																	
Reserve1																	
Reserve2																	
Reserve3																	

1. **O: Owner Bit.** Set 1: MAC. Set 0: CPU.
2. **DRST [14:0]:** RX Status. The MAC will update the RX status field after frame receiving is completed.

   DRST [14]: **RXOK,** RX successful. This bit indicates that the packet was received successfully without error. It includes:

   (1) RX_ER = 0 (MII interface).

   (2) Ignore DRIBBLE status.

   (3) No over buffer length.

   (4) Without CRC errors.

   (5) Not a LONG packet.

   (6) Not a RUNT packet.

   (7) No FIFO Full.

DRST [13]: Reserved.

DRST [12]: Reserved.

DRST [11]: **PHYERR,** PHY RX Error packet. Read 1 means that an error occurred in receiving packets on MII interface.

DRST [10]: **DRIBBLE**, Dribble packet. Read 1 means the received packet is a dribble packet.

DRST [9]: **OBL**, Over Buffer Length. Read 1 means the received packet length > buffer maximum length.

DRST [8]: **LONG**, Long packet. Read 1 means the received packet length > maximum packet length.

DRST [7]: **RUNT**, Runt packet. Read 1 means the received packet length < 64 Bytes.

DRST [6]: **CRCERR**, CRC Error packet. Read 1 means receiving a packet with CRC errors.

DRST [5]: **BROADCAST,** indicate that the received packet is a broadcast packet.

DRST [4]: **MULTICAST,** indicate that the received packet is a multicast packet.

DRST [3]: **MCH**, Multicast Hit. Indicate that the received packet hits one of the hash-table bits.

DRST [2]: **MIDH**, MID table is hit.

DRST [1:0]: **MID,** index of matched MIDx. These two bits indicate that the received packet hits one of the MID groups.

3. **DRLEN [15:0]:** RX Length.

   DRLEN [15:11]: Reserved.

   DRLEN [10:0]: The size of the received frame.

4. **DRBP [19:0]:** RX Data Buffer Pointer. This is a 20-bit address pointer and DRBP [1:0] is always 2'b00.
5. **DRNX [19:0]:** RX Next Frame Descriptor Pointer. This is a 20-bit descriptor address pointer and DRNX [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.
6. The RX circuit will stop receiving packet if Owner Bit=0.
7. **Reserve1, 2, 3:** these fields were reserved and not used.

Note:

1. RX Descriptor start address and Data Buffer start address must be Double-Word alignment.
2. Hardware is needed to check RX Buffer Length Register; do not write the received data into a buffer over the buffer size.
3. The RX packet will be filter if its length less than 6. (Not complete DA information.)

19.2 TX Descriptor Format

15			3	2	1	0
O	DTST [14:0]					
DTLEN [15:0]						
DTBP [15:2]					0	0
DTBP [19:16]						
DTNP[15:2]					0	0
DTNP [19:16]						

1. **O: Owner Bit.** Set 1: MAC. Set 0: CPU.

2. **DTST [14:0]:** TX Status and packet control. The MAC will update the TX status field after frame transmission is completed. The control bit is for each packet usage.

   DTST [14]: **TXOK,** TX packet successful**.** This bit indicates that the packet was transmitted successfully without error. It includes:

   (1) No late collision.

   (2) No excessive collision.

   (3) No TX FIFO under-run.

   (4) No lost carrier.

   DTST [13]: **DISCRC**, Disable append CRC field. This is a control bit, =1 disables CRC append, =0 enables CRC append on TX packet. When the status is updated, this bit will keep in previous setting.

   DTST [12:7]: Reserved.

   DTST [6]: **TXFUR**, FIFO Under-Run.

   DTST [5]: **LATEC**, Late Collision.

   DTST [4]: **EXCEEDC**, Exceed Collision.

   DTST [3:0]: **COLCNT**, Collision Counts.

3. **DTLEN [15:0]:** TX Length.

   DTLEN [15:11]: Reserved.

   DTLEN [10:0]: The length of the transmitted packet.

4. **DTBP [19:0]:** TX Buffer Pointer. This is a 20-bit address pointer. Transmit buffer can be located at any byte alignment address.

5. **DTNP [19:0]:** TX Next Descriptor Pointer. This is a 20-bit descriptor address pointer and DTNP [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.

6. The TX circuit will stop transmitting packet if the Owner Bit=0.

Note:

1. TX Descriptor start address must be Double-Word alignment.
2. TX Data Buffer start address can be any byte alignment address.
3. Driver is needed to take care that the transmitted data are less than 60 bytes.

19.3 MCR0: MAC Control Register 0 (00h)

Register Offset: 00h
Register Name: MCR0: MAC Control Register 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULLD	TXEIE	Rsvd	XMTEN	Reserved		FCEN	AMCP	RXEIE	FBCP	PROM	ADRB	ALONG	ARUNT	ACRCER	RCVEN

Bit	Name	Attribute	Description
15	FULLD	R/W	Full Duplex. Set 1: Full duplex. Set 0: Half duplex. (Default)
14	TXEIE	R/W	TX Early Interrupts Enable. Set 1: MAC will generate one TX early interrupt when the data are transmitted over early interrupt threshold (see MCR1 [7:6]). Set 0: TX early interrupt will be disabled.
13	Rsvd	RO	Reserved
12	XMTEN	R/W	Transmission Enable
11-10	Rsvd	RO	Reserved
9	FCEN	R/W	Flow Control Function Enable. Set 1: will enable flow control. Set 0: will disable flow control.
8	AMCP	R/W	Accept Multicast Packet. Set 1: will enable hash table function. Set 0: will disable hash table function
7	RXEIE	R/W	RX Early Interrupts Enable. Set 1: MAC will generate one RX early interrupt when the data are received over early interrupt threshold (see MCR1 [7:6]). Set 0: RX early interrupt will be disabled.
6	FBCP	R/W	Filter Broadcast Packet. Set 1: to filter broadcast packet. Set 0: to accept broadcast packet.
5	PROM	R/W	Promiscuous Mode. Set 1: MAC will receive all packets without checking the MAC address. Set 0: MAC will only receives the packet that hits the MAC address.
4	ADRB	R/W	Accept DRIBBLE packet. Set 1: Enable to accept dribble packets. Set 0: Disable.
3	ALONG	R/W	Accept Long packet. Set 1: Enable to accept long packets. Set 0: Disable.
2	ARUNT	R/W	Accept RUNT packet. Set 1: Enable to accept runt packets. The packets which length > 6 and < 64 will be accepted, but the packets which length >0 and < 6 will be rejected. Set 0: Disable to accept runt packets.

1	ACRCER	R/W	Accept CRC Error packet. Set 1: Enable. Set 0: Disable.
0	RCVEN	R/W	Receive Enable. Set 1: Enable packet receive. Set 0: Disable packet receive.

19.4 MCR1: MAC Control Register 1 (04h)

Register Offset: 04h
Register Name: MCR1: MAC Control Register 1
Reset Value : 0010h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						TPF	ECR	EITH [1:0]		MAXLEN [1:0]		Reserved		LBM	MRST

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved
9	TPF	RO	Status for Trigger Pause Frame to be transmitted. Set 1 to transmit pause frame and MAC will keep sending until this bit is cleared. If flow control (FCEN bit in MCR0 [9]) is enabled, this bit will be set automatically when received descriptor unavailable happens. A driver is needed to clear this bit after descriptor is available again. TPF refers to the XMTEN bit (MCR0 [12]). When the XMTEN bit is set, the pause frame can be sent.
8	ECR	R/W	Excessive Collision Retransmit times. 0: 16 times. (Default) 1: 32 times.
7-6	EITH [1:0]	R/W	Early Interrupt Threshold. 00: 1129 bytes. (Default) 01: 1257 bytes. 10: 1385 bytes. 11: 1513 bytes.
5-4	MAXLEN [1:0]	R/W	Maximum Packet Length Selector. Define the length of long packets. 01: 1518 bytes. (Default) 10: 1522 bytes. 11: 1534 bytes. 00: 1537 bytes.
3-2	Rsvd	RO	Reserved. These two bits must be set to 0.
1	LBM	R/W	Loop-Back mode. 0: Normal Mode. (Default) 1: MAC Loop-Back.
0	MRST	R/W	MAC Reset. Set 1 to reset MAC. After reset, this bit will be cleared to 0.

19.5 MBCR: MAC Bus Control Register (08h)

Register Offset: 08h
Register Name: MBCR: MAC Bus Control Register
Reset Value : 1F1Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RHPT [4:0]					Reserved		RXFTH [1:0]		TXFTH [1:0]		FIFOTL [1:0]	

PS. Update this register only when RCVEN=0

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved
12-8	RHPT [4:0]	R/W	SDRAM Bus Request High Priority Timer. When MAC issues a bus request to SDRAM arbiter, this timer will start to count down. After this timer is timeout, if SDRAM arbiter is still not granted to MAC, the SDRAM bus request will become high priority. Wait time = 0 ~15 host clocks. (Default=15 host clocks)
7-6	Rsvd	RO	Reserved
5-4	RXFTH [1:0]	R/W	RX FIFO Data Threshold. MAC receive machine starts to move the received data into host memory when receiving data over the RX FIFO threshold. 00: 8 bytes. 01: 16 bytes. (Default) 10: 32 bytes. 11: 64 bytes.
3-2	TXFTH [1:0]	R/W	TX FIFO Data Threshold. MAC transmit machine starts to send out packets to PHY when transmitting data into TX FIFO over the threshold. 00: 16 bytes. 01: 32 bytes. 10: 64 bytes. (Default) 11: 96 bytes.
1-0	FIFOTL [1:0]	R/W	FIFO Transfer Length. The every transfer data length between MAC FIFO and SDRAM. 00: 4 bytes. 01: 8 bytes. 10: 16 bytes. (Default) 11: 32 bytes.

19.6 MTICR: TX Interrupt Control Register (0Ch)

Register Offset: 0Ch
Register Name: MTICR: TX Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXINTC [3:0]				Reserved		TXTIMER [5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	TXINTC [3:0]	R/W	TX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after sending N packets (1~15 packets).
7-6	Rsvd	RO	Reserved
5-0	TXTIMER [5:0]	R/W	Wait TX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: (63 + TXTIMER * 64) TX clock

19.7 MRICR: RX Interrupt Control Register (10h)

Register Offset: 10h
Register Name: MRICR: RX Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RXINTC [3:0]				Reserved		RXTIMER [5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	RXINTC [3:0]	R/W	RX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after N packets (1~15 packets) are received.
7-6	Rsvd	RO	Reserved
5-0	RXTIMER [5:0]	R/W	Wait RX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: (63 + RXTIMER * 64) RX clock

19.8 MTPR: TX Poll Command Register (14h)

Register Offset: 14h
Register Name: MTPR: TX Poll Command Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															TM2TX

Bit	Name	Attribute	Description
15-1	Rsvd	RO	Reserved
0	TM2TX	R/W	Trigger MAC to Transmit. When Write: Trigger MAC to check TX description owner bit. If owner bit=0, MAC will standby until the owner bit=1 to start transmission. When Read: TM2TX is current transmission status. When TM2TX= 1, it means MAC is in transmitting. When TM2TX= 0, it means transmission was completed.

19.9 MRBSR: RX Buffer Size Register (18h)

Register Offset: 18h
Register Name: MRBSR: RX Buffer Size Register
Reset Value : 0600h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RBSZ [10:0]										RBSZ[0]

PS. Update this register only when RCVEN=0

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10-1	RBSZ [10:0]	R/W	RX Buffer Size Bit10~Bit1 for all RX frame data buffer of Descriptors.
0	RBSZ [0]	R/W	RX Buffer Size Bit0 must be 0.

19.10 MRDCR: RX Descriptor Control Register (1Ah)

Register Offset: 1Ah
Register Name: MRDCR: RX Descriptor Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXPT [7:0]								RXDESPAN [7:0]							

Bit	Name	Attribute	Description
15-8	RXPT [7:0]	R/W	RX Descriptor Threshold value. MAC controller will send TX Pause Frame when available RX Descriptor reaches this threshold value.
7-0	RXDESPAN [7:0]	R/W	RX Descriptor Available Number for flow-control. When MAC finishes one descriptor data transfer into RX buffer, the RX descriptor available number will decrease 1 automatically. Use “IN” instruction to read this register and “OUT” instruction to increase the register value. When RCVEN=0, use “OUT” instruction to setup RX descriptor available number. When RCVEN=1, use “OUT” instruction to increase RX descriptor available number. This register must be initialized before RCVEN = 1.

19.11 MLSR: MAC Last Status Register(1Ch)

Register Offset: 1Ch
Register Name: MLSR: MAC Last Status Register
Reset Value : 0000 –000 0000 0000b

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFUR	LATEC	EXCEEDC	Rsvd	PHYSTS	RXDESPUA	RXFOR	Rsvd	PHYEER	DRIBBLE	OBL	LONG	RUNT	CRCERR	BROADCAST	MULTICAST

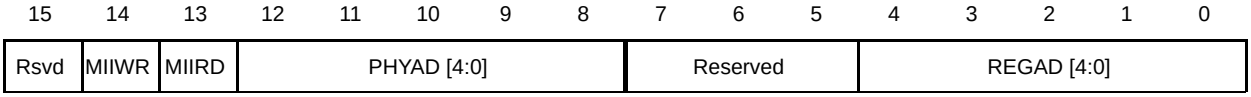
PS. The MAC last time status. It is updated by next packet coming.

Bit	Name	Attribute	Description
15	TXFUR	RO	TX FIFO Under-Run
14	LATEC	RO	Transmit Late Collision.
13	EXCEEDC	RO	Transmit Exceed Collision.
12	Rsvd	RO	Reserved
11	PHYSTS	RO	The value is the status of input pin PHY_CHG.

10	RXDESPUA	RO	RX Descriptor Unavailable.
9	RXFOR	RO	RX FIFO Over-Run.
8	Rsvd	RO	Reserved
7	PHYERR	RO	PHY RX Error.
6	DRIBBLE	RO	Dribble Packet.
5	OBL	RO	Received Packet Length Over Buffer Length.
4	LONG	RO	Received Packets Too Long.
3	RUNT	RO	Received Packets Too Short.
2	CRCERR	RO	Received Packets CRC Error.
1	BROADCAST	RO	Received Broadcast Packets.
0	MULTICAST	RO	Received Multicast Packets.

19.12 MMDIO: MDIO Control Register (20h)

Register Offset: 20h
Register Name: MMDIO: MDIO Control Register
Reset Value : 0000h



Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14	MIIWR	R/W	MDIO Write. Set 1 to write MIIWDATA [15:0] to MDIO. It will be cleared after the operation is completed.
13	MIIRD	R/W	MDIO Read. Set 1 to read data from MDIO into MIIRDATA [15:0]. It will be cleared after the operation is completed.
12-8	PHYAD [4:0]	R/W	PHY address.
7-5	Rsvd	RO	Reserved
4-0	REGAD [4:0]	R/W	REG address.

19.13 MMRD: MDIO Read Data Register (24h)

Register Offset: 24h
Register Name: MMRD: MDIO Read Data Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIIRDATA [15:0]															

Bit	Name	Attribute	Description
15-0	MIIRDATA [15:0]	RO	MII Read Data. The data, read from MDIO, are put in this register.

19.14 MMWD: MDIO Write Data Register (28h)

Register Offset: 28h
Register Name: MMRD: MDIO Write Data Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIIWDATA [15:0]															

Bit	Name	Attribute	Description
15-0	MIIWDATA [15:0]	R/W	MII Write Data. The data, intended for being written to MDIO, are put in this register.

19.15 MTDSA0: TX Descriptor Start Address 0 (2Ch)

Register Offset: 2Ch
Register Name: MTDSA0: TX Descriptor Start Address 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDSA [15:1]															0

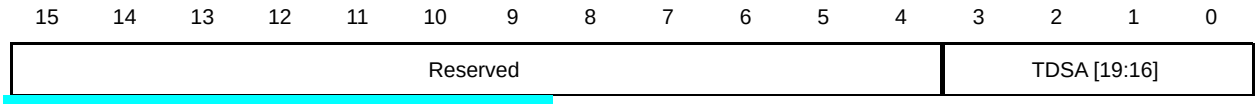
PS. Initial this register only when XMTEN=0

Bit	Name	Attribute	Description
15-1	TDSA [15:1]	R/W	TX Descriptor Start Address Bit 15 - Bit 1 that are currently being sent.
0	0	RO	This bit must be 0.

Note: The first TX descriptor start address TDSA [19:0] = {MTDSA1 [3:0], MTDSA0 [15:0]} must be Double-Word alignment. MAC will update the TX descriptor start address when the previous TX has been finished.

19.16 MTDSA1: TX Descriptor Start Address 1 (30h)

Register Offset: 30h
Register Name: MTDSA1: TX Descriptor Start Address 1
Reset Value : 0000h

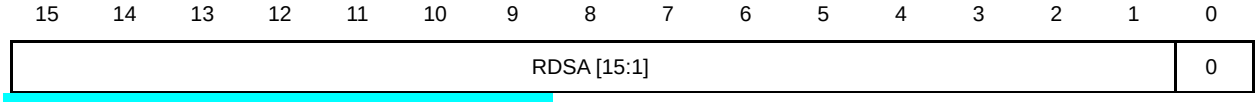


PS. Initial this register only when XMTEN=0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3-0	TDSA [19:16]	RW	TX Descriptor Start Address Bit 19-6 that are currently being sent.

19.17 MRDSA0: RX Descriptor Start Address 0 (34h)

Register Offset: 34h
Register Name: MRDSA0: RX Descriptor Start Address 0
Reset Value : 0000h



PS. Initial this register only when RCVEN=0

Bit	Name	Attribute	Description
15-1	RDSA [15:1]	R/W	RX Descriptor Start Address Bit 15-1.
0	0	RO	This bit must be 0.

Note: The first RX descriptor start address RDSA [19:0] = {MRDSA1 [3:0], MRDSA0 [15:0]} must be Double-Word alignment. MAC will update the RX descriptor start address after the previous RX has been finished.

19.18 MRDSA1: RX Descriptor Start Address 1 (38h)

Register Offset: 38h
Register Name: MRDSA1: RX Descriptor Start Address 1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RDSA [19:16]			

PS. **Initial this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3-0	RDSA [19:16]	RW	The first RX Descriptor Start Address Bit 19-16.

19.19 MISR: INT Status Register (3Ch)

Register Offset: 3Ch
Register Name: MISR: INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						PCHG	ECNTO	TXEI	Reserved		TXEND	RXEI	RXFF	RXDUA	RXEND

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	PCHG	RC	PHY Media Changed Interrupt status.
8	ECNTO	RC	Event Counter Overflow Interrupt status.
7	TXEI	RC	TX Early Interrupt status.
6-5	Rsvd	RO	Reserved.
4	TXEND	RC	This bit indicates Transmit Packet Finish Interrupt status.
3	RXEI	RC	RX Early Interrupt status.
2	RXFF	RC	RX FIFO Full Interrupt status.
1	RXDUA	RC	This bit indicates RX Descriptor Unavailable Interrupt status.
0	RXEND	RC	This bit indicates Receive Packet Finish Interrupt status.

Note: RC = Read Clear

19.20 MIER: INT Enable Register (40h)

Register Offset: 40h
Register Name: MIER: INT Enable Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MCHGE	ECNTOE	TXEIEN	Reserved		TXENDE	RXEIE	RXFFE	RXDNAE	RXENDE

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	MCHGE	RW	PHY Link Changed Interrupt Enable Set 1: Enable MAC to generate interrupts to CPU.
8	ECNTOE	R/W	Event Counter Overflow Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
7	TXEIEN	R/W	TX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
6-5	Rsvd	RO	Reserved.
4	TXENDE	R/W	Transmit Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
3	RXEIE	R/W	RX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
2	RXFFE	R/W	RX FIFO Full Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
1	RXDNAE	R/W	RX Descriptor Unavailable Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
0	RXENDE	R/W	Receive Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.

19.21 MECISR: Event Counter INT Status Register(44h)

Register Offset: 44h
Register Name: MECISR: Event Counter INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCI	LCCI	STPCI	RFFCI	RDUCI	Rsvd	LONGCI	RUNTCI	CRCECI	BCCI	MCCI	SRPCI

The correspond bit in Event Counter INT status register will be set when the MSB bit in related Event Counter register is set to 1. Reading this register will clear these bits. Those event counters will keep increasing until reaching 255 or 65535.

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCI	RO	TX FIFO under-run Dropped Packet Counter Interrupt status.
10	LCCI	RO	TX Late Collision Counter Interrupt status.
9	STPCI	RO	TX Successfully package counter Interrupt status.
8	RFFCI	RO	RX FIFO Full Counter Interrupt status.
7	RDUCI	RO	RX Descriptor Unavailable Dropped Packet Counter Interrupt status.
6	Rsvd	RO	Reserved.
5	LONGCI	RO	RX Long Packet Counter Interrupt status.
4	RUNTCI	RO	RX Runt Packet Counter Interrupt status.
3	CRCECI	RO	RX CRC Error Packet Counter Interrupt status.
2	BCCI	RO	RX Broadcast Packet Counter Interrupt status.
1	MCCI	RO	RX Multicast Packet Counter Interrupt status.
0	SRPCI	RO	RX Successfully Packet Counter Interrupt status.

19.22 MECIER: Event Counter INT Enable Register (48h)

Register Offset: 48h
Register Name: MECIER: Event Counter INT Mask Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCIE	LCCIE	STPCIE	RFFCIE	RDUCIE	Rsvd	LONGCIE	RUNTCIE	CRCECIE	BCCIE	MCCIE	SRPCIE

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCIE	RW	TX FIFO under-run Dropped Packet Counter Interrupt Enable
10	LCCIE	R/W	TX Late Collision Counter Interrupt Enable.
9	STPCIE	R/W	TX Successfully Packet Counter Interrupt Enable.
8	RFFCIE	R/W	RX FIFO Full Counter Interrupt Enable.
7	RDUCIE	R/W	RX Descriptor Unavailable Dropped Packet Counter Interrupt Enable.
6	Rsvd	RO	Reserved.
5	LONGCIE	R/W	RX Long Packet Counter Interrupt Enable.
4	RUNTCIE	R/W	RX Runt Packet Counter Interrupt Enable.
3	CRCECIE	R/W	RX CRC Error Packet Counter Interrupt Enable.

2	BCCIE	R/W	RX Broadcast Packet Counter Interrupt Enable.
1	MCCIE	R/W	RX Multicast Packet Counter Interrupt Enable.
0	SRPCIE	R/W	RX Successfully Packet Counter Interrupt Enable.

Note: Reading any one of all the following event counter registers will clear its value to 0.

19.23 MRCNT: Successfully Received Packet Counter (50h)

Register Offset: 50h
Register Name: MRCNT: Successfully Received Packet Counter
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRPCNT [15:0]															

Bit	Name	Attribute	Description
15-0	SRPCNT [15:0]	RC	Successfully Received Packet Counter

Note: RC = Read Clear

19.24 MECNT0: Event Counter 0 (52H)

Register Offset: 52h
Register Name: MECNT0: Event Counter 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCCNT [7:0]								MCCNT [7:0]							

Bit	Name	Attribute	Description
15-8	BCCNT [7:0]	RC	Broadcast Packet Counter.
7-0	MCCNT [7:0]	RC	Multicast Packet Counter.

Note: RC = Read Clear

19.25 MECNT1: Event Counter 1 (54h)

Register Offset: 54h
Register Name: MECNT1: Event Counter 1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUNCNT [7:0]								CRCECNT [7:0]							

Bit	Name	Attribute	Description
15-8	RUNCNT [7:0]	RC	Run Packet Counter.
7-0	CRCECNT [7:0]	RC	CRC Error Packet Counter.

Note: RC = Read Clear

19.26 MECNT2: Event Counter 2 (56h)

Register Offset: 56h
Register Name: MECNT2: Event Counter 2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								LONGCNT [7:0]							

Bit	Name	Attribute	Description
15-8	Rsvd	RC	Reserved
7-0	LONGCNT [7:0]	RC	Receive Long Packet Counter.

Note: RC = Read Clear

19.27 MCENT3: Event Counter 3 (58h)

Register Offset: 58h
Register Name: MECNT3: Event Counter 3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFFCNT [7:0]								RDUVCNT [7:0]							

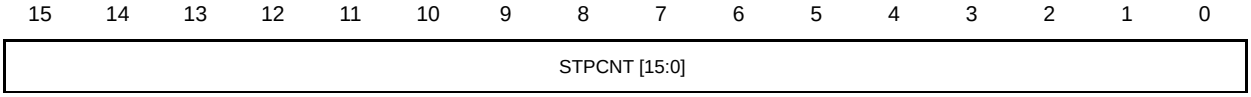
Bit	Name	Attribute	Description

15-8	RFFCNT [7:0]	RC	RX FIFO Full Packet Counter.
7-0	RDUVCNT [7:0]	RC	RX Descriptor Unavailable Packet lost Counter.

Note: RC = Read Clear

19.28 MTCNT: Successfully Transmit Packet Counter (5Ah)

Register Offset: 5Ah
Register Name: MTCNT: Successfully Transmit Packet Counter
Reset Value : 0000h

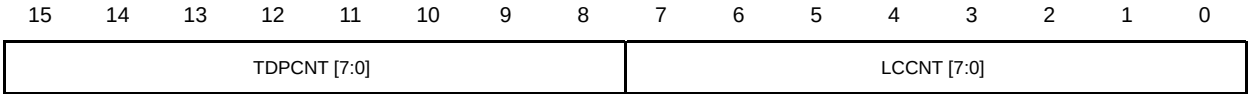


Bit	Name	Attribute	Description
15-0	STPCNT [15:0]	RC	Successfully Transmitted Packet Counter.

Note: RC = Read Clear

19.29 MCENT4: Event Counter 4 (5Ch)

Register Offset: 5Ch
Register Name: MECNT4: Event Counter 4
Reset Value : 0000h



Bit	Name	Attribute	Description
15-8	TDPCNT [7:0]	RC	TX Dropped Packet Counter by TX FIFO under-run.
7-0	LCCNT [7:0]	RC	TX Late Collision Packet Counter.

Note: RC = Read Clear

19.30 MPCNT: Pause Frame Counter (5Eh)

Register Offset: 5Eh
Register Name: MPCNT: Pause Frame Counter
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXPFCNT [7:0]								RXPFCNT [7:0]							

Bit	Name	Attribute	Description
15-8	TXPFCNT [7:0]	RC	Transmitted Pause Frame Counter.
7-0	RXPFCNT [7:0]	RC	Received Pause Frame Counter.

Note: RC = Read Clear

19.31 MAR0 ~3: Hash Table Word 0 ~3 (60h, 62h, 64h, 66h)

Register Offset: 60h
Register Name: MAR0: Hash Table Word 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR0 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR0 [15:0]	R/W	Hash Table Word 0.

Register Offset: 62h
Register Name: MAR1: Hash Table Word 1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR1 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR1 [15:0]	R/W	Hash Table Word 1.

Register Offset: 64h
Register Name: MAR2: Hash Table Word 2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR2 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR2 [15:0]	R/W	Hash Table Word 2.

Register Offset: 66h
Register Name: MAR3: Hash Table Word 3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR3 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR3 [15:0]	R/W	Hash Table Word 3.

19.32 MID0 (68h, 6Ah, 6Ch)

Register Offset: 68h
Register Name: MID0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0L [15:0]															

Register Offset: 6Ah
Register Name: MID0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0M [15:0]															

Register Offset: 6Ch
Register Name: MID0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0H [15:0]															

The MAC/Multicast address MID0 [47:0] = {MID0H [15:0], MID0M [15:0], MID0L [15:0]};

For example: MAC address is 01:02:03:04:05:06, the contents for MID are:

MID0L [15:0] = 0201h

MID0M [15:0] = 0403h

MID0H [15:0] = 0605h

Bit 15-0: MID0L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID0M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID0H [15:0], the two bytes in the last line of the MAC/Multicast address.

19.33 MID1 (70h, 72h, 74h)

Register Offset: 70h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1L [15:0]															

Register Offset: 72h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1M [15:0]															

Register Offset: 74h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1H [15:0]															

The MAC/Multicast address MID1 [47:0] = {MID1H [15:0], MID1M [15:0], MID1L [15:0]};

Bit 15-0: MID1L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID1M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID1H [15:0], the two bytes in the last line of the MAC/Multicast address.

19.34 MID2 (78h, 7Ah, 7Ch)

Register Offset: 78h
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2L [15:0]															

Register Offset: 7Ah
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2M [15:0]															

Register Offset: 7Ch
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2H [15:0]															

The MAC/Multicast address MID2 [47:0] = {MID2H [15:0], MID2M [15:0], MID2L [15:0]};

Bit 15-0: MID2L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID2M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID2H [15:0], the two bytes in the last line of the MAC/Multicast address.

19.35 MID3 (80h, 82h, 84h)

Register Offset: 80h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3L [15:0]															

Register Offset: 82h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3M [15:0]															

Register Offset: 84h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3H [15:0]															

The MAC/Multicast address MID3 [47:0] = {MID3H [15:0], MID3M [15:0], MID3L [15:0]};

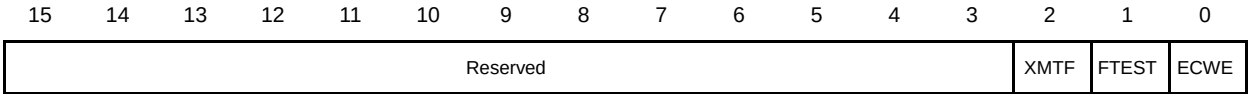
Bit 15-0: MID3L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID3M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID3H [15:0], the two bytes in the last line of the MAC/Multicast address.

19.36 MTSCF: The Configure of Test Mode (ACh)

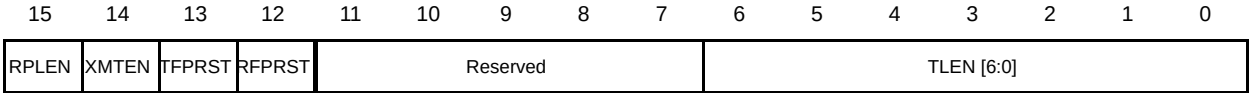
Register Offset: ACh
Register Name: MTSCF: The Configure of Test Mode
Reset Value : 0000h



Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved
2	XMTF	R/W	Transmit Flag. This bit must be set to 1.
1	FTEST	R/W	1: The buffer manager and the I/F of arbiter will be halted. Then Users can write the TX buffer and read RX buffer directly. 0: Normal function. Changing this bit from 1 to 0 will trigger MRST.
0	ECWE	R/W	Event Counter Read/Write Enable. 1: The event counter can be read or write. 0: Normal function. Read only.

19.37 MTSCR: The Control of Test Mode (AEh)

Register Offset: AEh
Register Name: MTSCF: The Control of Test Mode
Reset Value : 0000h



Bit	Name	Attribute	Description
15	RPLEN	R/W	Indicate that there was a packet in RX Buffer.
14	XMTEN	R/W	Trigger the MAC to send the packet in TX Buffer. This bit is set by SW and cleared by HW.
13	TFPRST	R/W	Reset TX FIFO read/write pointer. This bit is set by SW and cleared by HW.
12	RFPRST	R/W	Reset RX FIFO read/write pointer. This bit is set by SW and cleared by HW.
11-7	Rsvd	RO	Reserved
6-0	TLEN [6:0]	R/W	TX packet Length.

19.38 MTSTF: The TX FIFO RD/WR Data (B0h)

Register Offset: B0h
Register Name: MTSTF: The TX FIFO RD/WR Data
Reset Value : ----h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FTD [15:0]															

Bit	Name	Attribute	Description
15-0	FTD [15:0]	R/W	FIFO TX Data. Users can read /write data from this register. The pointer will be automatically increased by two after reading/writing.

19.39 MTSRF: The RX FIFO RD/WR Data (B2h)

Register Offset: B2h
Register Name: MTSTF: The RX FIFO RD/WR Data
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRD [15:0]															

Bit	Name	Attribute	Description
15-0	FRD [15:0]	R/W	FIFO RX Data. Users can read /write data from this register. The pointer will be automatically increased by two after reading/writing.

19.40 MTSRS: The RX Status in Test Mode (B4h)

Register Offset: B4h
Register Name: MTSTS: The RX Status in Test Mode
Reset Value : 00FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				FRLEN [5:0]				FRRUNT	FRCRCE	FRBC	FRMC	FRMCH	FRMID [2:0]		

Bit	Name	Attribute	Description
15-14	Rsvd	RO	Reserved
13-8	FRLEN [5:0]	R/W	Received packet Length.
7	FRRUNT	R/W	Received Runt packet.
6	FRCRCE	R/W	Received CRC Error packet.
5	FRBC	R/W	Received Broadcast packet.
4	FRMC	R/W	Received Multicast packet.
3	FRMCH	R/W	Received Multicast Hit in hash table.
2-0	FRMID	R/W	This group has been hit in hash table.

20. DC Electrical Characteristics

20.1 Absolute Maximum Ratings (25℃)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC/AVCC	Supply Voltage	3.0	3.6	V	
VIN	DC Input Voltage (VIN)	3.0	3.6	V	
VOUT	DC Output Voltage (VOUT)	VCC-0.3	VCC+0.3	V	
Vil	Input Low Voltage	---	0.3xVCC	V	
Vih	Input High Voltage	0.7xVCC	---	V	
Vol	Output Low Voltage	---	0.4	V	
Voh	Output High Voltage	2.4	---	V	
Iol*	Switching Current Low	16VCC	---	mA	VCC>Vout≧0.6VCC
Ioh**	Switching Current High	-12VCC	---	mA	0<Vout≦0.3VCC

Note: * Eq. C = (256/VCC) x Vout x (VCC - Vout)

** Eq. D = (98.0/VCC) x (Vout - VCC) x (Vout + 0.4VCC)

20.2 Operating Temperature

Symbol	Parameter	Typ.	Unit	Conditions
TA$_{PQFP}$	Ambient Temperature	70	℃	1. Open case testing. 2. for PQFP package.

21. AC Electrical Characteristics

21.1 Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description	Parameter Symbol	No.	Description
tAVCH	14	AD Address Valid to Clock High	tCVCTV	20	Control Active Delay 1
tAVLL	12	AD Address Valid to ALE Low	tCVCTX	31	Control Inactive Delay
tAVRL	66	AD Address Valid to RD_n Low	tCXCSX	17	PCS_n Hold from Command Inactive
tAZRL	24	AD Address Float to RD_n Active	tDVCL	1	Data in Setup
tCHCSV	67	SD_CLK High to LCS_n/UCS_n Valid	tHVCL	58	HOLD Setup
tCHCSX	18	PCS_n Inactive Delay	tLHAV	23	ALE High to Address Valid
tCHCTV	22	Control Active Delay 2	tLHLL	10	ALE Width
tCHLH	9	ALE Active Delay	tLLAX	13	AD Address Hold from ALE Inactive
tCHLL	11	ALE Inactive Delay	tRESIN	57	RST_n Setup Time
tCLAV	5	AD Address Valid Delay	tRHAV	29	RD_n Inactive to AD Address Active
tCLAX	6	Address Hold	tRHDX	59	RD_n High to Data Hold on AD Bus
tCLAZ	15	AD Address Float Delay	tRHLH	28	RD_n Inactive to ALE High
tCLCSV	16	PCS Active Delay	tRLRH	26	RD_n Pulse Width
tCLDOX	30	Data Hold Time	tWHDEX	35	WR_n Inactive to DEN_n Inactive
tCLDV	7	Data Valid Delay	tWHDX	34	Data Hold after WR_n
tCLDX	2	Data in Hold	tWHLH	33	WR_n Inactive to ALE High
tCLRH	27	RD_n Inactive Delay	tWLWH	32	WR_n Pulse Width
tCLRL	25	RD_n Active Delay			

21.2 Numerical Key to Switching Parameter Symbols

No.	Parameter Symbol	Description	No.	Parameter Symbol	Description
1	tDVCL	Data in Setup	24	tAZRL	AD Address Float to RD_n Active
2	tCLDX	Data in Hold	25	tCLRL	RD_n Active Delay
5	tCLAV	AD Address Valid Delay	26	tRLRH	RD_n Pulse Width
6	tCLAX	Address Hold	27	tCLRH	RD_n Inactive Delay
7	tCLDV	Data Valid Delay	28	tRHLH	RD_n Inactive to ALE High
9	tCHLH	ALE Active Delay	29	tRHAV	RD_n Inactive to AD Address Active
10	tLHLL	ALE Width	30	tCLDOX	Data Hold Time
11	tCHLL	ALE Inactive Delay	31	tCVCTX	Control Inactive Delay
12	tAVLL	AD Address Valid to ALE Low	32	tWLWH	WR_n Pulse Width
13	tLLAX	AD Address Hold from ALE Inactive	33	tWHLH	WR_n Inactive to ALE High
14	tAVCH	AD Address Valid to Clock High	34	tWHDX	Data Hold after WR_n
15	tCLAZ	AD Address Float Delay	35	tWHDEX	WR_n Inactive to DEN_n Inactive
16	tCLCSV	PCS Active Delay	57	tRESIN	RST_n Setup Time
17	tCXCSX	PCS_n Hold from Command Inactive	58	tHVCL	HOLD Setup
18	tCHCSX	PCS_n Inactive Delay	59	tRHDX	RD_n High to Data Hold on AD Bus
20	tCVCTV	Control Active Delay 1	66	tAVRL	AD Address Valid to RD_n Low
22	tCHCTV	Control Active Delay 2	67	tCHCSV	SD_CLK High to LCS_n/UCS_n Valid
23	tLHAV	ALE High to Address Valid			

21.3 CPU Bus

● **Read Cycle (100 MHz)**

Parameter			Preliminary 100 MHz		Unit
No.	Symbol	Description	Min.	Max.	
General Timing Requirements					
1	tDVCL	Data in Setup	2	---	ns
2	tCLDX	Data in Hold[c]	0.4	---	ns
General Timing Responses					
5	tCLAV	AD Address Valid Delay and BHE	3.2	---	ns
6	tCLAX	Address Hold	3	---	ns
9	tCHLH	ALE Active Delay	3	---	ns
10	tLHLL	ALE Width	1T	1.5T	ns
11	tCHLL	ALE Inactive Delay	---	2.7	ns
12	tAVLL	AD Address Valid to ALE Low[a]	4.4 (T1+no wait)	9.2 (T1+wait)	ns
13	tLLAX	AD Address Hold from ALE Inactive[a]	0.8	0.8+T1 wait	ns
14	tAVCH	AD Address Valid to Clock High	---	1.2	ns
15	tCLAZ	AD Address Float Delay	---	3.5	ns
16	tCLCSV	PCS_n Active Delay	8	---	ns
17	tCXCSX	PCS_n Hold from Command Inactive[a]	7	---	ns
18	tCHCSX	PCS_n Inactive Delay	5	---	ns
20	tCVCTV	Control Active Delay 1[b]	---	8.5	ns
22	tCHCTV	Control Active Delay 2[b]	---	3	ns
23	tLHAV	ALE High to Address Valid	5.6	---	ns
Read Cycle Timing Responses					
24	tAZRL	AD Address Float to RD_n Active	---	0	ns
25	tCLRL	RD_n Active Delay	3	---	ns
26	tRLRH	RD_n Pulse Width	2T (0 wait)	2T+T3 wait	ns
27	tCLRH	RD_n Inactive Delay	2.8	---	ns
28	tRHLH	RD_n Inactive to ALE High[a]	4.5	---	ns
29	tRHAV	RD_n Inactive to AD Address Active[a]	6	---	ns
59	tRHDX	RD_n High to Data Hold on AD Bus[c]	0	---	ns
66	tAVRL	AD Address Valid to RD_n Low[a]	---	14	ns
67	tCHCSV	SD_CLK High to LCS_n/UCS_n Valid	---	6	ns

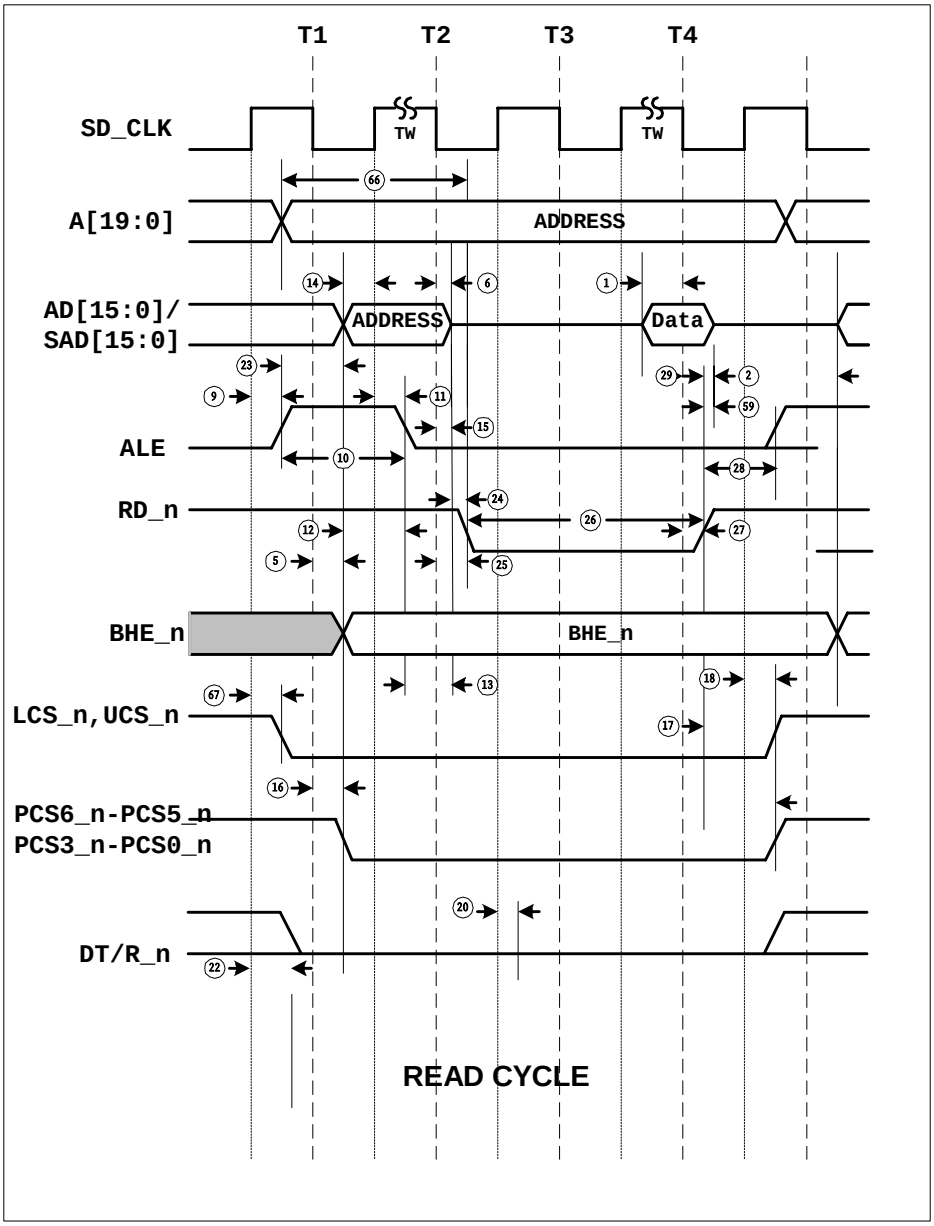
Notes: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a. Equal loading on referenced pins.

b. This parameter applies to the INTA1_n–INTA0_n , WR_n, WHB_n, and WLB_n signals.

c. If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

● **Read Cycle Waveforms**



● Write Cycle (100 MHz)

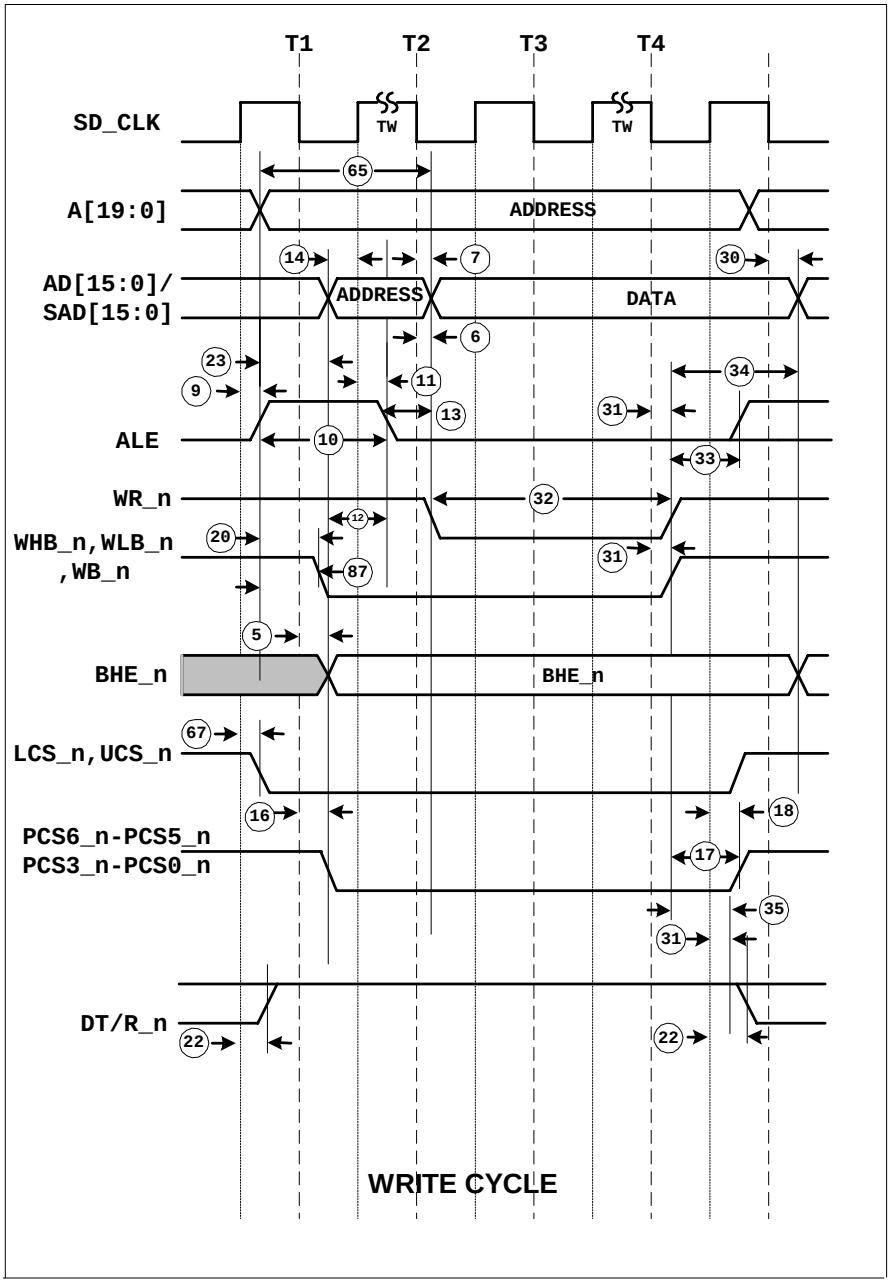
Parameter			Preliminary 100 MHz		Unit
No.	Symbol	Description	Min.	Max.	
General Timing Responses					
5	tCLAV	AD Address Valid Delay and BHE	**3.2**	**---**	ns
6	tCLAX	Address Hold	**3**	**---**	ns
7	tCLDV	Data Valid Delay	**2.5**	**---**	ns
9	tCHLH	ALE Active Delay	**3**	**---**	ns
10	tLHLL	ALE Width	**1T**	**1.5T**	ns
11	tCHLL	ALE Inactive Delay	**---**	**2.7**	ns
12	tAVLL	AD Address Valid to ALE Low[a]	**4.4 (T1 no wait)**	**9.2 (T1 wait)**	ns
13	tLLAX	AD Address Hold from ALE Inactive[a]	**0.8 (T1 no wait)**	**5.6 (T1 wait)**	ns
14	tAVCH	AD Address Valid to Clock High	**---**	**1.2**	ns
16	tCLCSV	PCS_n Active Delay	**8**	**---**	ns
17	tCXCSX	PCS_n Hold from Command Inactive[a]	**7**	**---**	ns
18	tCHCSX	PCS_n Inactive Delay	**5**	**---**	ns
20	tCVCTV	Control Active Delay 1[b]	**---**	**8.5**	ns
22	tCHCTV	Control Active Delay 2[b]	**---**	**3**	ns
23	tLHAV	ALE High to Address Valid	**5.6**	**---**	ns
Write Cycle Timing Responses					
30	tCLDOX	Data Hold Time	**2.1**		ns
31	tCVCTX	Control Inactive Delay[b]	**0.3**	**---**	ns
32	tWLWH	WR_n Pulse Width	**2T**	**2T+wait**	ns
33	tWHLH	WR_n Inactive to ALE High	**1/2T+1.6**		ns
34	tWHDX	Data Hold after WR_n	**1T+0.5**		ns
35	tWHDEX	WR_n Inactive to DEN_n Inactive	**1/2T+0.3**		ns
67	tCHCSV	SD_CLK High to LCS_n/UCS_n Valid	**---**	**6**	ns

Notes: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where V_{IH} = V_{CC} – 0.5 V.

a. Equal loading on referenced pins.

b. This parameter applies to the INTA1_n–INTA0_n , WR_n, WHB_n, and WLB_n signals.

Write Cycle Waveforms

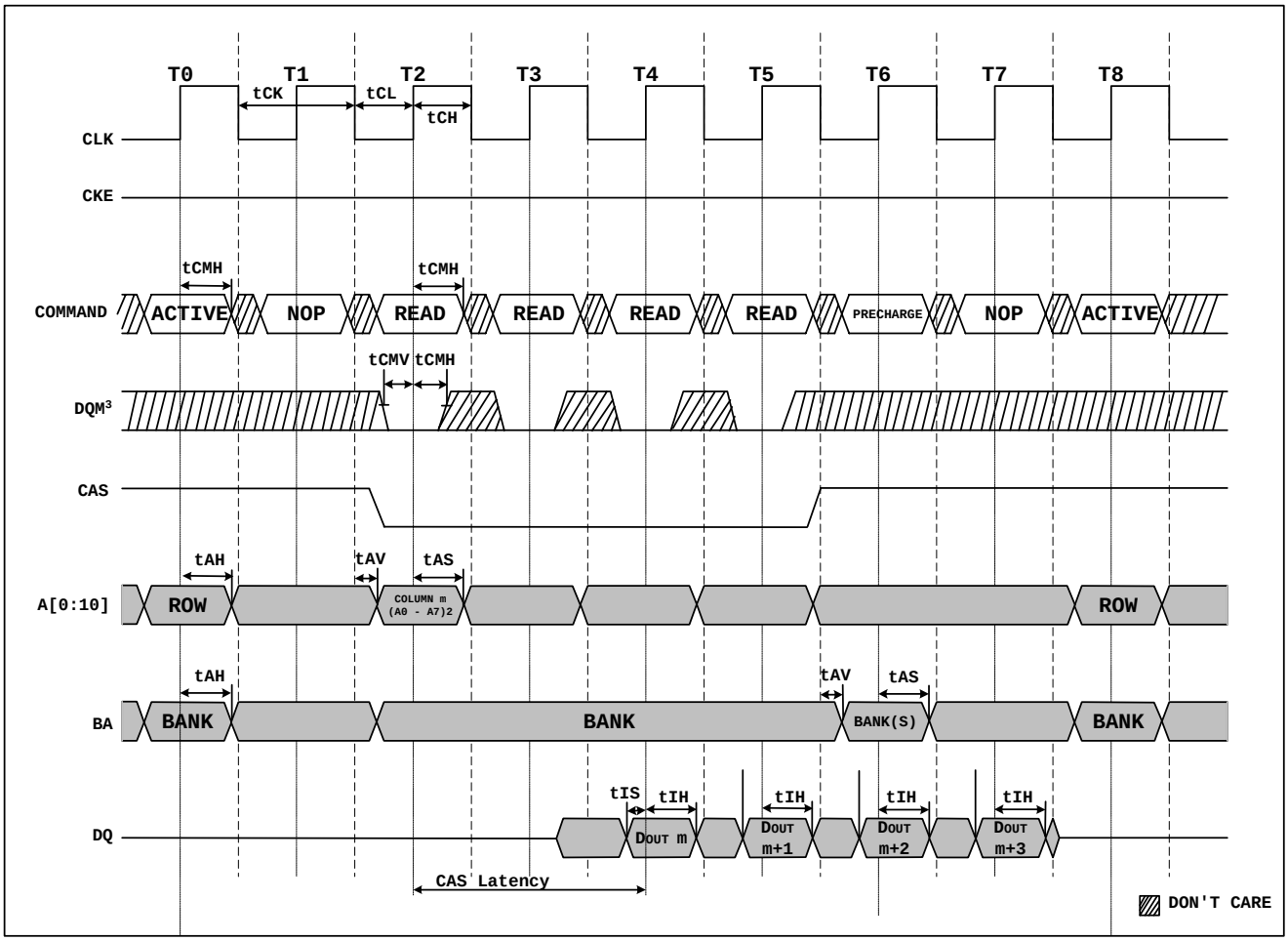


21.4 SDRAM Bus

SDRAM Read Cycle (100 MHz)

Symbol	Description	Min.	Type	Max.
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
TCMV	Command Valid Delay time	---	---	6
Tcmh	Command Hold time	4	---	---
TAv	Address Valid Delay time	---	---	5
tAH	Address Hold time	4	---	---
tIS	Data Input Setup time	2	---	---
tIH	Data Input Hold time	1	---	---

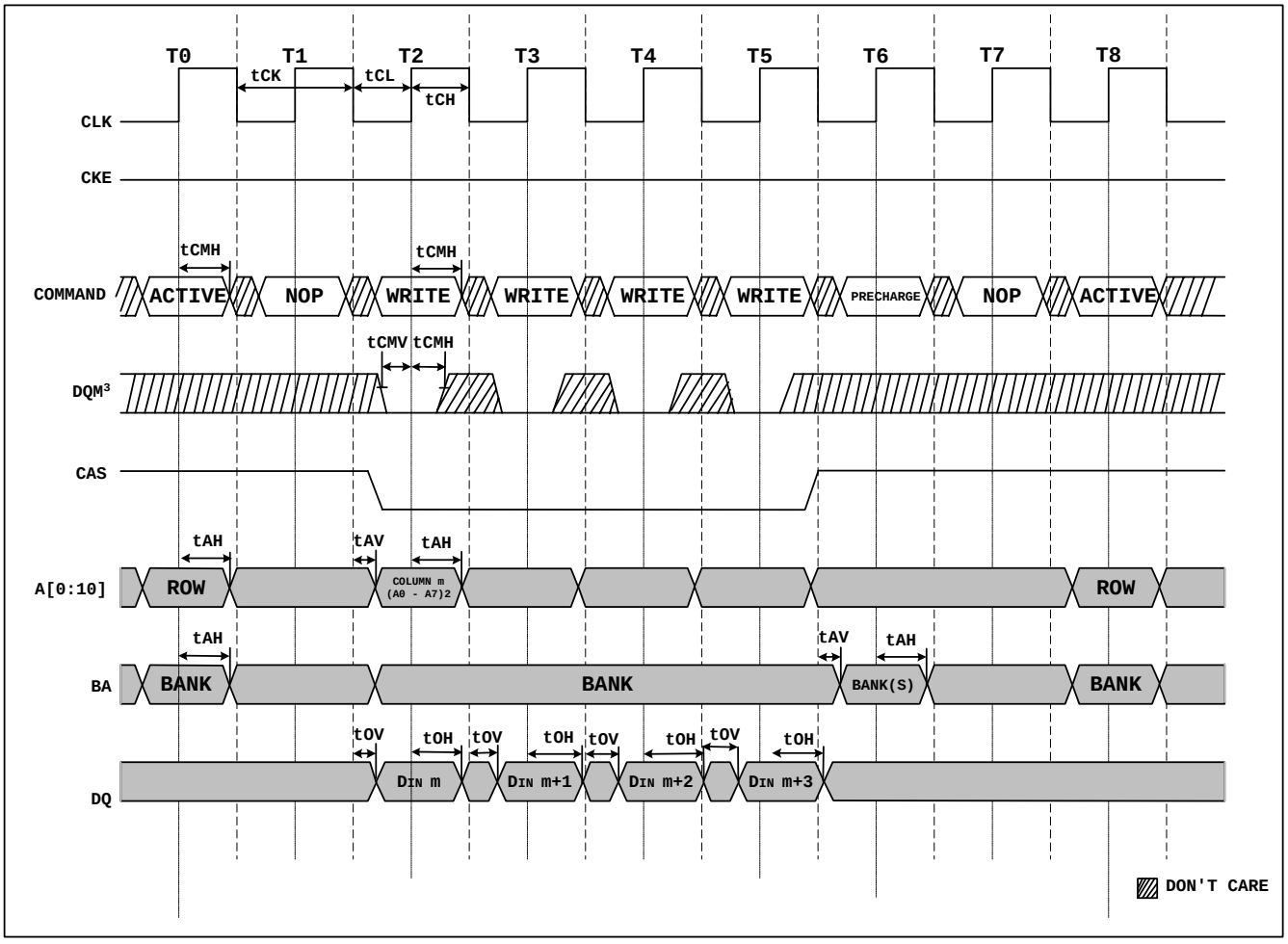
● **SDRAM Read Cycle Waveforms**



● SDRAM Write Cycle (100 MHz)

Symbol	Description	Min.	Type	Max.
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
tCMV	Command Valid Delay time	---	---	6
tCMH	Command Hold time	4	---	---
tAV	Address Valid Delay time	---	---	5
tAH	Address Hold time	---	---	5
tOV	Data Output Valid Delay time	---	---	8
tOH	Data Output Hold time	2	---	---

● SDRAM Write Cycle Waveforms



21.5 CPU Reset

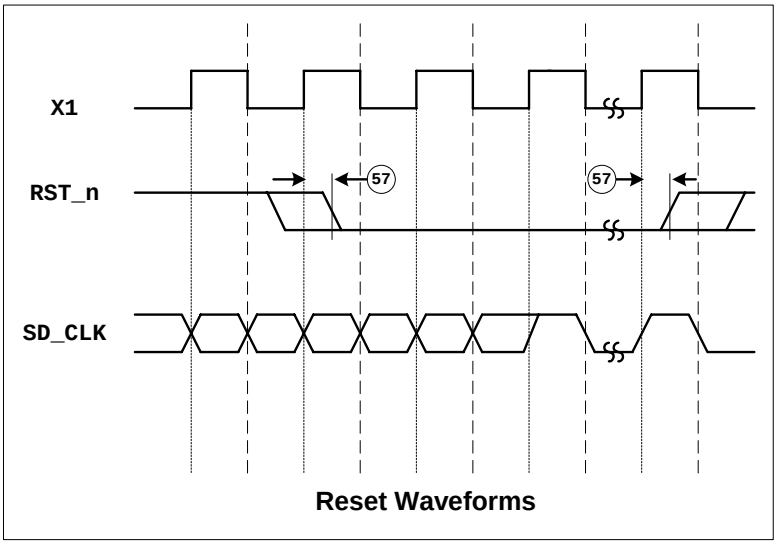
● Reset and Bus Hold (100 MHz)

Parameter			Preliminary 100 MHz		Unit
No.	Symbol	Description	Min.	Max.	
Reset and Bus Hold Timing Requirements					
5	tCLAV	AD Address Valid Delay and BHE	**3.2**	**---**	ns
15	tCLAZ	AD Address Float Delay	**---**	**3.5**	ns
57	tRESIN	RST_n Setup Time	**2**	**---**	ns
58	tHVCL	HOLD Setup[a]	**2.5**	**---**	ns

Note: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a. This timing must be met to guarantee recognition at the next clock.

● Reset Waveforms

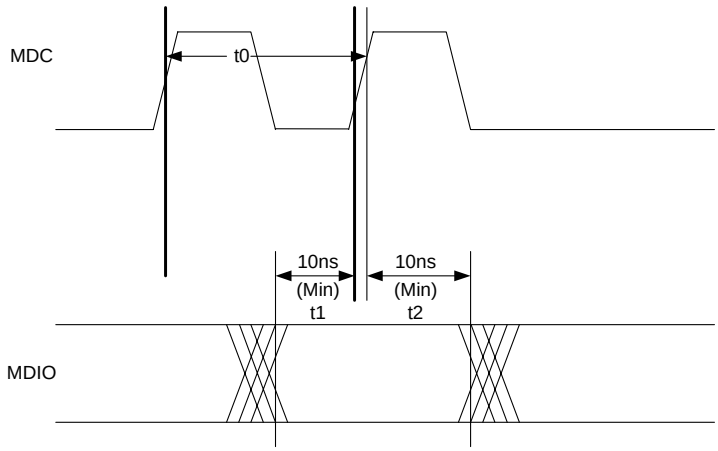


Reset Waveforms

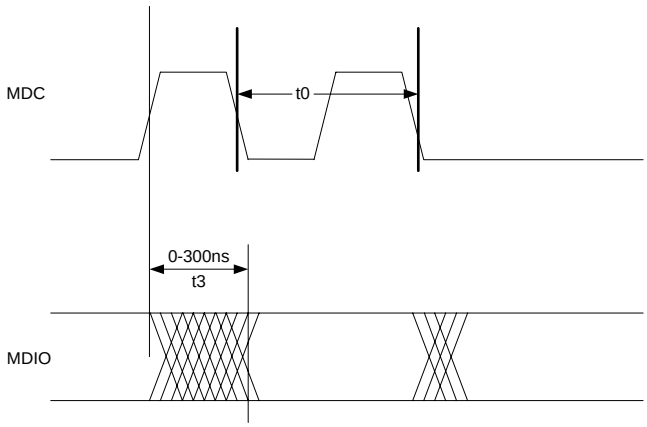
21.6 MDC/MDIO Timing

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
t0	MDC Cycle Time		TXC/10			
t1	MDIO Setup before MDC		MDC/2-10			
t2	MDIO Hold after MDC		MDC/2+10			
t3	MDC to MDIO Output Delay	0		300		

MDIO Timing When OUTPUT by EVA-X1610C



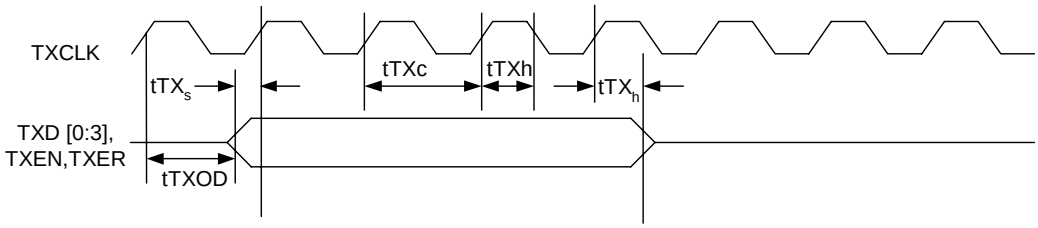
MIDO Timing When OUTPUT by PHY



21.7 TX Transmit Timing Parameters

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tTXh, tTXl	TXCLK High/Low Time					
tTXs	TXD{0:3}, TXEN, and TXER Setup to TXCLK High	1T-6				
tTXh	TXD{0:3}, TXEN, and TXER Hold from TXCLK High			4		
tTXOD	TXCLK to Output Delay			6		
Typical Values are at 25℃ and for design aid only; not guaranteed and not subject to production testing.						

21.8 TX Transmit Timing Diagram

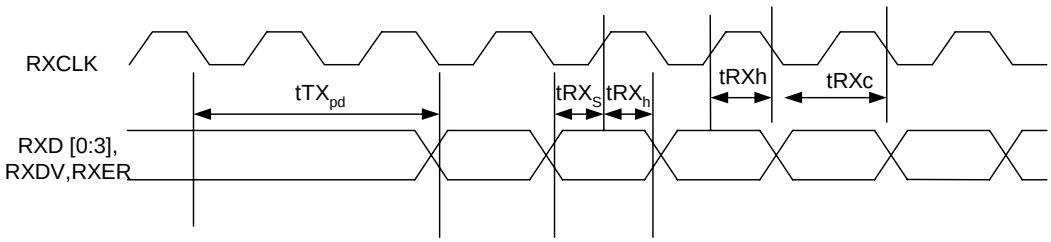


Note: The rising time for TXCLK must be less than 3.6ns.

21.9 RX Receive Timing Parameters

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tRXs	RXD{0:3}, RXDN, and RXER Setup to RXCLK High	0.8				
tRXh	RXD{0:3}, RXDN, and RXER Hold from RXCLK High	1				
Typical Values are at 25℃ and for design aid only; not guaranteed and not subject to production testing.						

21.10 RX Receive Timing Diagram



Note: The rising time for RXCLK must be less than 3.6ns.

22. Instruction Set OP-Code and Clock Cycles

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if	1/8	

Function	Format				Clocks	Notes
				sw=01		
immediate to accumulator	0000010w	data	data if w=1		1	
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)	1111011w	mod 100 r/m				
register-byte					13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m				
register-byte					16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)	1111011W	mod 110 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)	1111011w	mod 111 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
AAS = ASCII adjust for subtraction	00111111				3	
DAS = Decimal adjust for subtraction	00101111				2	
AAA = ASCII adjust for addition	00110111				3	
DAA = Decimal adjust for addition	00100111				2	
AAD = ASCII adjust for divide	11010101	00001010			14	
AAM = ASCII adjust for multiply	11010100	00001010			15	

CBW = Corrvert byte to word	10011000				2	
CWD = Convert word to double-word	10011001				2	

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	
JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp			1/9	
JNBE/JA = not below or equal/above	01110111	disp			1/9	

Function	Format			Clocks	Notes
JNP/JPO = not parity/parity odd	01111011	disp		1/9	
JNO = not overflow	01110001	disp		1/9	
JNS = not sign	01111001	disp		1/9	
Unconditional Transfers					
CALL = Call procedure					
direct within segment	11101000	disp-low	disp-high	11	
reg/memory indirect within segment	11111111	mod 010 r/m		12/17	
indirect intersegment	11111111	mod 011 r/m	(mod≠11)	25	
direct intersegment	10011010	segment offset		18	
		selector			
RET = Retum from procedure					
within segment	11000011			16	
within segment adding immed to SP	11000010	data-low	data-high	16	
intersegment	11001011			23	
instersegment adding immed to SP	1001010	data-low	data-high	23	
JMP = Unconditional jump					
short/long	11101011	disp-low		9/9	
direct within segment	11101001	disp-low	disp-high	9	
reg/memory indirect within segment	11111111	mod 100 r/m		11/16	
indirect intersegment	11111111	mod 101 r/m	(mod ?11)	18	
direct intersegment	11101010	segment offset		11	
		selector			
Iteration Control					
LOOP = Loop CX times	11100010	disp		7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp		7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp		7/16	
JCXZ = Jump if CX = zero	11100011	disp		7/15	
Interrupt					
INT = Interrupt					
Type specified	11001101	type		41	
Type 3	11001100			41	
INTO = Interrupt on overflow	11001110			43/4	
BOUND = Detect value out of range	01100010	mod reg r/m		21-60	
IRET = Interrupt return	11001111			31	
PROCESSOR CONTROL INSTRUCTIONS					
CLC = clear carry	11111000			2	
CMC = Complement carry	11110101			2	
STC = Set carry	11111001			2	
CLD = Clear direction	11111100			2	
STD = Set direction	11111101			2	
CLI = Clear interrupt	11111010			5	
STI = Set interrupt	11111011			5	
HLT = Halt	11110100			1	
WAIT = Wait	10011011			1	
LOCK = Bus lock prefix	11110000			1	
ESC = Math coprocessor escape	11011MMM	mod PPP r/m		1	
NOP = No operation	10010000			1	
SEGMENT OVERRIDE PREFIX					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

23. EVA-X1610C Execution Timing

The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with data or displacement required for execution, has been prefetched and resided in the instruction queue at the time needed.

2. No wait states or bus HOLDs occur.

3. All word -data are located on even-address boundaries.

4. One RISC micro operation (*u*OP) maps one cycle (according to the pipeline stages described below), except the following case:

Pipeline Stages for single micro operation (one cycle):

Fetch → Decode → op_r → ALU → WB (For ALU function *u*OP)

Fetch → Decode → EA → Access → WB (For Memory function *u*OP)

4.1 *Memory read u*OP need 6 cycles for bus.

Pipeline stages for *Memory read u*OP(6 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB

Bus Cycle

4.2 *Memory push u*OP need 1 cycle if it has no previous *Memory push u*OP, and 5 cycles if it has previous *Memory push* or *Memory Write u*OP.

Pipeline stages for *Memory push u*OP after *Memory push u*OP (another 5 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB (1st *Memory push u*OP)

(2nd *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

pipeline stall

4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8 bits operation need both 8 cycles, for 16 bits operation need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*Unconditional Fetch u*OP) will need 9 cycles.

Pipeline stages for unconditional fetch:

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → Fetch (*Fetch u*OP)

(next *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

will be flushed

These 9 cycles caused branch penalty

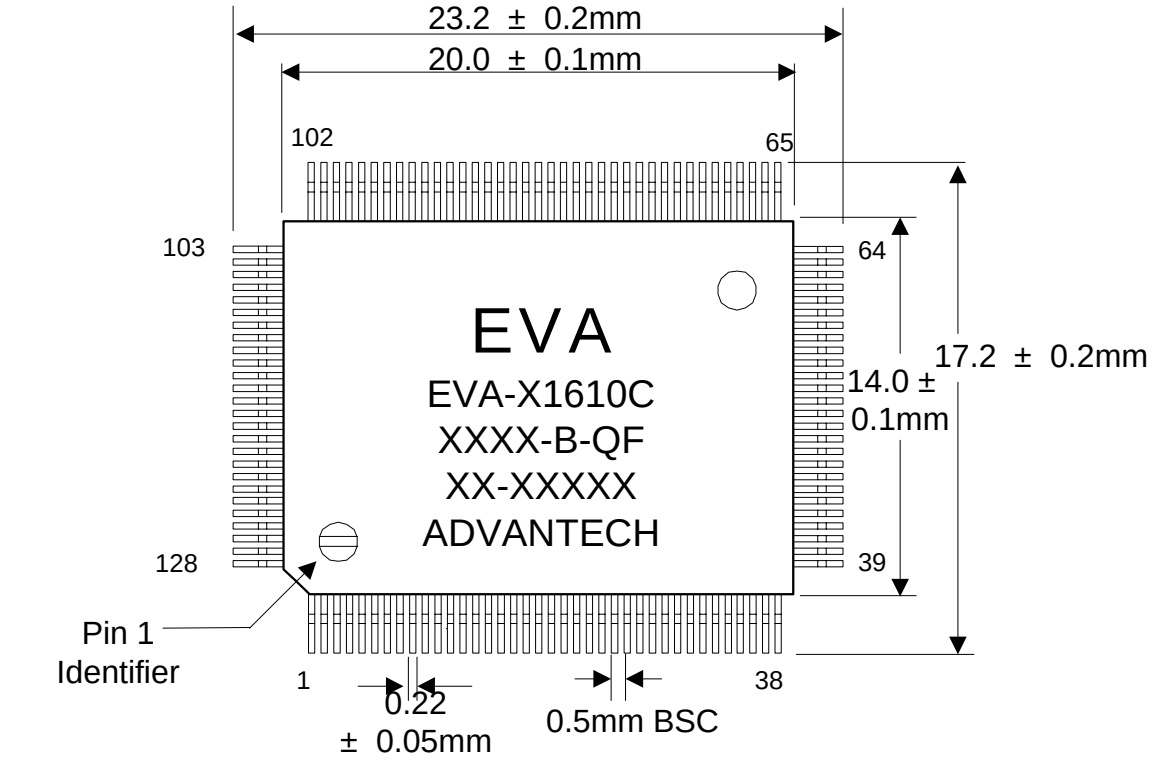
→ Fetch → Decode → following stages...(New *u*OP)

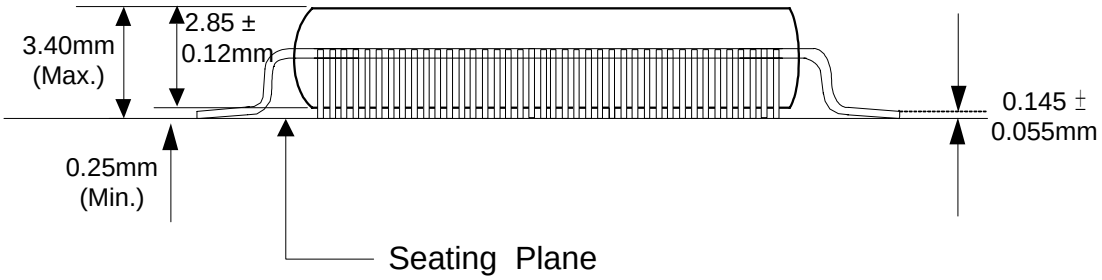
Note: op_r: operand read stage, EA: Calculate Effective Address stage, Idle: Bus Idle stage, T0..T3: Bus T0..T3 stage,

Access: Access data from cache memory stage.

24. Package Information

24.1 PQFP 128 pins





25. Revision History

Rev.	Date	History
Draft	04/23/2002	Draft Version
P01	05/17/2002	Preliminary Version 0.1
P02	06/13/2002	Preliminary Version 0.2
P03	07/03/2002	Preliminary Version 0.3
P04	09/12/2002	Preliminary Version 0.4
F10	10/01/2002	Final Version 1.0
F11	10/14/2002	Final Version 1.1
F12	12/17/2002	Final Version 1.2
F13	01/03/2003	Final Version 1.3
F14	02/14/2003	Final Version 1.4
F15	03/21/2003	Final Version 1.5 1. page 98: Bit 6 & 5 for F4h register are modified to be **Reserved.** 2. page 128 & 131: Add in **Signal No.** 30, 33, 34 and 35, and the related **values**.