



User Manual

ARK-3420

Compact Embedded IPC

Trusted ePlatform Services

ADVANTECH

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 - Description of your peripheral attachments
 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Packing List

Before installation, please ensure the following items have been shipped:

- 1 x ARK-3420 Unit
- 1 x DVI to CRT adapter connector
- 2 x Desk/Wall mount plate
- 1 x 4-pin Phoenix DC power connector
- 1 x Utility CD
- 1 x Registration and 2 years Warranty card

Ordering information

Model Number Description

ARK-3420F-S6A1E	Intel® Core® 2 Duo L7500 1.6GHz Compact Embedded Box IPC
ARK-3420F-S1A1E	Intel® Core® 2 Duo U7500 1.06GHz Compact Embedded Box IPC
ARK-3420F-U0A1E	Mobile Intel® Celeron® 550 2.0GHz Compact Embedded Box IPC

Optional accessories

Part Number	Description
1757002161	AC-to-DC Adapter, DC19 V/7.89A 150W, with Phoenix Power Plug, 0 ~ 40° C for Home and Office Use
1702002600	Power cable 3-pin 180 cm, USA type
1700004713	Cable DVI-I to DVI and CRT
1700009398	LVDS cable for ARK-3420
1700009396	LVDS power cable for ARK-3420
1700009399	Digital IO cable for ARK-3420
1700009397	LPT cable for ARK-3420
*9696R00100E	2 slots riser card, 2 x PCIe4
*9696R00200E	2 slots riser card, 2 x PCIe1
*9696R00400E	2 slots riser card, 1 x PCIe4 + 1 x PCI
*9696R00500E	2 slots riser card, 1 x PCIe1 + 1 x PCI

Note: * By project option.

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Chapter 1

General Introduction

This chapter gives background information on ARK-3420 series.

1.1 Introduction

ARK-3420 Compact Embedded Box IPC is an ideal application ready system platform solution. All electronics are protected in a compact sealed aluminum case for easy embedding in customers own housing, or as a stand-alone application, where space is limited and the environment harsh.

A solid sealed aluminum case provides vibration and dust resistance while also providing a passive cooling solution. The ARK-3420 provides system integrators with a turn-key solution and versatile application development path without breaking the bank or missing time to market deadlines.

The ARK-3420 can be used as a standalone system, wall-mounted and desktop mounted. The system accepts a wide range of power supplies (DC power in) and comes in a footprint of only 220 mm x 102.5 mm x 200 mm (8.66" x 4.04" x 7.87"). The rugged cast aluminum case not only provides great protection from EMI, shock/vibration, cold and heat, but also passive cooling for quiet fanless operation.

The ARK-3420 answers this demand by offering 1 x DVI-I interface for dual display, 6 x USB 2.0 ports, 2 x Giga LAN port, audio function, 4 x COM ports and 2 PCI expansion slots; packed into a small rugged unit and powered by an Intel Core 2 Duo processor. It also supports a wide range of input voltages from 9 VDC to 34 VDC. The ARK-3420 Compact Embedded IPC supports 2 x 2.5" SATA HDD and 1 x Compact Flash card for storage options and it can provide the diversified application field.

1.2 Product Feature

1.2.1 General

- Intel® Core® 2 Duo Processor up to 1.6 GHz
- Dual display and support for wide screen with high resolution
- Support 2 GbE, eSATA, 6 USB 2.0 and 4 COMs
- Internal two 2.5-inch SATA HDD drive bay
- Various expansion interfaces for diverse applications
- 6 programmable function keys
- Easy integration, easy maintenance, and wide input voltage range

1.2.2 Display

- **CRT display:** Using a DVI to CRT adapter connector
- **Dual display:** CRT + DVI-D extended by DVI-I Y-cable(Optional)
- **LVDS support:** Support 48-bit LVDS interface (Optional)

1.2.3 Power consumption

- **Typical:** 29 W (CPU is Intel® Core® 2 Duo L7500 1.6 GHz and w/o expansion)
- **Max.:** 35 W (CPU is Intel® Core® 2 Duo L7500 1.6 GHz and w/o expansion)

1.3 Hardware Specification

- **CPU:** Intel® Core 2 Duo L7500, 1.6 GHz/Core 2 Duo U7500, 1.06 GHz/Celeron® M 550, 2.0 GHz
- **System Chipset:** Intel® GME965 + ICH8M
- **BIOS:** AWARD™ 4 Mbit, FWH
- **System Memory:** 2 x 200-pin SODIMM socket, Support DDR2 533/677 MHz, up to 4 GB
- **SSD:** Supports 1 x CF Card TYPE I/II
- **HDD:** Supports 2 x industrial extend temperature grade 2.5" SATA HDD
- **Watchdog Timer:** Single chip Watchdog 255-level interval timer, setup by software
- **I/O Interface:** 2 x RS232, 2 x RS232/422/485 (w/ auto flow control)
- **USB:** 6 x USB 2.0 compliant Ports
- **Audio:** Supports Line-in, Speaker out, Microphone-in
- **Ethernet Chipset:** 2 x Intel 82541PI (Gigabit LAN)
 - Speed: 10/100/1000 Mbps
 - Interface: 2 x RJ45 w/ LED
 - Standard: IEEE 802.3z/ab (1000Base-T) or IEEE 802.3u 100Base-T compliant
- **Expansion:**
 - PCI: 2 slots
 - Mini PCIe: 1 socket
- **Programmable function key:** 6 keys
- **Chipset:** Integrated graphics built in Intel® GME965, Mobile Intel® Graphics Media Accelerator X3100
- **Memory Size:** Dynamic Video Memory Technology (DVMT 4.0; Support up to 384 MB)
- **Resolution:**
 - CRT: Up to QXGA (2048x1536 @ 60 Hz)
 - DVI: Support up to UXGA (1600X1200 @ 75 Hz)
- **Dual Independent:** CRT + DVI-D (Extended by DVI-I Y-cable)

1.4 Mechanical Specification

1.4.1 Dimensions

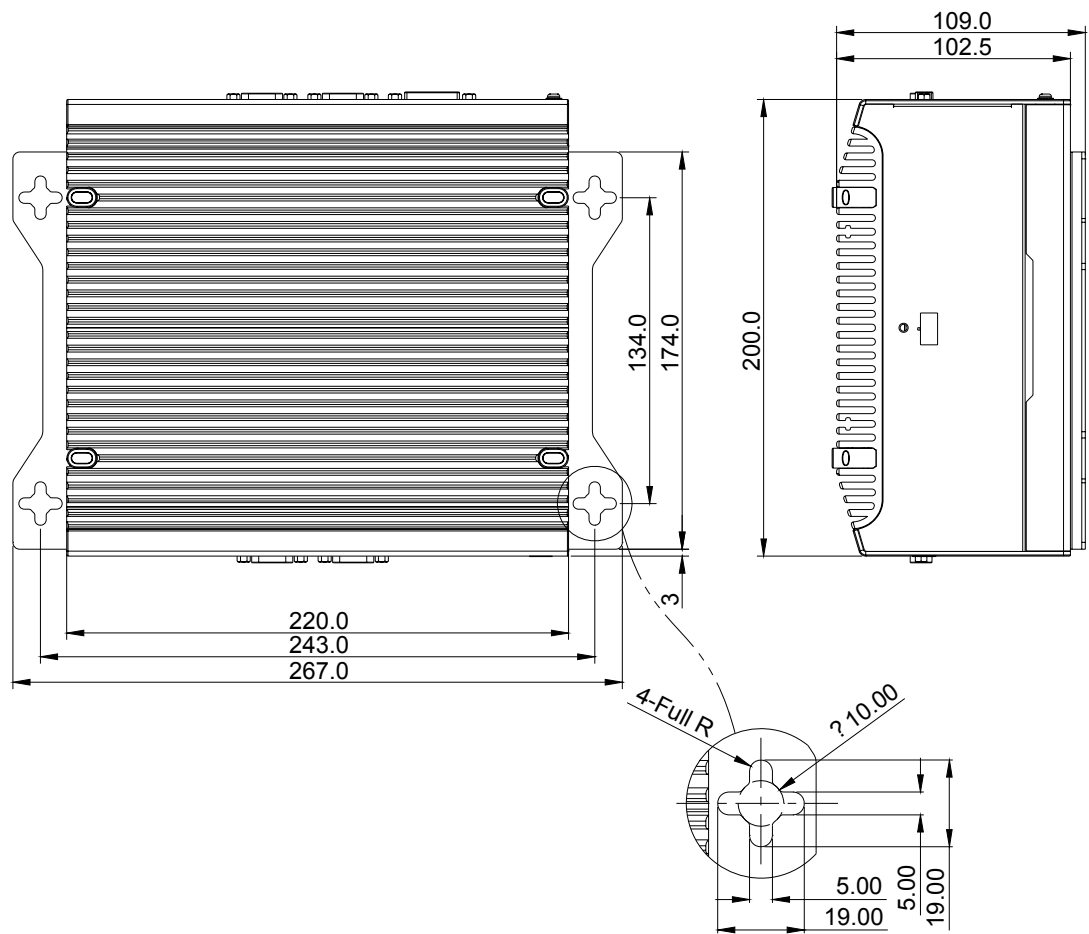


Figure 1.1 ARK-3420 Mechanical Dimension Drawing

1.4.2 Weight

4 kg (8.8 lb)

1.5 Power requirement

1.5.1 System power

Minimum power input: DC 9 V - 34 V 6.0 A - 1.5 A

1.5.2 RTC battery

3 V / 195 mAH BR2032

1.6 Environmental Specifications

1.6.1 Operation temperature

- With Industrial Grade CompactFlash disk: -20 ~ 55° C
- With 2.5-inch extended temperature hard disk -20 to 45° C, with air flow, speed=0.7 m/sec

1.6.2 Relative Humidity

95% @ 40° C (non-condensing)

1.6.3 Storage temperature

-40 ~ 85° C (-40 ~ 185° F)

1.6.4 Vibration loading during operation

- With CompactFlash disk: 5 Grms, IEC 60068-2-64, random, 5 ~ 500 Hz, 1 Oct./min, 1 hr/axis.
- With 2.5-inch hard disk: 1 Grms, IEC 60068-2-64, random, 5 ~ 500 Hz, 1 Oct./min, 1 hr/axis.

1.6.5 Shock during operation

- With CompactFlash disk: 50 G, IEC 60068-2-27, half sine, 11 ms duration
- With hard disk: 20 G, IEC 60068-2-27, half sine, 11 ms duration

1.6.6 Safety

UL, CCC, BSMI

1.6.7 EMC

CE, FCC, CCC, BSMI

Chapter 2

Hardware installation

This chapter introduces external IO and the installation of ARK-3420 Hardware.

2.1 ARK-3420 I/O Indication

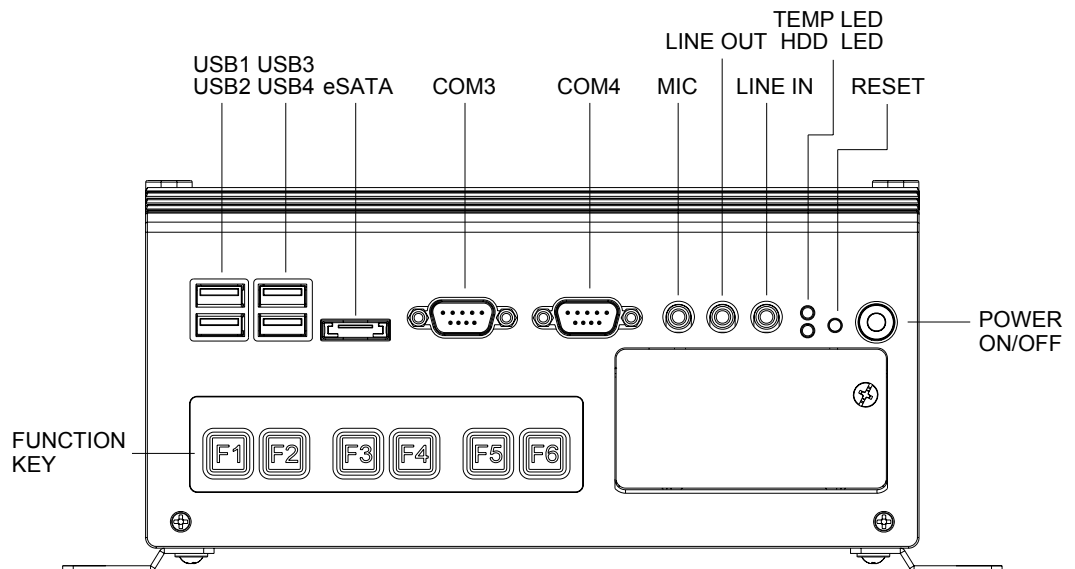


Figure 2.1 ARK-3420 Front View

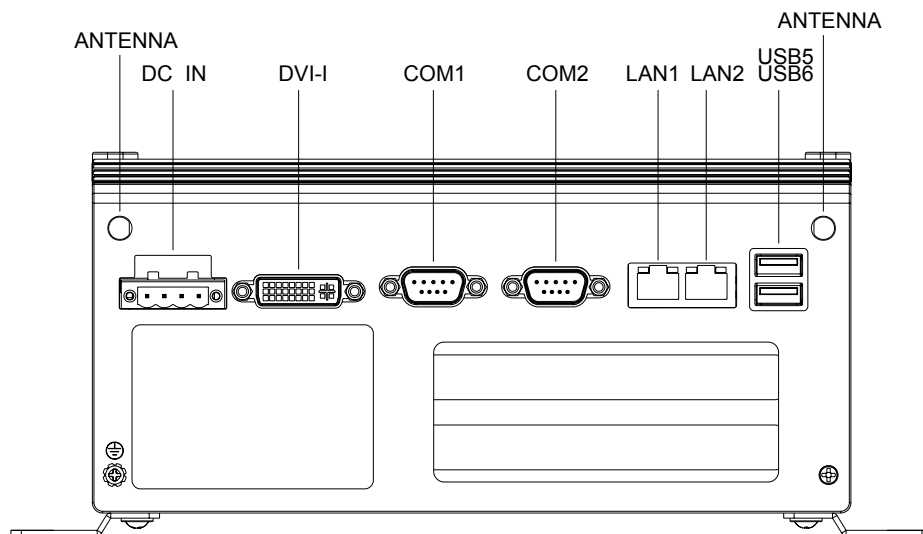


Figure 2.2 ARK-3420 Rear View

2.2 ARK-3420 front side external I/O connectors

2.2.1 Power ON/OFF Button

ARK-3420 comes with a Power On/Off button with LED indicators on the front side to show its On status (Green LED) and Off/Suspend status (Orange LED), that support dual function of Soft Power -On/Off (Instant off or Delay 4 Second), and Suspend.

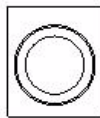


Figure 2.3 Power ON/OFF Button

2.2.2 Reset Button

ARK-3420 has a Reset button on front side. Press the button can to activates the reset function.



Figure 2.4 Reset Button

2.2.3 LED Indicators

There are two LED on ARK-3420 front metal face plate for indicating system status: Thermal LED is for system thermal alarm status; and HDD LED is for HDD & compact flash disk status.

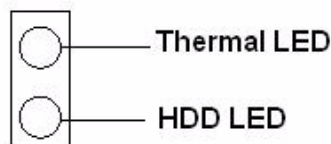


Figure 2.5 LED Indicators

2.2.4 Audio Connector

ARK-3420 offers stereo audio ports by three phone jack connectors of Speaker_Out, Line_In, Mic_In. The audio chip controller is ALC888, Which is compliant with Azalea standard, its Speaker_Out supports 3D surrounding stereo sound and has dual 2.2 W amplifier.

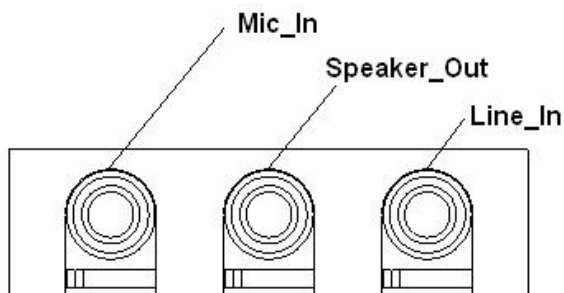


Figure 2.6 Audio jack connectors

2.2.5 COM Connector

ARK-3420 provides four D-sub 9-pin connectors that are serial communication interface ports. The COM1/2 in the rear side only support RS-232, the COM3/4 in the front side can support RS-232/422/485 mode by BIOS selection. Default setting of these four ports are RS-232. If you want to use RS-422/485 of COM3/4, you can find the selecting item in the BIOS setup menu.

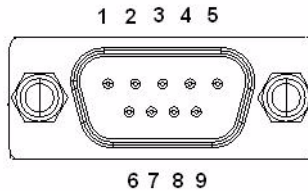


Figure 2.7 COM port connector

Table 2.1: COM standard serial port pin assignments

	RS-232	RS-422	RS-485
Pin	Signal Name	Signal Name	Signal Name
1	DCD	Tx-	DATA-
2	RxD	Tx+	DATA+
3	TxD	Rx+	NC
4	DTR	Rx-	NC
5	GND	GND	GND
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

Note: NC represents "No Connection".

2.2.6 eSATA Connector

ARK-3420 has a 7 pin external connector for eSATA device. That is fully compliant with SATA I/SATA II standards, its can be access with external SATA I/SATA II device then up to 300MB/sec.



Figure 2.8 eSATA connector

2.2.7 USB Connector

ARK-3420 provides six connectors of USB interface, which give complete Plug & Play and hot swapping for up to 127 external devices. The USB interface complies with USB UHCI, Rev. 2.0 compliant. The USB interface can be disabled in the system BIOS setup. Please refer to Table. 2.2 for its pin assignments

The USB connectors are used for connecting any device that conforms to the USB interface. Many recent digital devices conform to this standard. The USB interface supports Plug and Play, which enables you to connect or disconnect a device whenever you want, without turning off the computer.

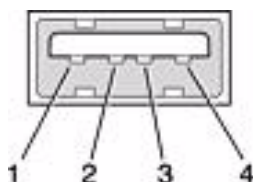


Figure 2.9 USB connector

Table 2.2: USB Connector

Pin	Signal name	Pin	Signal name
1	VCC	2	USB_data-
3	USB_data+	4	GND

2.2.8 Compact Flash Card

ARK-3420 is equipped with an external CF card. You can find the installation in Chapter 2.2.

2.3 ARK-3420 rear side external I/O connectors

2.3.1 Power Input Connector

ARK-3420 comes with a four pins header that carries 9~34 VDC external power input.

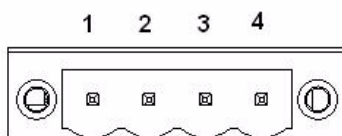


Figure 2.10 Power Input Connector

Table 2.3: Power connector pin assignments

Pin	Signal Name
1	GND
2	+9 ~ 34 VDC
3	+9 ~ 34 VDC
4	GND

2.3.2 Digital Visual Interface Connector (DVI-I)

The ARK-3420 offers a integrate Digital Visual Interface connector by a D-sub 24-pin female DVI-I connector, it integrates analog and digital video signal. This supports high-speed, high-resolution digital display and traditional analog display.

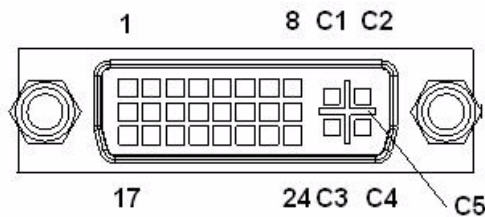


Figure 2.11 DVI-I connector

Table 2.4: DVI-I Connector pin assignments

Pin	Signal Name	Pin	Signal Name
1	TMDS Data 2-	2	TMDS Data 2+
3	TMDS Data 2/4 shield	4	TMDS Data 4-
5	TMDS Data 4+	6	DDC clock
7	DDC data	8	Analog vertical sync
9	TMDS Data 1-	10	TMDS Data 1+
11	TMDS Data 1/3 shield	12	TMDS Data 3-
13	TMDS Data 3+	14	+5 V
15	Ground	16	Hot plug detect
17	TMDS data 0-	18	TMDS data 0+
19	TMDS data 0/5 shield	20	TMDS data 5-
21	TMDS data 5+	22	TMDS clock shield
23	TMDS clock+	24	TMDS clock-
C1	Analog red	C2	Analog green
C3	Analog blue	C4	Analog horizontal sync
C5	Analog ground		

2.3.3 Ethernet Connector (LAN)

ARK-3420 provides two RJ45 connectors of Gb LAN interface, they are equipped with two Intel 82541PI Ethernet controllers that are fully compliant with IEEE 802.3u 10/100/1000Base-T CSMA/CD standards. The Ethernet port provides a standard RJ-45 jack connector with LED indicators on the front side to show its Active/Link status (Green LED) and Speed status (Yellow LED).

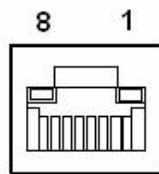


Figure 2.12 Ethernet connector

Table 2.5: RJ-45 Connector pin assignments

Pin	10/100/1000BaseT Signal Name
1	TX+
2	TX-
3	RX+
4	MDI2+
5	MDI2-
6	RX-
7	MDI3+
8	MDI3-

2.4 Memory Installation

Step 1: Remove the Heatsink by loosen the fixing screws.

Step 2: Remove the heatspreader by unscrew the 5 screws.

Step 3: Insert the memory module into the SODIMM socket.

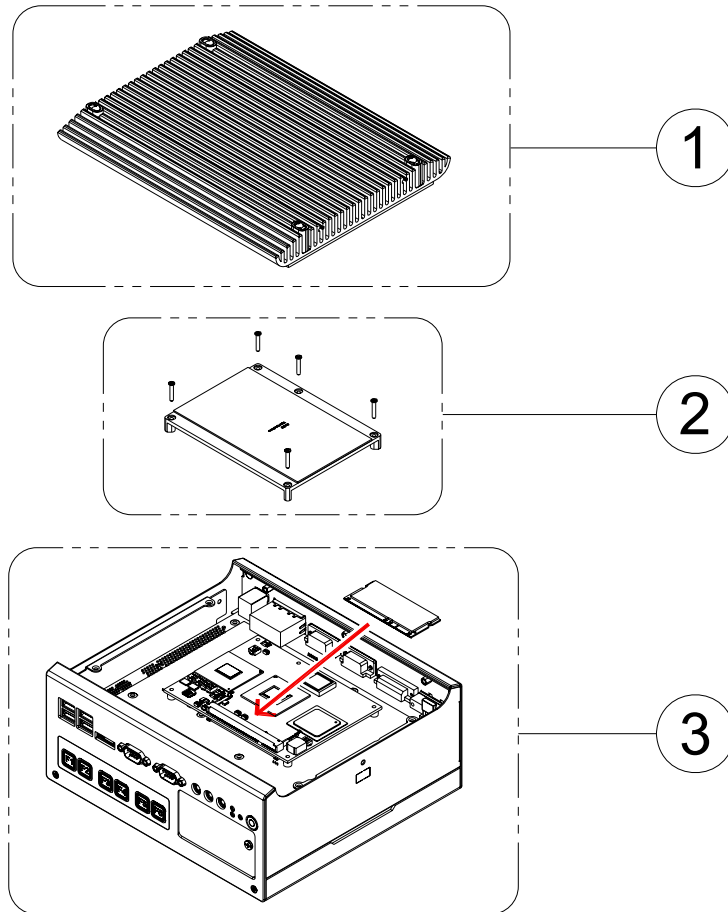


Figure 2.13 Memory Installation

2.5 Compact Flash installation

Step 1: Open the front CF/HDD door by loosen the door screw.

Step 2: Insert the CF card into the CF socket.

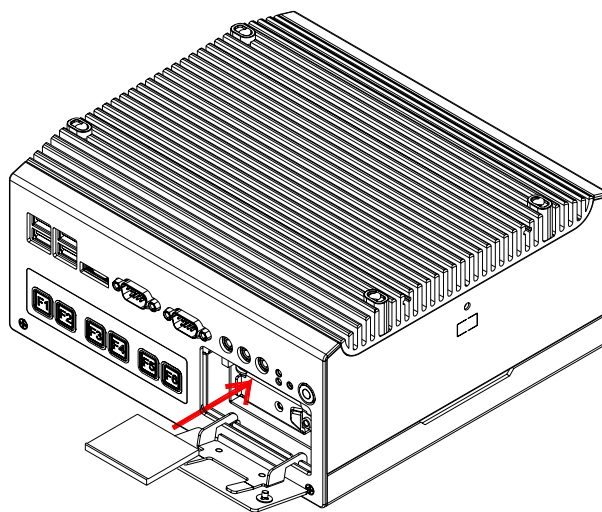


Figure 2.14 CF Card installation

2.6 HDD installation

2.6.1 Internal fixed HDD installation

Step 1: Remove the bottom cover by unscrew the 4 screws.

Step 2: Install the 2.5-inch SATA HDD by 4 HDD screws.

Step 3: Connect the SATA signal cable and power cable with the fixing 2.5-inch HDD.

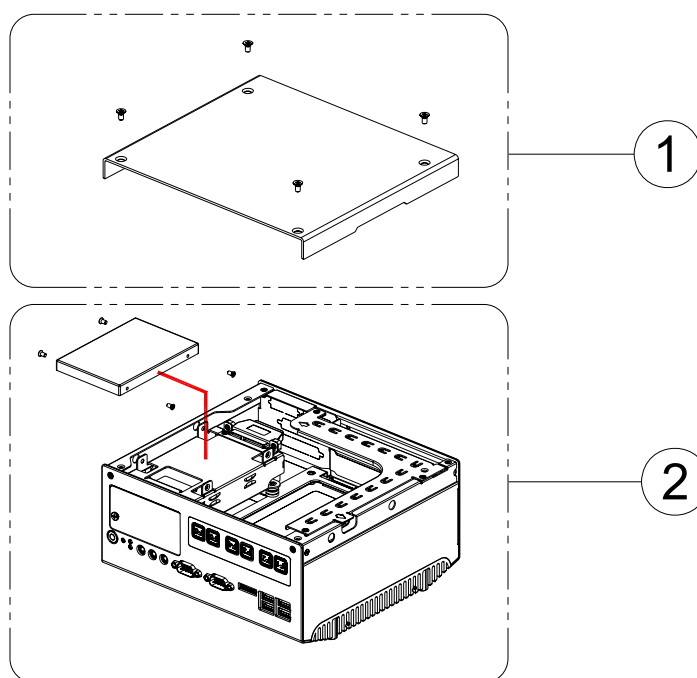


Figure 2.15 Internal Fixed HDD Installation

2.6.2 Removable HDD installation

Step 1: Open the front CF/HDD door by loosen the door screw.

Step 2: Assemble the 2.5-inch SATA HDD on the loader by 4 HDD screws.

Step 3: Slide in HDD loader along the rails to the end and fix the lever screw.

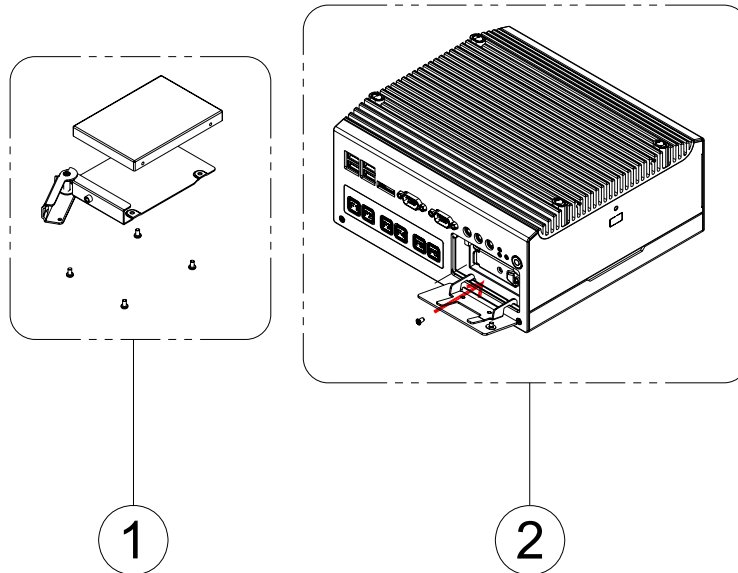


Figure 2.16 Removable HDD Installation

2.7 PCI card installation

Step 1: Remove the bottom cover by unscrew the 4 screws. (Refer Chapter 2.6.1)

Step 2: Remove the Riser card module.

Step 3: Insert the PCI extension card into the PCI slot of the riser card module.

Step 4: Assemble the Riser card module back.

Step 5: Assemble the bottom cover.

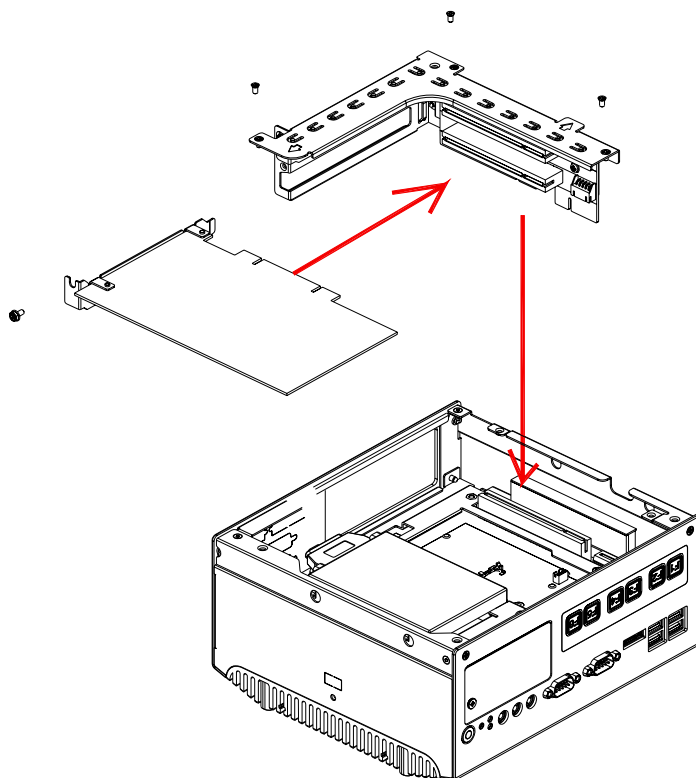


Figure 2.17 Removable HDD Installation

2.8 Mini PCIe installation

Step 1: Open the bottom cover and remove the Riser card module. (Refer Chapter 2.7)

Step 2: Insert the Mini PCIe card into the Mini PCIe socket and latched.

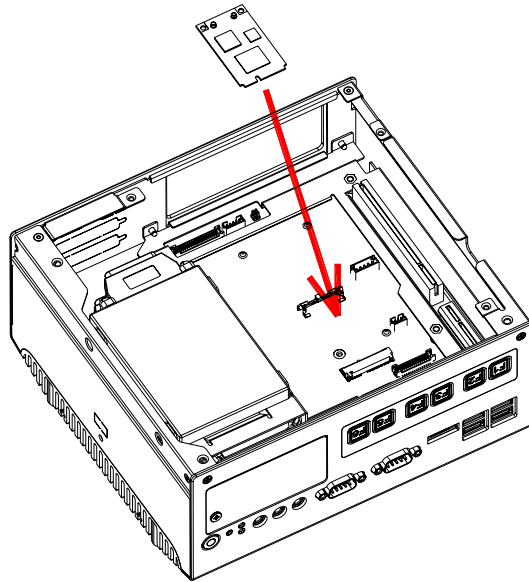


Figure 2.18 Mini PCIe Card Installation

2.9 Antenna installation

Step 1: Remove the Heatsink by loosening the fixing screws. (Refer Chapter 2.4)

Step 2: Pass the internal antenna cable jack through the antenna hole on the rear panel and fix it by tightening the matched nut.

Step 3: Put on the external antenna cable.

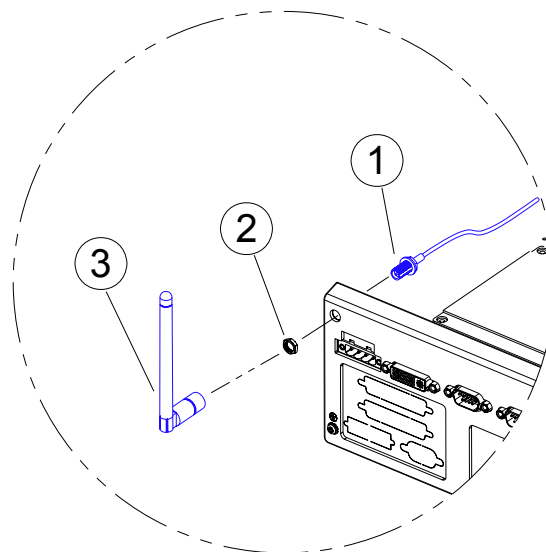


Figure 2.19 Antenna installation

2.10 Optional cable installation

Open the bottom cover and see the below drawing and table for the option cables installation and connection.

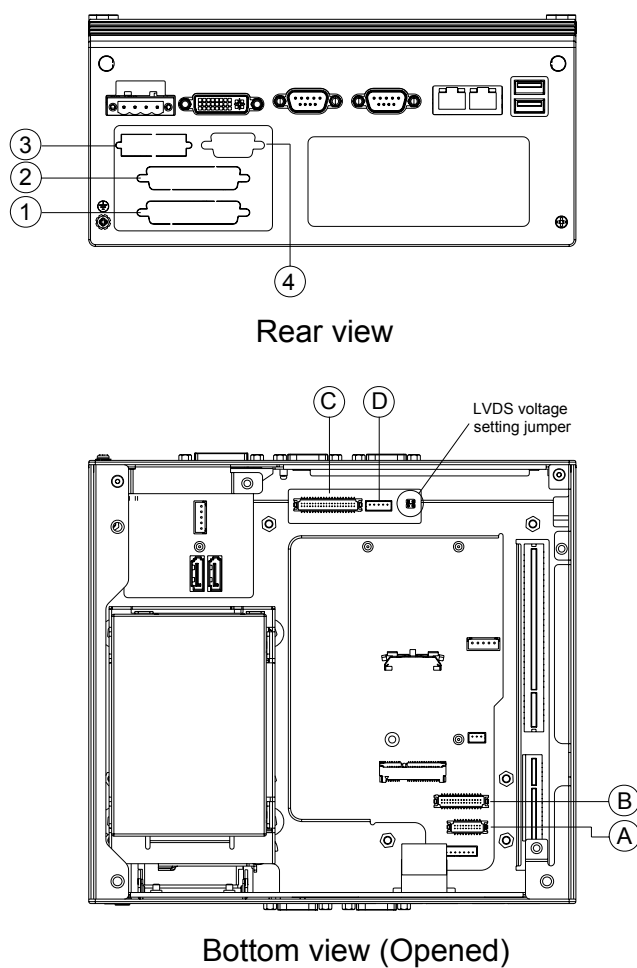


Figure 2.20 Removable HDD Installation

	Outer connector fixing(connection)	Inner connector fixing(connection)
DIO cable (P/N: 1700009399)	1	A
LPT cable (P/N: 1700009397)	2	B
LVDS cable (P/N: 1700009398)	3	C
LVDS power cable (P/N: 1700009396)*	4	D

Note! When the LVDS panel power source is provided from the system, the LVDS voltage jumper needs to be selected.



Chapter 3

BIOS settings

This chapter introduces how to set BIOS configuration data.

3.1 BIOS Introduction

Advantech provides full-featured AwardBIOS 6.0 and delivers the superior performance, compatibility and functionality that system integrators demand.

The modular, adaptable AwardBIOS 6.0 supports the broadest range of third-party peripherals and all popular chipsets, plus Intel, AMD, nVidia, VIA, and compatible CPUs from 386 through Pentium and AMD Geode, K7 and K8 (including multiple processor platforms), and VIA Eden C3 and C7 CPU.

You can use Advantech's utilities to select and install features as needed.

3.2 BIOS Setup

The ARK-3420 series system has build-in AwardBIOS with a CMOS SETUP utility which allows user to configure required settings or to activate certain system features.

The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to the CMOS RAM.

When the power is turned on, press the button during the BIOS POST (Power-On Self Test) will take you to the CMOS SETUP screen.

CONTROL KEYS

< ↑ >< ↓ >< ← >< → >	Move to highlight item
----------------------	------------------------

<Enter>	Select Item
---------	-------------

<Esc>	Main Menu - Quit and not save changes into CMOS
-------	---

<Esc>	Sub Menu - Exit current page and return to Main Menu
-------	--

<Page Up/+>	Increase the numeric value or make changes
-------------	--

<Page Down/->	Decrease the numeric value or make changes
---------------	--

<F1>	General help, for Setup Sub Menu
------	----------------------------------

<F2>	Item Help
------	-----------

<F5>	Load Previous Values
------	----------------------

<F7>	Load Optimized Default
------	------------------------

<F10>	Save all CMOS changes
-------	-----------------------

3.2.1 Main Menu

Press to enter AwardBIOS CMOS Setup Utility, the Main Menu will appear on the screen. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.

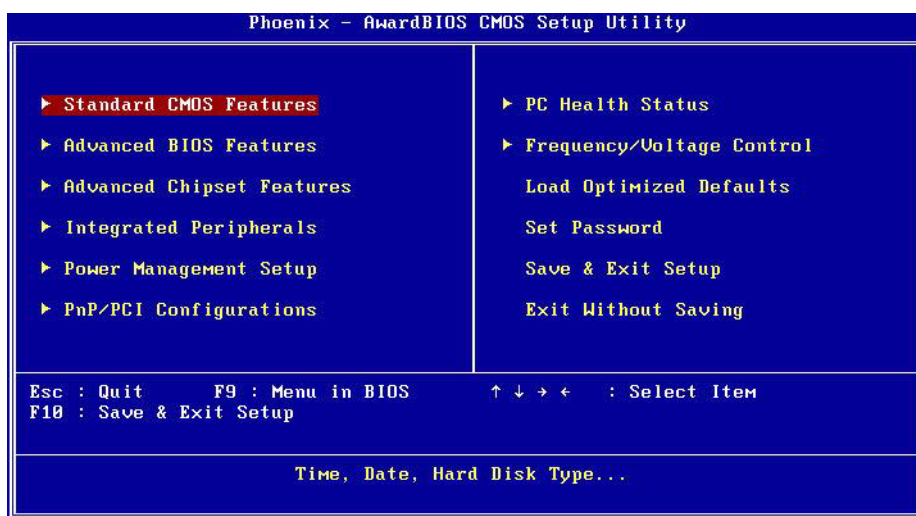


Figure 3.1 Award BIOS CMOS Setup Utility

- **Standard CMOS Features**
This setup page includes all the items in standard compatible BIOS.
- **Advanced BIOS Features**
This setup page includes all the items of Award BIOS enhanced features.
- **Advanced Chipset Features**
This setup page includes all the items of Chipset configuration features.
- **Integrated Peripherals**
This setup page includes all onboard peripheral devices.
- **Power Management Setup**
This setup page includes all the items of Power Management features.
- **PnP/PCI Configurations**
This setup page includes PnP OS and PCI device configuration.
- **PC Health Status**
This setup page includes the system auto detect CPU and system temperature, voltage, fan speed.
- **Frequency/Voltage Control**
This setup page includes CPU host clock control, frequency ratio and voltage.
- **Load Optimized Defaults**
This setup page includes Load system optimized value, and the system would be in best performance configuration.
- **Set Password**
Establish, change or disable password.
- **Save & Exit Setup**
Save CMOS value settings to CMOS and exit BIOS setup.
- **Exit Without Saving**
Abandon all CMOS value changes and exit BIOS setup.

3.2.2 Standard CMOS Features

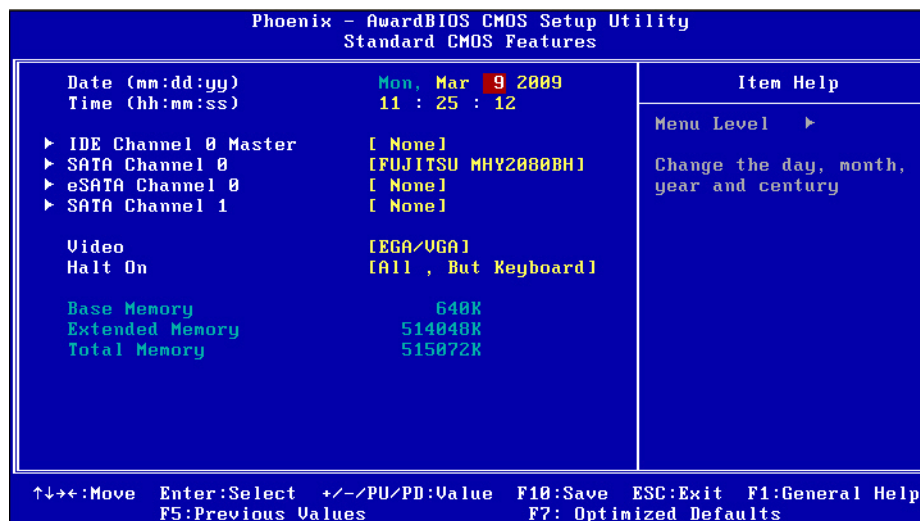


Figure 3.2 Award BIOS Standard CMOS Features

- **Date**

The date format is <weekday>, <month>, <day>, <year>.

 - Weekday From Sun to Sat, determined and display by BIOS only
 - Month From Jan to Dec.
 - Day From 1 to 31
 - Year From 1999 through 2098
- **Time**

The time format in <hour> <minute> <second>, is based on 24-hour time.
- **IDE Channel 0 Master**

CF Card Auto-Detection Press "Enter" for automatic device detection.
- **SATA Channel 0/1**

SATA HDD Auto-Detection Press "Enter" for automatic device detection.
- **eSATA Channel 0**

eSATA HDD Auto-Detection Press "Enter" for automatic device detection.
- **Video**

The item determines that VGA display support type.

 - EGA/VGA Support VGA color mode.
 - CGA 40 Support VGA color mode.
 - CGA 80 Support VGA color mode.
 - MONO Support VGA mono mode.

- **Halt on**

The item determines whether the computer will stop if an error is detected during power up.

No Errors	The system boot will not stop for any error
All Errors	Whenever the BIOS detects a non-fatal error the system will be stopped.
All, But Keyboard	The system boot will not stop for a keyboard error; it will stop for all other errors. (Default value)
All, But Diskette	The system boot will not stop for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not stop for a keyboard or disk error; it will stop for all other errors.
- **Base Memory**

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system.
- **Extended Memory**

The POST of the BIOS will determine the amount of extended memory (above 1 MB in CPU's memory address map) installed in the system.
- **Total Memory**

This item displays the total system memory size.

3.2.3 Advanced BIOS Features

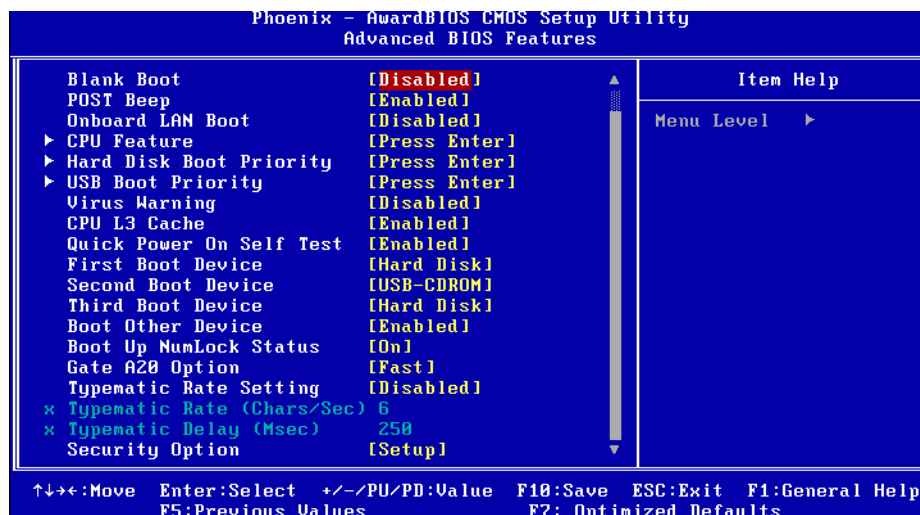


Figure 3.3 Award BIOS Advanced CMOS Features

- **Blank Boot [Disabled]**
This item allows user to enable/disable BIOS POST screen output
- **POST Beep [Enabled]**
This item allows user to enable/disable POST beep sound.
- **Onboard LAN Boot [Disabled]**
This item allows user to select boot sequence for LAN1 or LAN2.
- **CPU Feature**
This item allows user to adjust CPU features, CPU ratio, VID and Thermal and special feature like XD flag.
- **Hard Disk Boot Priority**
This item allows user to select boot sequence for system device HDD, SCSI, RAID.
- **USB Boot Priority**
This item allows user to select boot sequence for USB devices.
- **Virus Warning [Disabled]**
This item allows user to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection.
- **CPU L3 Cache [Enabled]**
This item allows user to enable CPU L3 cache.
- **Hyper-Threading Technology [Enabled]**
This item allows user to enable supported on the Intel® Pentium® 4 Processor with HT Technology.
- **Quick Power On Self Test [Enabled]**
This field speeds up the Power-On Self Test (POST) routine by skipping retesting a second, third and fourth time. Setup setting default is enabled.

- **First / Second / Third / Other Boot Drive**

Floppy	Select boot device priority by Floppy.
Hard Disk	Select boot device priority by Hard Disk.
CDROM	Select boot device priority by CDROM.
USB Device	Select boot device priority by USB Device.
ZIP 100	Select boot device priority by ZIP.
USB-FDD	Select boot device priority by USB-FDD.
USB-ZIP	Select boot device priority by USB-ZIP.
USB-CDROM	Select boot device priority by USB-CDROM.
LAN	Select boot device priority by LAN.
Disabled	Disable this boot function.
- **Boot Up NumLock Status [Enabled]**

This item enables users to activate the Number Lock function upon system boot
- **Gate A20 Option [Fast]**

This item enables users to switch A20 control by port 92 or not.
- **Typematic Rate Setting**

This item enables users to set the two typematic controls items.

This field controls the speed at

 - Typematic Rate (Chars/Sec)

This item controls the speed at system registers repeated keystrokes.
Eight settings are 6, 8, 10, 12, 15, 20, 24 and 30.
 - Typematic Delay (Msec)

This item sets the time interval for displaying the first and second characters.
Four delay rate options are 250, 500, 750 and 1000.
- **Security Option [Setup]**

System	Correct password must be supplied for both System boot, and for Setup page access.
Setup	Correct password must be supplied for access to Setup page. (Default value)
- **APIC Mode [Enabled]**

This item allows user to enabled of disabled “Advanced Programmable Interrupt Controller”. APIC is implemented in the motherboard and must be supported by the operating system, and it extends the number of IRQ's available.

3.2.4 Advanced Chipset Features

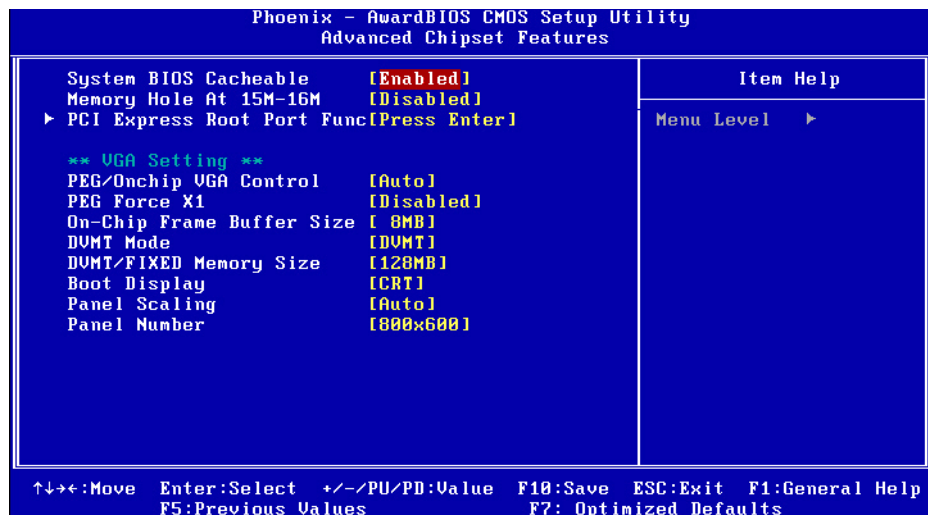


Figure 3.4 Award BIOS Advanced Chipset Features

Note! This “Advanced Chipset Features” screen controls the configuration of the board’s chipset for fine-tuning system performance. Screen options depend on the specific chipset. It is strongly recommended that only technical users make changes to the default settings..



- **System BIOS Cacheable [Enabled]**
This item allows the system BIOS to be cached to allow faster execution and better performance.
- **Memory Hole At 15 M-16 M [Disabled]**
This item reserves 15MB-16MB memory address space to ISA expansion cards that specifically require the setting. Memory from 15MB-16MB will be unavailable to the system because of the expansion cards can only access memory at this area.
- **PCI Express Root port Func [Press Enter]**
This item allows the user to adjust PCIe port on, off or auto.
- **PEG/Onboard VGA Control [Auto]**
This item allows the user to select whether onboard graphics processor or the PCI Express card.
- **PEG Force X1 [Disabled]**
This item allows the user to convert a PCI Express X16 slot to PCI Express X1 slot.
- **On-Chip Frame Buffer Size [8 MB]**
This item allows the user to adjust on-chip graphics of memory buffer.
- **DVMT Mode [DVMT]**
Intel's Dynamic Video Memory Technology (DVMT) takes that concept further by allowing the system to dynamically allocate memory resources according to the demands of the system at any point in time. The key idea in DVMT is to improve the efficiency of the memory allocated to either system or graphics processor.
The BIOS feature that controls all this is the DVMT Mode BIOS feature. It allows you to select the DVMT operating mode.

Fixed	the graphics driver will reserve a fixed portion of the system memory as graphics memory. This ensures that the graphics processor has a guaranteed amount of graphics memory but the downside is once allocated, this memory cannot be used by the operating system even when it is not in use.
DVMT	the graphics chip will dynamically allocate system memory as graphics memory, according to system and graphics requirements. The system memory is allocated as graphics memory when graphics-intensive applications are running but when the need for graphics memory drops, the allocated graphics memory can be released to the operating system for other uses.
BOTH	the graphics driver will allocate a fixed amount of memory as dedicated graphics memory, as well as allow more system memory to be dynamically allocated between the graphics processor and the operating system.

- **DVMT/FIXED Memory Size [128 MB]**

This item allows the user to adjust DVMT/FIXED graphics memory size.

- **Boot Display [DVI+CRT]**

This item allows the user to decide that display mode.

Auto	Select boot display mode by Auto.
CRT	Select boot display mode by CRT.
LFP	Select boot display mode by LFP.
CRT+LFP	Select boot display mode by CRT+LFP.
DVI	Select boot display mode by DVI.
DVI+CRT	Select boot display mode by DVI+CRT.

- **Panel Scaling [Auto]**

This item allows the user to control panel scaling feature.

- **Panel Number [800x600]**

These fields allow you to select the LCD Panel type. The default values for these ports are:

- 640 x 480, 18 bits
- 800 x 600, 18 bits
- 1024 x 768, 18 bits
- 1280 x 1024, 48 bits

3.2.5 Integrated Peripherals

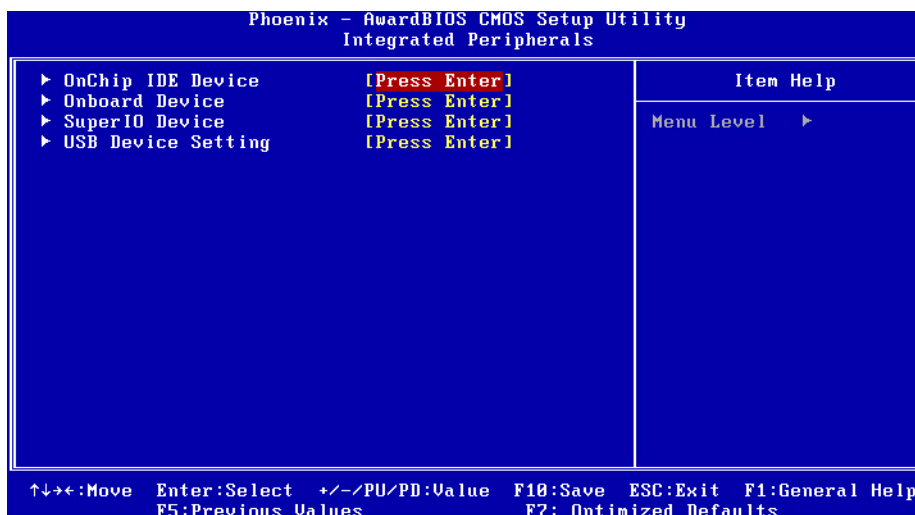


Figure 3.5 Award BIOS Integrated Peripherals

Note! This "Integrated Peripherals" option controls the configuration of the board's chipset, includes IDE, ATA, SATA, USB, AC97, MC97 and Super IO and Sensor devices, this page depends on the particular chipset installed.



- **OnChip IDE Device**
This item enables users to set the OnChip IDE device status, includes enable IDE devices and setting PIO and DMA access mode, and some of new chipset also support for SATA device (Serial-ATA).
- **Onboard Device**
This item enables users to set the Azalia/AC97 status enable or disable.
- **Super IO Device**
This item enables users to set the Super IO device status, includes enable Floppy, COM, LPT, IR and control GPIO and Power fail status.
- **Onboard Serial port 1 [3F8/IRQ4]**
This item allows user to adjust serial port 1 of address and IRQ.
- **Onboard Serial port 2 [2F8/IRQ3]**
This item allows user to adjust serial port 2 of address and IRQ.
- **Onboard Serial port 3 [3E8/IRQ5]**
This item allows user to adjust serial port 3 of address and IRQ.
- **SP3 AutoFlow Control [Disable]**
Auto flow control is used in RS-485, is used to tri-state the transmitter when no other data is available, so that other nodes can use the shared lines.
When auto flow control is enable, the device monitors the local output buffer for not empty and empty conditions. If enable, the flow control will force signal to the desired polarity under the empty or not empty condition.
- **Onboard Serial port 3 Mode [RS232]**
This item allows user to adjust serial port 3 mode of RS232/RS422/RS485.
- **Onboard Serial port 4 [2E8/IRQ10]**
This item allows user to adjust serial port 4 of address and IRQ.

- **SP4 AutoFlow Control [Disable]**

Auto flow control is used in RS-485, is used to tri-state the transmitter when no other data is available, so that other nodes can use the shared lines.

When auto flow control is enable, the device monitors the local output buffer for not empty and empty conditions. If enable, the flow control will force signal to the desired polarity under the empty or not empty condition.
- **Onboard Serial port 4 Mode [RS232]**

This item allows user to adjust serial port 4 mode of RS232/RS422/RS485.
- **Onboard Parallel Port [378/IRQ7]**

This item allows user to adjust parallel port of address and irq.
- **Parallel Port Mode [Standard]**

This item allows user to adjust parallel port mode of standard/SPP/EPP and ECP.
- **ECP Mode Use DMA [3]**

This item allows user to adjust ECP DMA resource.
- **USB Device Setting**

This item enables users to set the OnChip USB functions, includes enable USB1.1/2.0 controller and operation mode, and USB keyboard/mouse/storage functions.

3.2.6 Power Management Setup

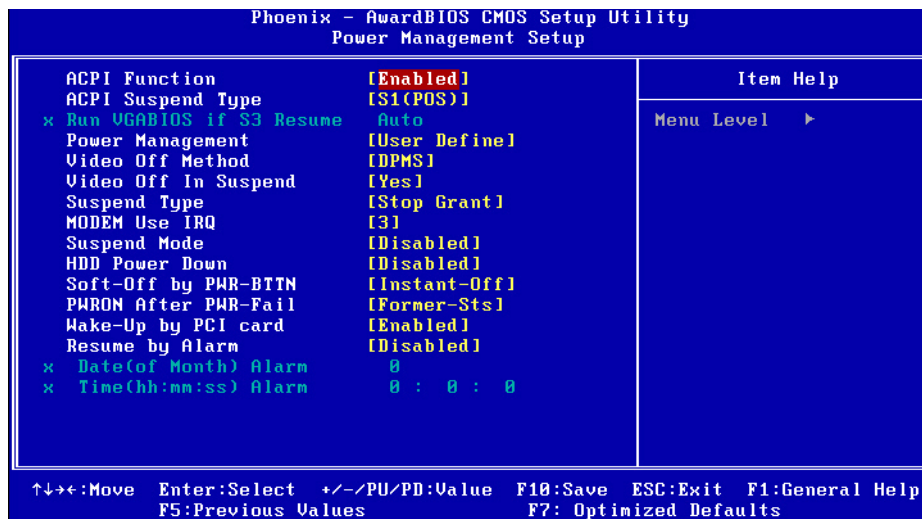


Figure 3.6 Award BIOS Power Management Setup

Note! This “Power Management Setup” screen configures the system to most effectively save energy while operating in a manner consistent with your computer use.



- **ACPI Function [Enabled]**
This item defines the ACPI (Advanced Configuration and Power Management) feature that makes hardware status information available to the operating system, and communicate PC and system devices for improving the power management.
- **ACPI Suspend Type [S1 (POS)]**
This item allows user to select sleep state when suspend.
 - S1(POS) The suspend mode is equivalent to a software power down;
 - S3(STR) The system shuts down with the exception of a refresh current to the system memory.
 - S1&S3 Allow by OS.
- **Run VGA BIOS if S3 Resume [Auto]**
This item allows system to reinitialize VGA BIOS after system resume from ACPI S3 mode.
- **Power Management [User Define]**
This item allows user to select system power saving mode.
 - Min Saving Minimum power management. Suspend Mode=1 hr.
 - Max Saving Maximum power management. Suspend Mode=1 min.
 - User Define Allows user to set each mode individually.
Suspend Mode= Disabled or 1 min ~1 hr.

- **Video Off Method [DPMS]**
 This item allows user to determine the manner in which the monitor is blanked.
 V/H SYNC+Blank This option will cause system to turn off vertical and horizontal synchronization ports and write blanks to the video buffer.

Blank Screen	This option only writes blanks to the video buffer.
DPMS	Initial display power management signaling.
- **Video Off In Suspend [Yes]**
 This item allows user to turn off Video during system enter suspend mode.
- **Suspend Type [Stop Grant]**
 This item allows user to determine the suspend type.
- **Modem use IRQ [3]**
 This item allows user to determine the IRQ which the MODEM can use.
- **Suspend Mode [Disabled]**
 This item allows user to determine the time of system inactivity, all devices except the CPU will be shut off.
- **HDD Power Down Mode [Disabled]**
 This item allows user to determine the time of system inactivity, the hard disk drive will be powered down.
- **Soft-Off by PWR-BTTN [Instant-Off]**
 This item allows user to define function of power button.

Instant-Off	Press power button then Power off instantly.
Delay 4 Sec	Press power button 4 sec. to Power off.
- **PWRON After PWR-Fail [Former-Sts]**
 This item allows user to select system power status after power loss.
- **Wake-Up by PCI card [Enabled]**
 This item allows user to defines PCI cards to wake up the system from the suspend mode.
- **Resume by Alarm [Disabled]**
 This item allows user to enable and key in Date/time to power on system

Disabled	Disable this function.
Enabled	Enable alarm function to power on system
Data (of month)	Alarm1-31
Time (HH:MM:SS)	Alarm(0-23) : (0-59) : 0-59)

3.2.7 PnP/PCI Configurations

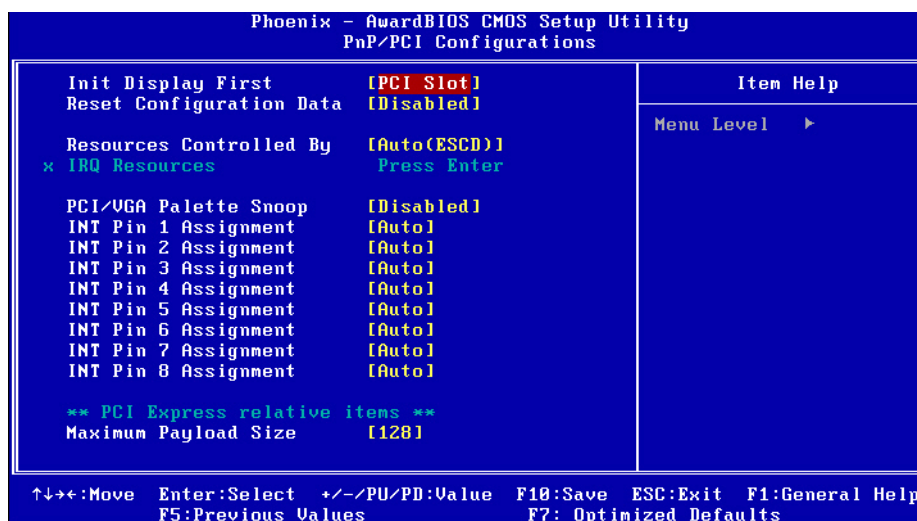


Figure 3.7 Award BIOS PnP/PCI Configurations

Note! Use this "PnP/PCI Configurations" option for setting up the IRQ and DMA (both PnP and PCI) bus assignments.



- **Init Display First [PCI Slot]**
This item is setting for start up Video output from PCI or Onboard device.
- **Reset Configuration Data [Disabled]**
This item allow user to clear any PnP configuration data stored in the BIOS.
- **Resources Controlled By [Auto (ESCD)]**
 - IRQ Resources
This item allows you respectively assign an interruptive type for IRQ-3, 4, 5, 7, 9, 10, 11, 12, 14, and 15.
- **PCI VGA Palette Snoop [Disabled]**
The item is designed to solve problems caused by some non-standard VGA cards. A built-in VGA system does not need this function.
- **INT Pin 1~8 Assignment [Auto]**
The interrupt request (IRQ) line assigned to a device connected to the PCI interface on your system.
- **Maximum payload Size [128]**
The item allows user to adjust maximum TLP (Transaction Layer Packet) payload size.

3.2.8 PC Health Status

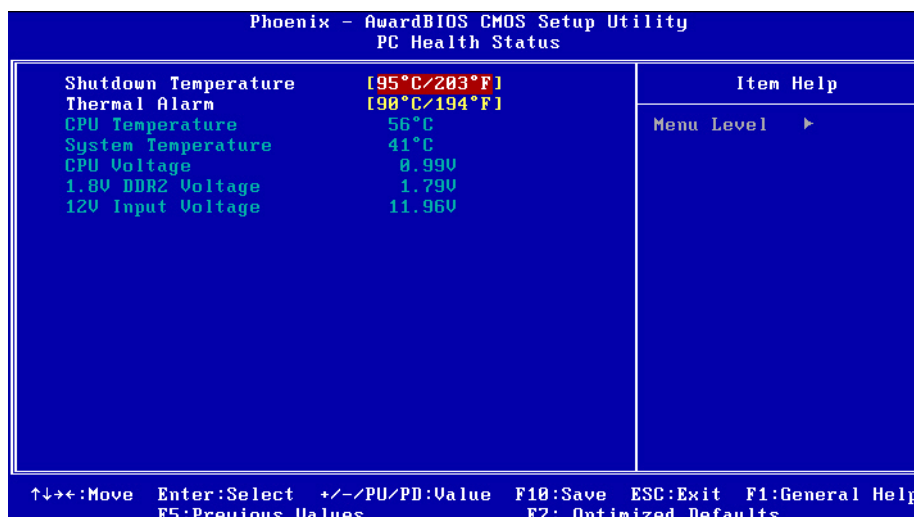


Figure 3.8 Award BIOS PC Health Status

Note! This “PC Health Status” screen reports the Thermal, FAN and Voltage status of the board. This page this page depends on the particular chipset installed.



- **Shutdown Temperature [95°C/203°F]**
This item allow user to set the temperature to notify the ACPI OS to shutdown the system.
- **Thermal Alarm [90°C/194°F]**
This item allow user to set the temperature to notify the ACPI OS to tiger the thermal alarm LED.
- **CPU Temperature [Show Only]**
This item displays current CPU temperature.
- **Local Temperature [Show Only]**
This item displays current system temperature.
- **CPU/ 1.8 V DDR2/12 V Input Voltage [Show Only]**
This item displays current CPU and system Voltage.

3.2.9 Frequency/voltage Control

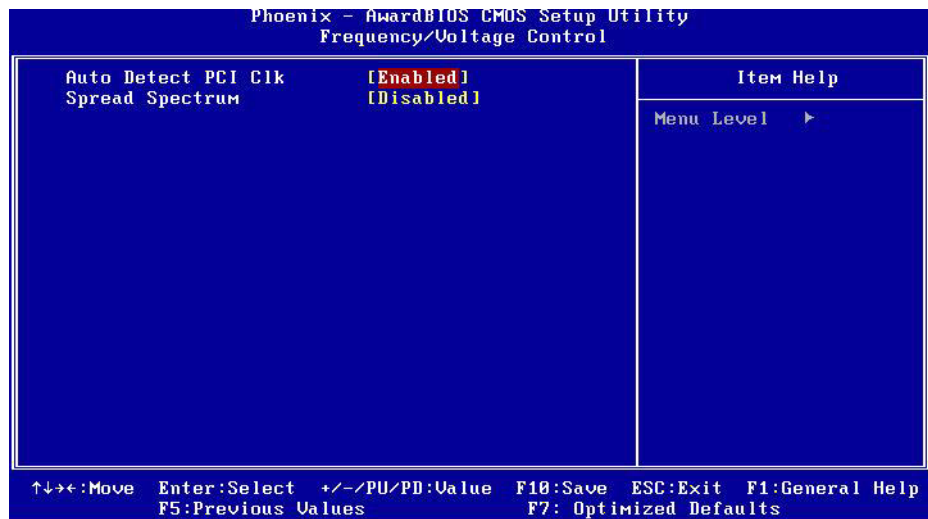


Figure 3.9 Award BIOS Frequency/Voltage Control

Note! *This “Frequency/Voltage Control” screen controls the CPU Host and PCI frequency, this page this page depends on the particular CPU and chipset installed; some items will only show up when you install a processor which supports those functions..*



- **Auto Detect PCI Clk [Enabled]**
This item enables users to set the PCI Clk by system automatic detection or by manual.
- **Spread Spectrum [Disabled]**
This item enables users to set the spread spectrum modulation.

3.2.10 Load Optimized Defaults

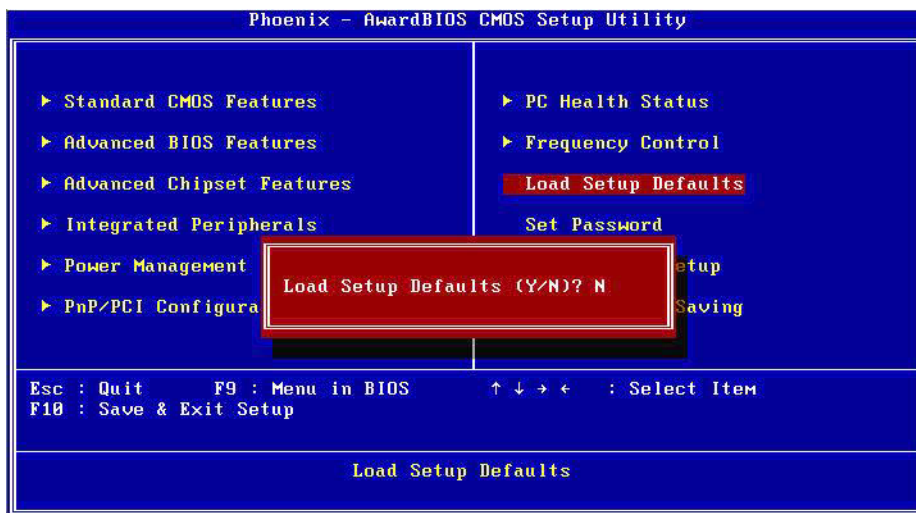


Figure 3.10 Award BIOS Load Setup Defaults

Note! *Load Optimized Defaults loads the default system values directly from ROM. If the stored record created by the Setup program should ever become corrupted (and therefore unusable).*



These defaults will load automatically when you turn the ARK-3420 Series system on.

3.2.11 Set Password

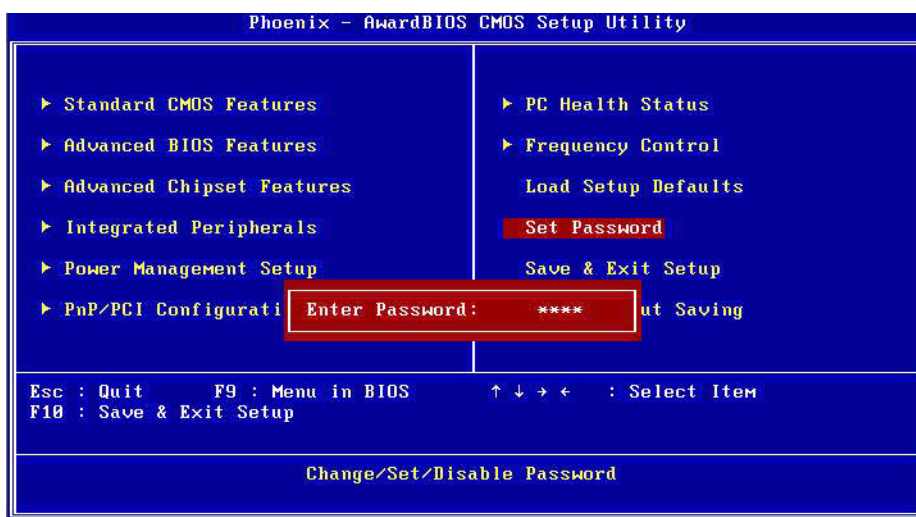


Figure 3.11 Award BIOS Set Password

Note! *To enable this feature, you should first go to the Advanced BIOS Features menu, choose the Security Option, and select either Setup or System, depending on which aspect you want password protected. Setup requires a password only to enter Setup. System requires the password either to enter Setup or to boot the system. A password may be at most 8 characters long.*



To Establish Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see “Enter Password”, enter the desired password and press <Enter>.
3. At the “Confirm Password” prompt, retype the desired password, then press <Enter>.
4. Select Save to CMOS and EXIT, type <Y>, then <Enter>.

To Change Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see “Enter Password”, enter the existing password and press <Enter>.
3. You will see “Confirm Password”. Type it again, and press <Enter>.
4. Select Set Password again, and at the “Enter Password” prompt, enter the new password and press <Enter>.
5. At the “Confirm Password” prompt, retype the new password, and press <Enter>.
6. Select Save to CMOS and EXIT, type <Y>, then <Enter>.

To Disable Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see “Enter Password”, enter the existing password and press <Enter>.
3. You will see “Confirm Password”. Type it again, and press <Enter>.
4. Select Set Password again, and at the “Enter Password” prompt, please don’t enter anything; just press <Enter>.
5. At the “Confirm Password” prompt, again, don’t type in anything; just press <Enter>.
6. Select Save to CMOS and EXIT, type <Y>, then <Enter>.

3.2.12 Save & Exit Setup

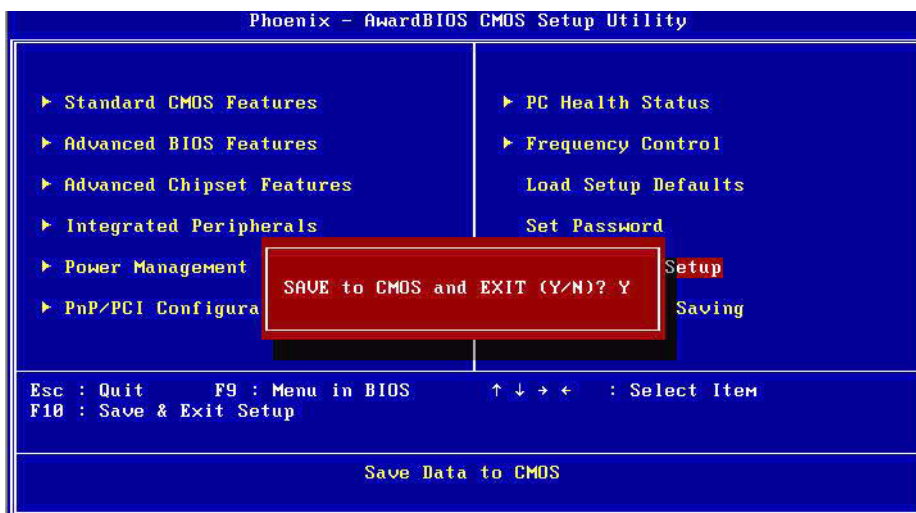


Figure 3.12 Award BIOS SAVE to CMOS and EXIT

Note! Typing "Y" will quit the BIOS Setup Utility and save user setup value to CMOS.



Typing "N" will return to BIOS Setup Utility.

3.2.13 Quit Without Saving

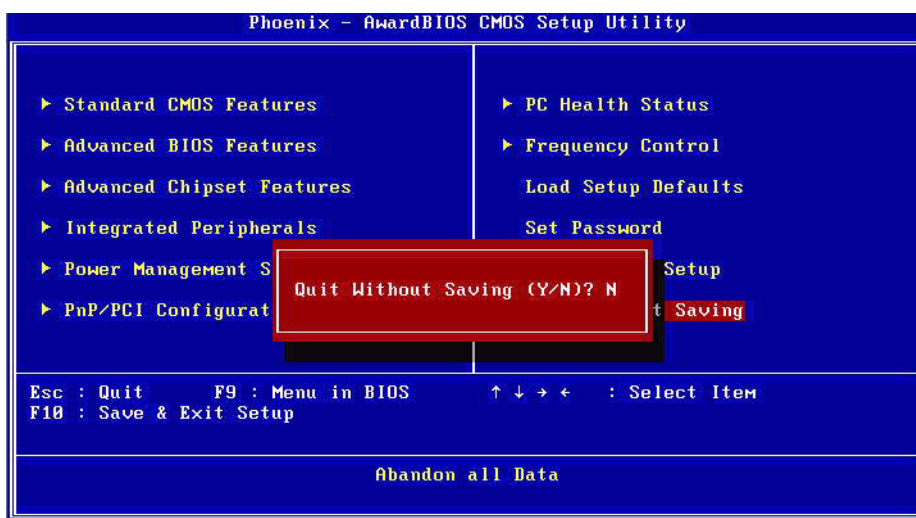


Figure 3.13 Award BIOS Quit without Saving

Note! Typing "Y" will quit the BIOS Setup Utility and save user setup value to CMOS.



Typing "N" will return to BIOS Setup Utility.

Chapter 4

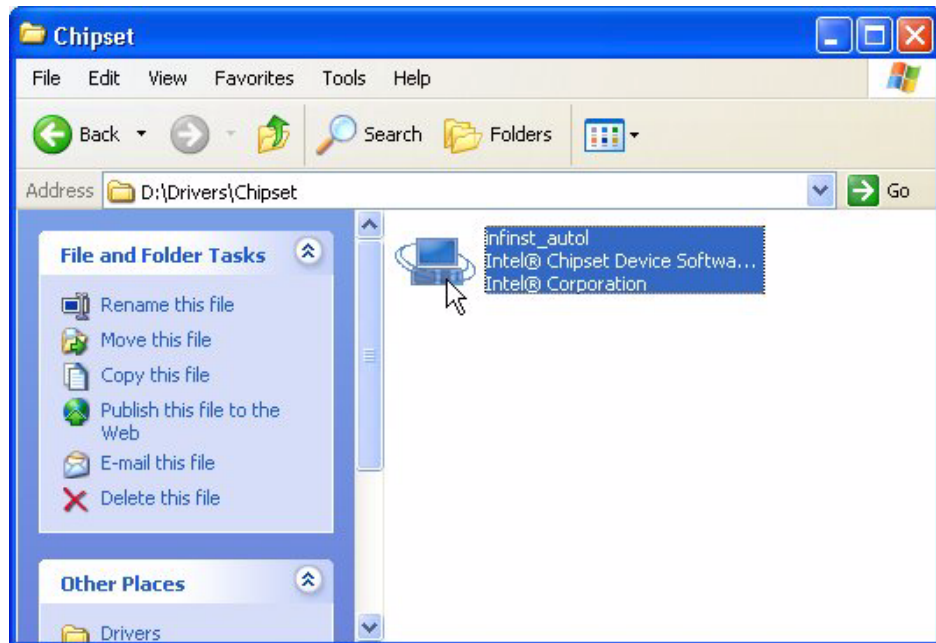
Software Installation

This chapter introduces driver installation.

4.1 Driver Installation

4.1.1 Chipset driver installation

1. Change folder address to \Drivers\Chipset. And double click to execute infinst_autol.exe.



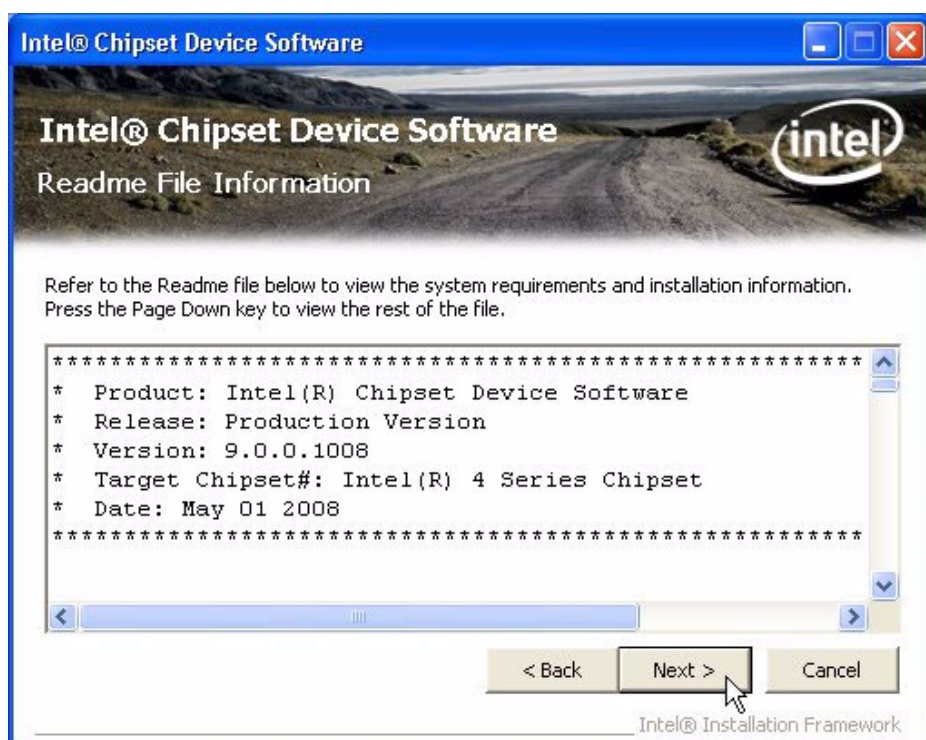
2. Click "Next;" go to the next step.



3. Click "Yes" to accept License Agreement.



4. Click "Next" to exit Readme File Information window.



5. Click “Next” button to continue.

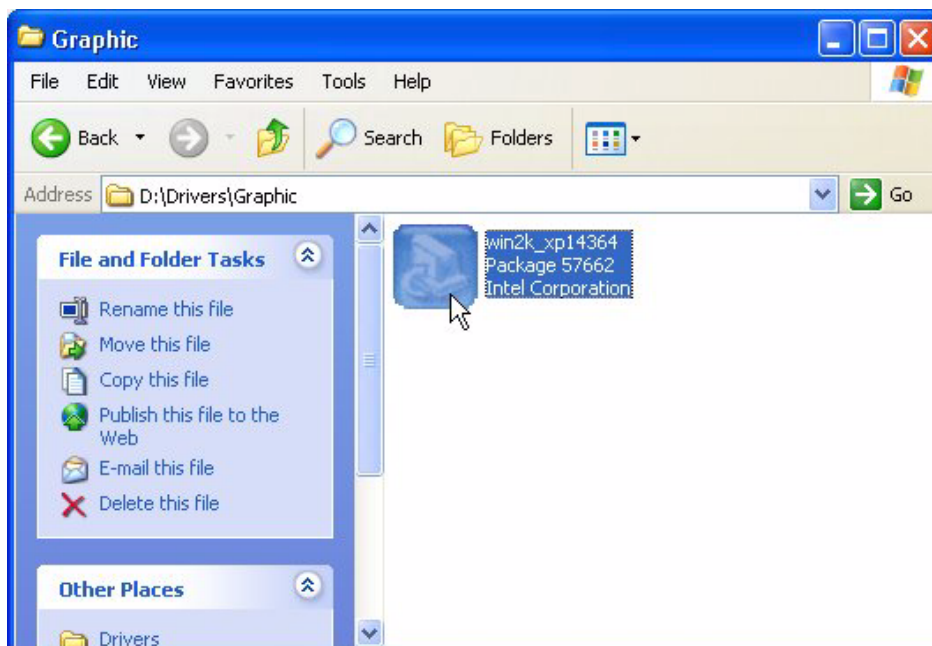


6. Select “Yes, I want to restart this computer now.” and click “Finish” button. The computer will restart automatically. Then the driver installation is completed.

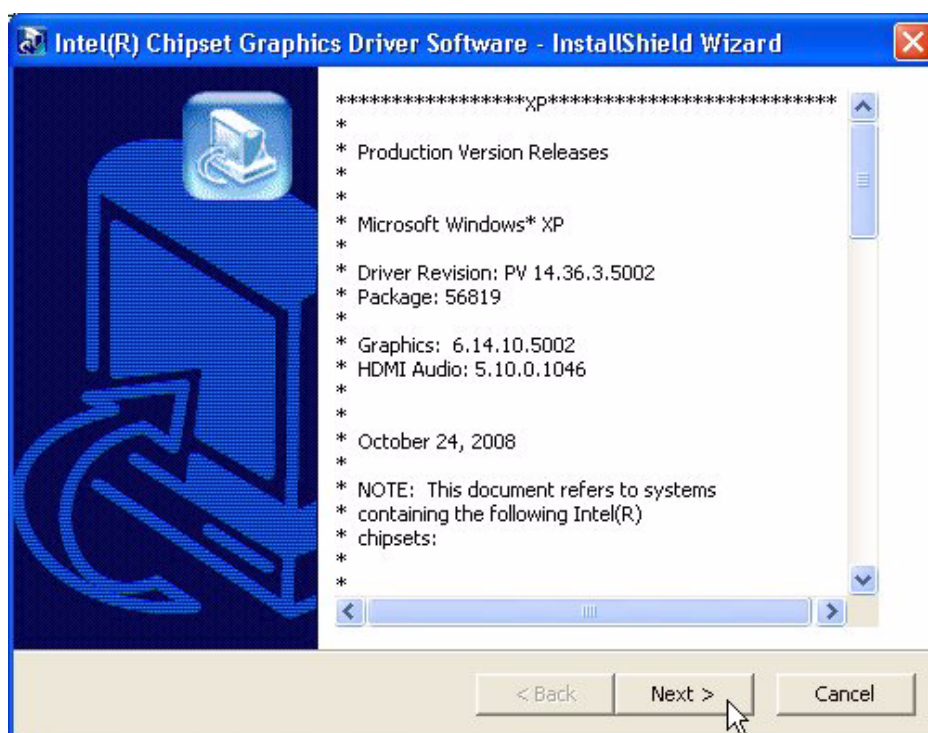


4.1.2 Graphic driver installation

1. Change folder address to \Drivers\Graphic. And double click to execute win2k_xp14364.exe.



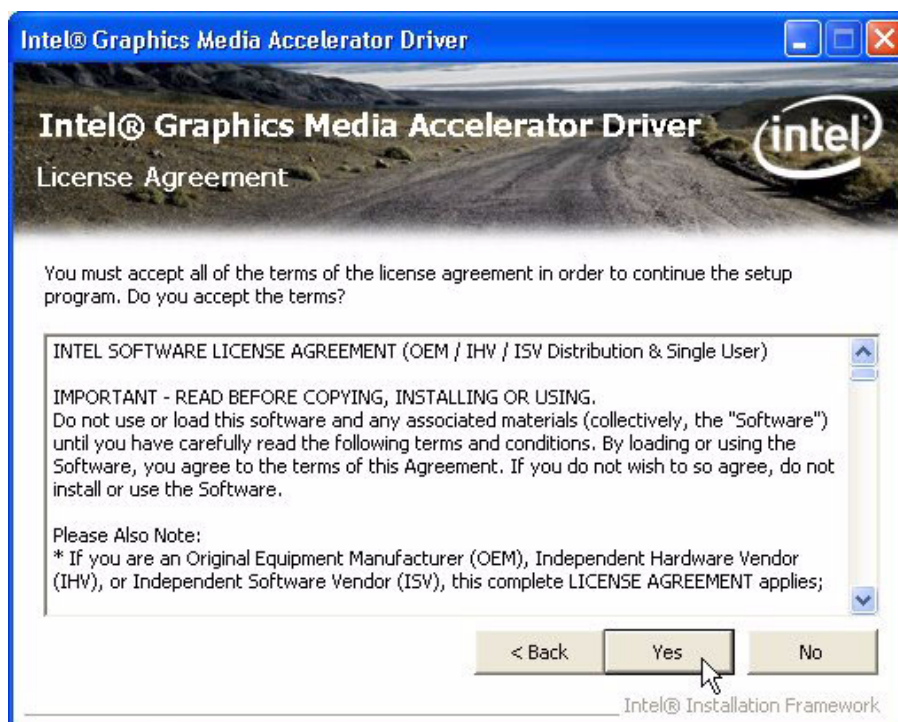
2. Click "Next" button to continue installation.



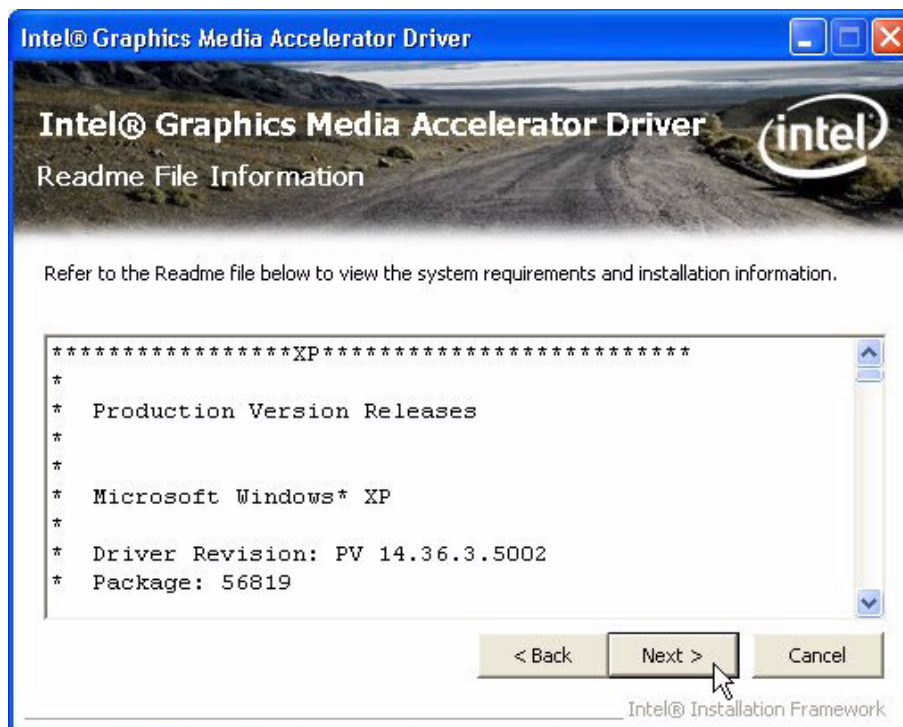
3. Click "Next" button to skip through welcome window.



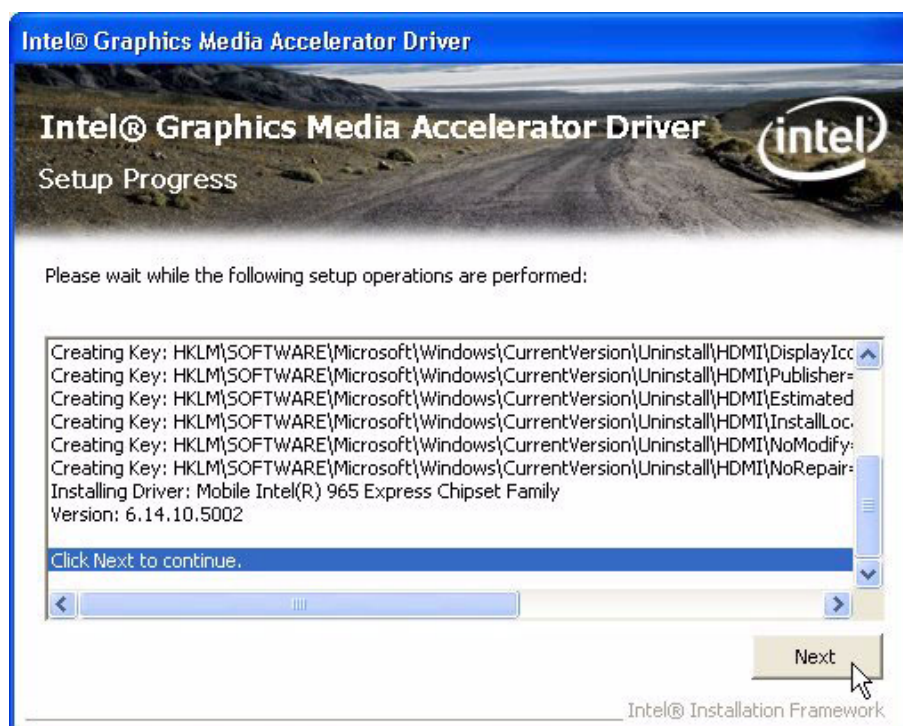
4. Click "Yes" to accept License Agreement.



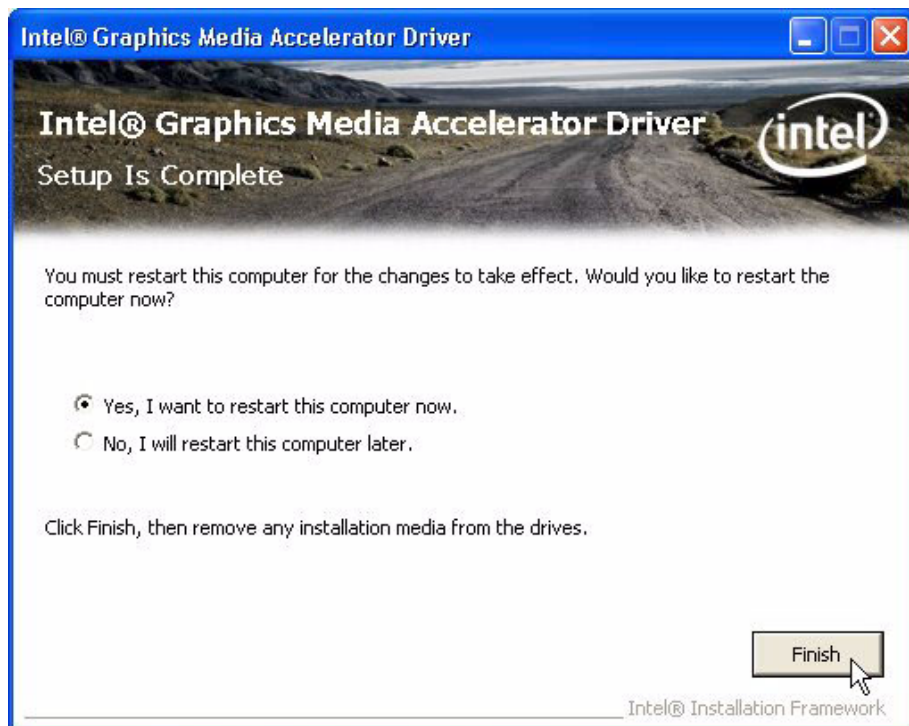
5. Click "Next" to exit Readme File Information window.



6. Click "Next" button to continue.

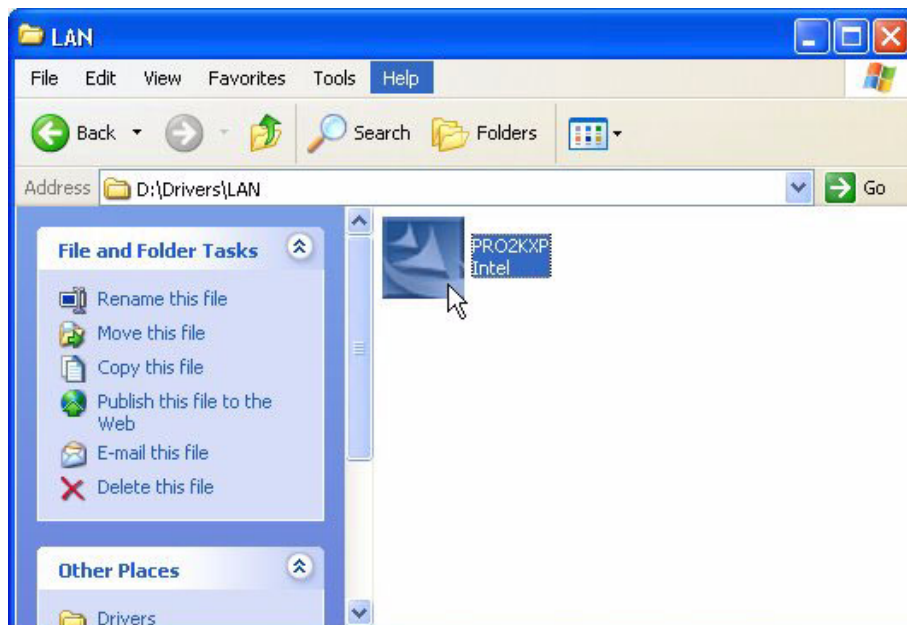


7. Select “Yes, I want to restart this computer now.” and click “Finish” button. The computer will restart automatically. Then the driver installation is completed.

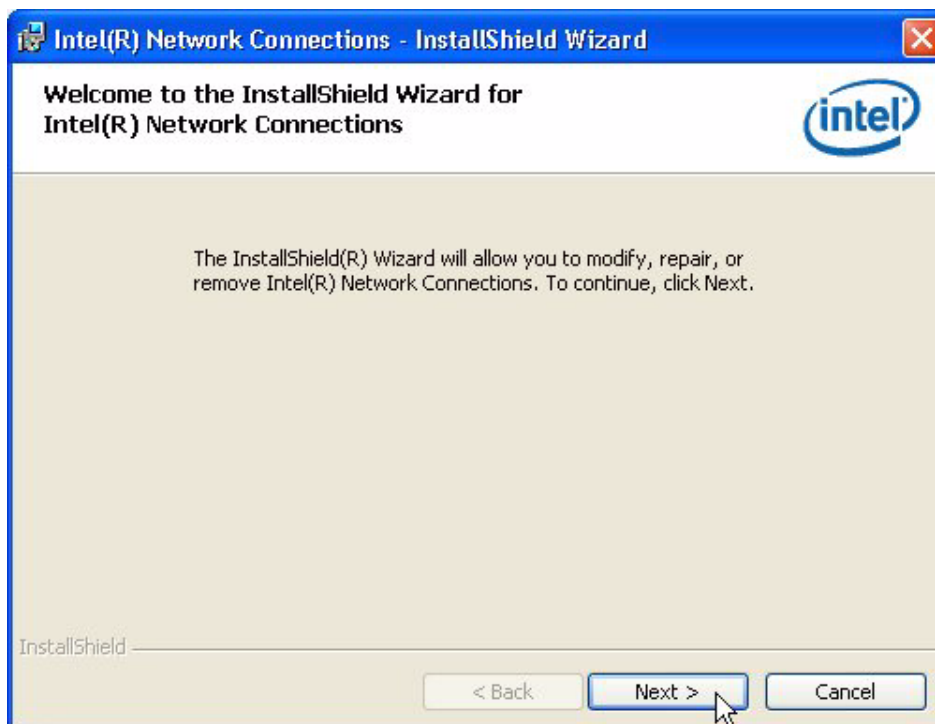


4.1.3 LAN driver installation

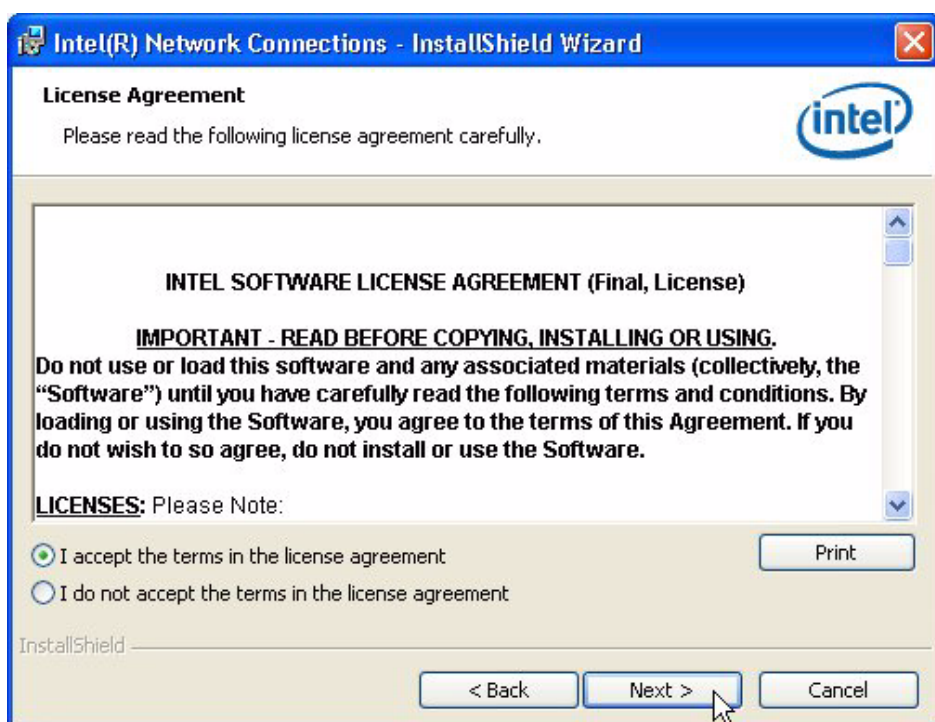
1. Change folder address to \Drivers\LAN. And double click to execute PRO2KXP.exe.



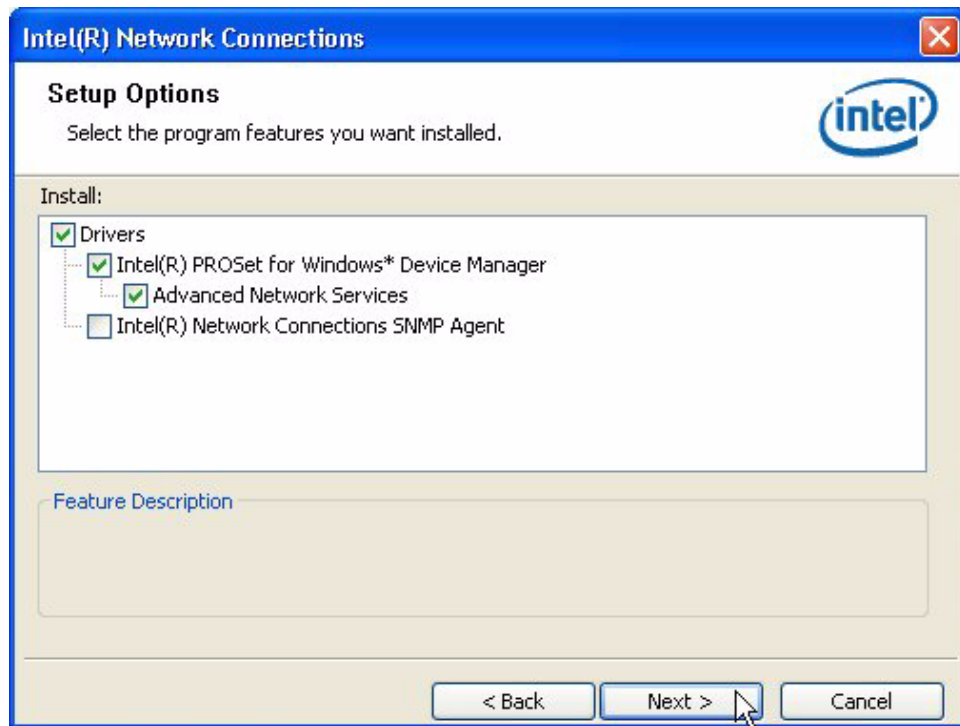
2. Click "Next" button to the next step.



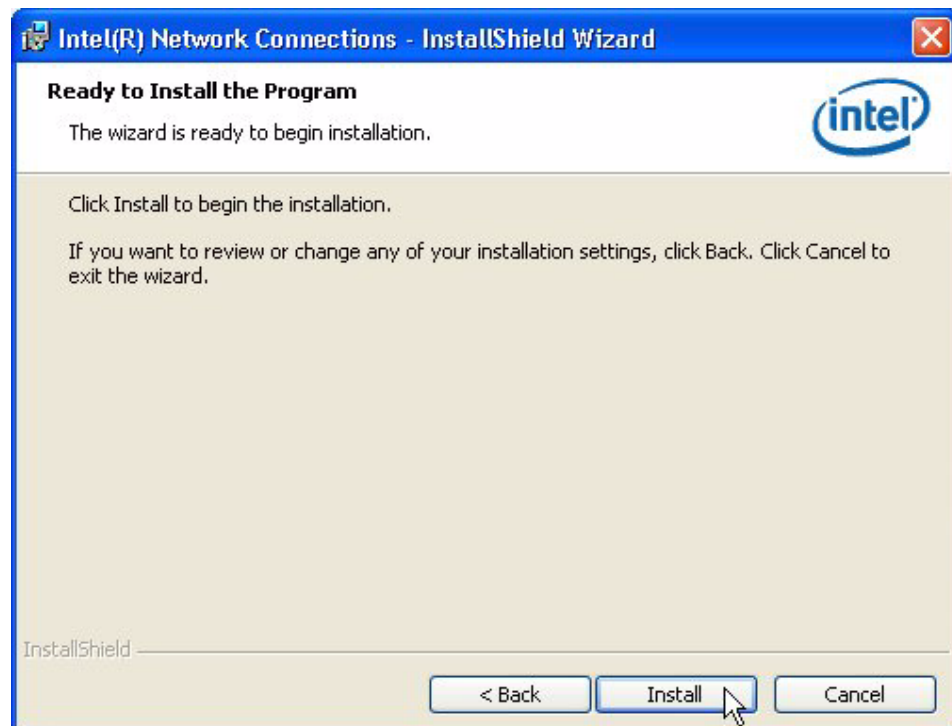
3. Click "Yes" to accept License Agreement.



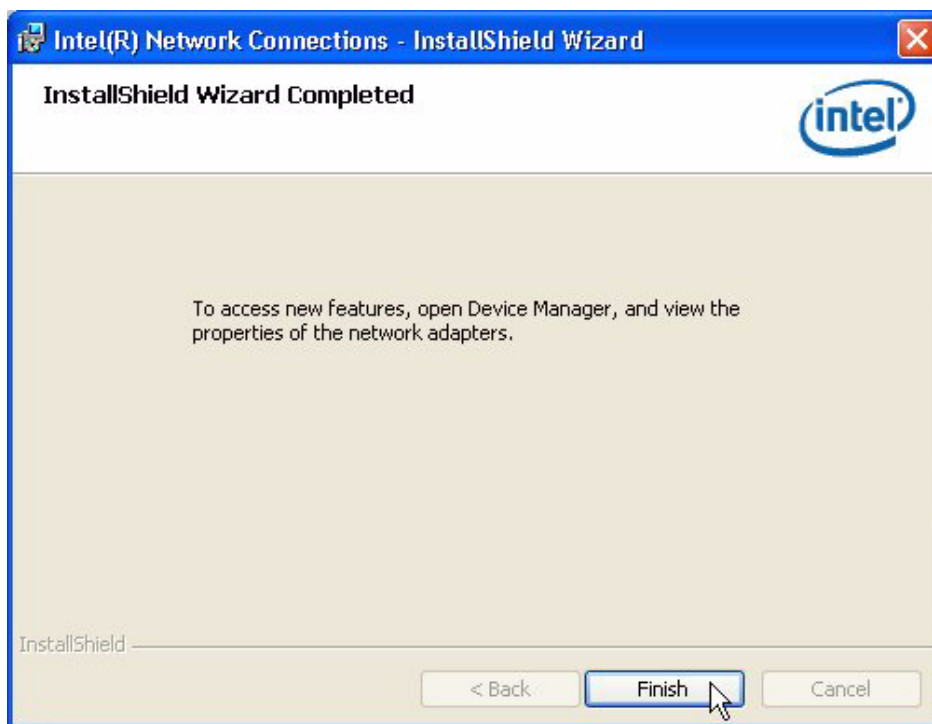
4. Select Drivers->Intel(R) PROSet for Windows* Device Manager -> Advanced Networks Services [default setting]. And click "Next" button to next step.



5. Click "Install" button to start Installation.

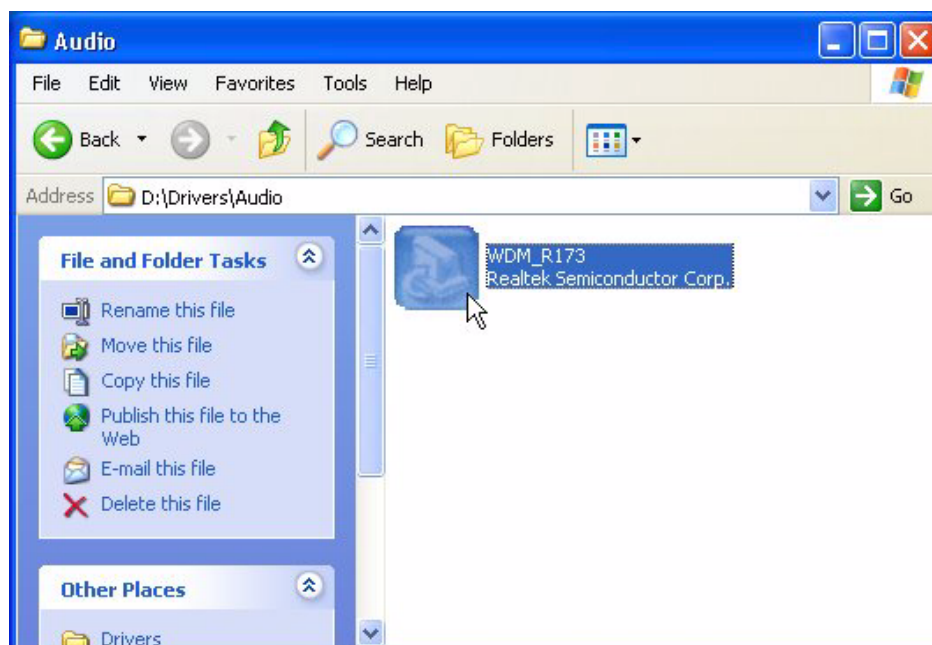


6. The network driver installation is completed. Click “Finish” button to exit InstallShield.

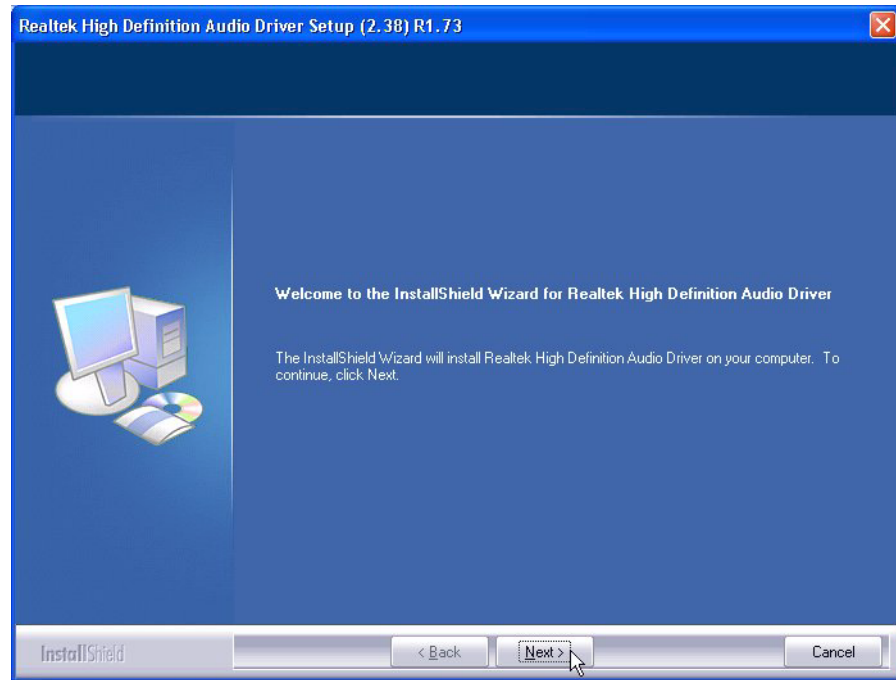


4.1.4 Audio driver installation

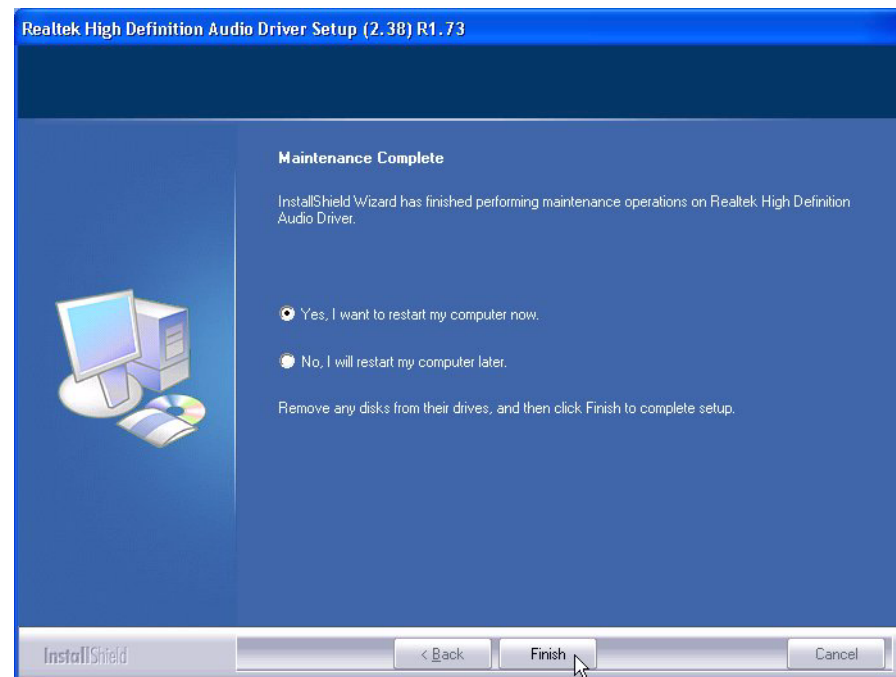
1. Change folder address to \Drivers\Audio. And double click to execute WDM_R173.exe.



2. Click “Next” button to skip welcome message.



3. Select “Yes, I want to restart this computer now,” and click “Finish” button. The computer will restart automatically. Then the driver installation is completed.



Appendix **A**

Function Settings

A.1 Function Setting

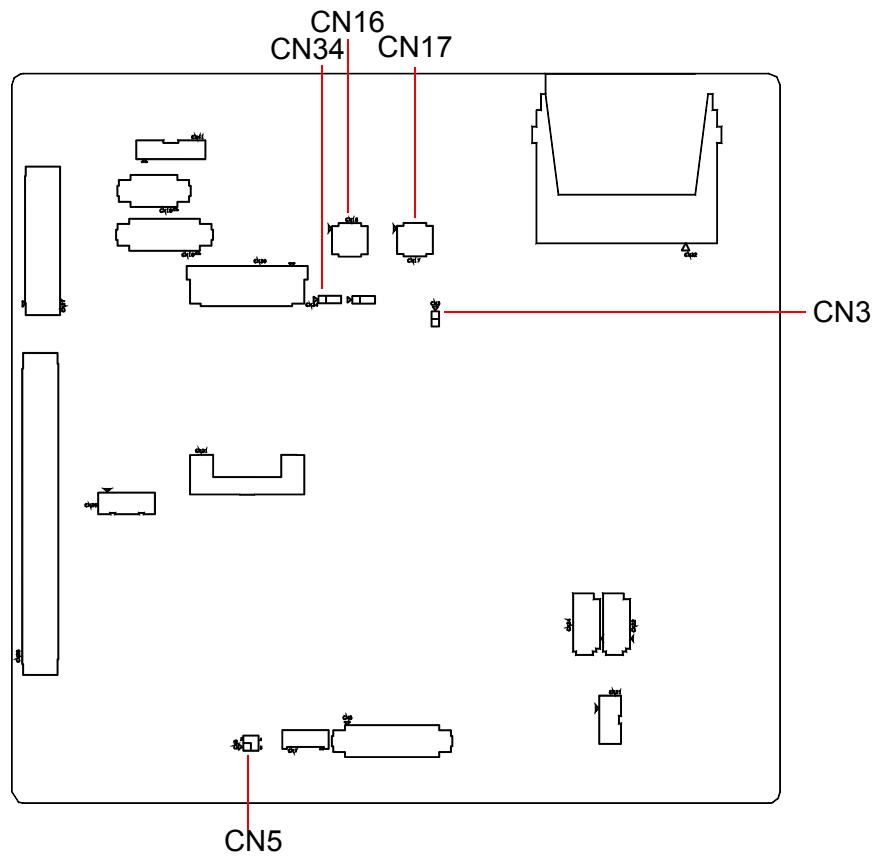


Figure A.1 Carrier board bottom connector indication

Table A.1: Setting Table

CN3		ATX / AT Mode switch	
Part Number	1653002101		
Footprint	JH2X1V-2M		
Description	PIN HEADER 2*1P 180D(M)SQUARE 2.0 mm DIP W/O Pb		
Setting	Function		
NL	ATX Mode(default)		
ON	AT Mode		
<hr/>			
CN5		Internal LVDS PANEL POWER Select	
Part Number	1653002201		
Footprint	JH2X2V-2M		
Description	PIN HEADER 2*2P 180D(M) SQUARE 2.0 mm		
Setting	Function		
(1-2)	3.3V for LVDS_PANEL POWER Select (Default)		
(3-4)	5V for LVDS_PANEL POWER Select		
<hr/>			
CN16		POWER Output Enable for DB-9 Connector	
Part Number	1653004260		
Footprint	JH4X2S-2M		
Description	PIN HEADER 4*2P 180D(M) 2.0 mm SMD		
Setting	Function		
(1-3),(2-4)			
(5-7),(6-8)	12 V Output to DB-9 Connector		
All NL	No Power Output with DB-9 Connector (Default)		
<hr/>			
CN17		DB-9 Connector Pin-9 Function Select	
Part Number	1653004260		
Footprint	JH4X2S-2M		
Description	PIN HEADER 4*2P 180D(M) 2.0 mm SMD		
Setting	Function		
(1-2),(3-4)			
(5-6),(7-8)	Set DB-9 Connector Pin-9 Function with °×Ring°± (Default)		
All NL	Set DB-9 Connector Pin-9 Function with °×Power Output°±		
<hr/>			
CN34		CLEAR CMOS	
Part Number	1653003101		
Footprint	JH3X1V-2M		
Description	PIN HEADER 3*1P 180D(M) 2.0 mm DIP SQUARE W/O Pb		
Setting	Function		
(1-2)	CLEAR CMOS		
(2-3)	NORMAL (Default)		

Appendix **B**

Display Application

B.1 Introduction

The ARK-3420 has an onboard Intel GME965 chipset for its PCIE controller. It supports LVDS & DVI displays and conventional analog CRT monitors with 384MB frame buffer shared with system memory. The VGA controller can drive CRT displays with resolutions up to 1600 x 1200 @ 85 Hz and 2048 x 1536 @ 75 Hz and support 24/48 bits LVDS display mode up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz.

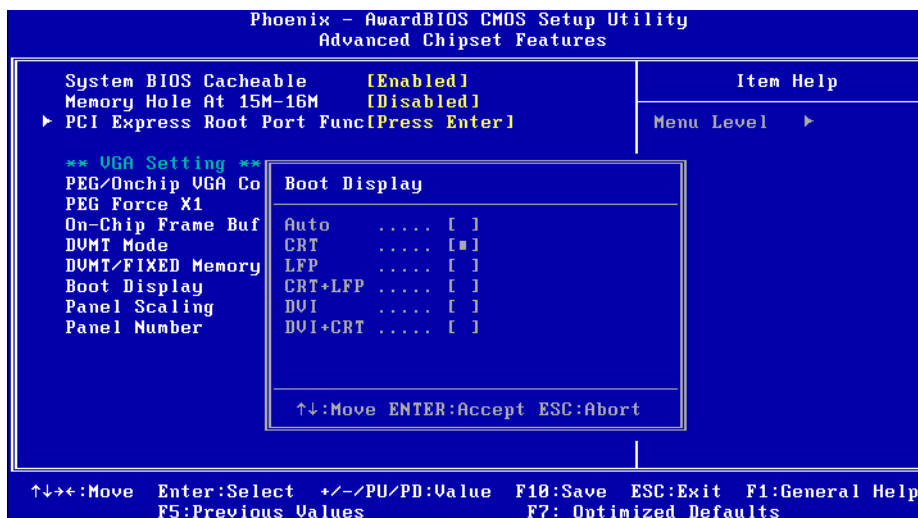


Figure B.1 BIOS VGA setting

B.2 LVDS

Low-voltage differential signaling, or LVDS, is an electrical signaling system that can run at very high speeds over inexpensive twisted-pair copper cables. It was introduced in 1994, and has since become very popular in computers, where it forms part of very high-speed networks and computer buses.

The ARK-3420 support 24/48 bits LVDS display mode up to UXGA panel resolution with frequency range from 25-MHz to 112-MHz. Refer to Chapter 3 “BIOS Operation” to find out how to change this setting. The default setting of “Boot Display” is “CRT”.

B.3 Dual Display

A multiple monitor setup increases the net display area of a system and can be an inexpensive way of improving computer usage. Resulting display area after upgrading to a multi-monitor configuration is limited by the size, resolution and number of monitors. The monitors used for multi-monitor can be different types (CRT+LPT or CRT+DVI) and sizes. The operating system manages the monitors' resolutions independently.

B.3.1 Display modes

■ Clone mode

Initially on PCs, the multiple output interface was designed to display the same image on all output interfaces (sometimes referred to as mirroring or cloning). This reflected the fact that these video cards were originally used in presentations where the user typically had his or her face to the audience with a duplicate of the projected image available to the presenter.

■ Extended mode

In "extended" mode, additional desktop area is created on additional monitors. Each monitor can use different settings (resolution, color, refresh rate). Macintosh computers have supported the "extended desktop" concept since the late 1980s, increasing the platform's utility for professional media and software developers such as graphic designers, video editors, and game developers.

The concept was further developed by PC manufacturers and led to the "extended" or "independent displays" mode and the "spanning" or "stretched" display mode. In both of these modes, display devices are positioned next to each other in order to create the illusion that the two displays are logically contiguous.

B.4 Display Resolution Setting

The ARK-3420 can drive CRT displays with resolutions up to 1600 x 1200 @ 85 Hz and 2048 x 1536 @ 75 Hz and support 24/48 bits LVDS display mode up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz.

Appendix **C**

Application Notes

C.1 RS-485 Auto Flow Control

The COM3 & COM4 port connector located on the rear face plate of ARK-3420 unit can be configured to operate in RS-232, RS-422 or RS-485 mode by adjusting the “Onboard Serial port 3 Mode” & “Onboard Serial port 4 Mode” of “Integrated Peripherals” in the BIOS.

Refer to Chapter 3 “BIOS Operation” to find out how to change this setting. The default setting of COM3 & COM4 is RS-232.

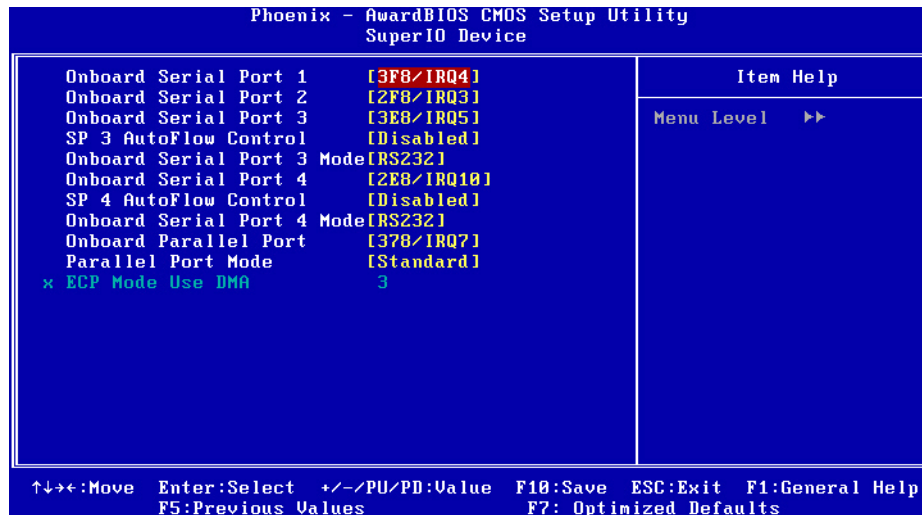


Figure C.1 BIOS COM port setting

C.1.1 Flow control, introduction

Consider the situation where someone is helping you harvest apples from a tree. Your helper climbs up the tree and throws all the apples down to you. You have to put them in buckets. In the normal situation, you can easily catch all the apples, but when one bucket is full and it has to be replaced by an empty one, this action takes more time than is available between two apples thrown by your helper.

Two different things can occur. Your helper stops until the new bucket is in position, or some apples are damaged because they fall on the (rock hard, as it happens) ground in the small period you are not able to catch them.

You would probably prefer the first method where your helper stops for a small period. To achieve this, there will be some communication, eye-contact, a yell, or something like that to stop him/her from throwing new apples. How simple, but is it always this simple? Consider the situation where one computer device sends information to another using a serial connection. Now and then, the receiver needs to do some other actions, to write the contents of its buffers to disk for example. In this period of time no new information can be received. Some communication back to the sender is needed to stop the flow of bytes on the line. A method must be present to tell the sender to pause. To do this, both software and hardware protocols have been defined.

C.1.2 Software flow control

Both software and hardware flow control need software to perform the handshaking task. This makes the term software flow control somewhat misleading. What is meant is that with hardware flow control, additional lines are present in the communication cable which signal handshaking conditions. With software flow control, which is also known under the name XON-XOFF flow control, bytes are sent to the sender using the standard communication lines.

Using hardware flow control implies, that more lines must be present between the sender and the receiver, leading to a thicker and more expensive cable. Therefore, software flow control is a good alternative if it is not needed to gain maximum performance in communications. Software flow control makes use of the datachannel between the two devices which reduces the bandwidth. The reduction of bandwidth is in most cases however not so astonishing that it is a reason to not use it.

Two bytes have been predefined in the ASCII character set to be used with software flow control. These bytes are named XOFF and XON, because they can stop and restart transmitting. The bytevalue of XOFF is 19, it can be simulated by pressing Ctrl-S on the keyboard. XON has the value 17 assigned which is equivalent to Ctrl-Q.

Using software flow control is easy. If sending of characters must be postponed, the character XOFF is sent on the line, to restart the communication again XON is used. Sending the XOFF character only stops the communication in the direction of the device which issued the XOFF.

This method has a few disadvantages. One is already discussed: using bytes on the communication channel takes up some bandwidth. One other reason is more severe. Handshaking is mostly used to prevent an overrun of the receiver buffer, the buffer in memory used to store the recently received bytes. If an overrun occurs, this affects the way newcoming characters on the communication channel are handled. In the worst case where software has been designed badly, these characters are thrown away without checking them. If such a character is XOFF or XON, the flow of communication can be severely damaged. The sender will continuously supply new information if the XOFF is lost, or never send new information if no XON was received.

This also holds for communication lines where signal quality is bad. What happens if the XOFF or XON message is not received clearly because of noise on the line? Special precaution is also necessary that the information sent does not contain the XON or XOFF characters as information bytes.

Therefore, serial communication using software flow control is only acceptable when communication speeds are not too high, and the probability that buffer overruns or data damage occur are minimal.

C.1.3 Hardware flow control

Hardware flow control is superior compared to software flow control using the XON and XOFF characters. The main problem is, that an extra investment is needed. Extra lines are necessary in the communication cable to carry the handshaking information.

Hardware flow control is sometimes referred to as RTS / CTS flow control. This term mentions the extra input and outputs used on the serial device to perform this type of handshaking. RTS / CTS in its original outlook is used for handshaking between a computer and a device connected to it such as a modem.

First, the computer sets its RTS line to signal the device that some information is present. The device checks if there is room to receive the information and if so, it sets the CTS line to start the transfer. When using a null modem connection, this is somewhat different. There are two ways to handle this type of handshaking in that situation.

One is, where the RTS of each side is connected with the CTS side of the other. In that way, the communication protocol differs somewhat from the original one. The RTS output of computer A signals computer B that A is capable of receiving information, rather than a request for sending information as in the original configuration. This type of communication can be performed with a null modem cable for full handshaking. Although using this cable is not completely compatible with the original way hardware flow control was designed, if software is properly designed for it it can achieve the highest possible speed because no overhead is present for requesting on the RTS line and answering on the CTS line.

In the second situation of null modem communication with hardware flow control, the software side looks quite similar to the original use of the handshaking lines. The CTS and RTS lines of one device are connected directly to each other. This means, that the request to send query answers itself. As soon as the RTS output is set, the CTS input will detect a high logical value indicating that sending of information is allowed. This implies, that information will always be sent as soon as sending is requested by a device if no further checking is present. To prevent this from happening, two other pins on the connector are used, the data set ready DSR and the data terminal ready DTR. These two lines indicate if the device attached is working properly and willing to accept data. When these lines are cross-connected (as in most null modem cables) flow control can be performed using these lines. A DTR output is set, if that computer accepts incoming characters.

C.1.4 How to implement

Implementing proper flow control can give some headaches. The main problem are the numerous ways it can be done and especially for null modem connections, the lack of a standard way of doing. The best way to implement rigid flow control in your software is to use preprogrammed routines from a reliable source. The problems involved in the own development of communication routines is often not worth the effort compared to the relative low prices of professional communication libraries. A good library is the COMM-DRV/Lib from Willies Computer Software Co. This library supports all versions of Windows and MS-DOS. XModem, YModem and ZModem file transfer routines are provided and all source code is included. Includes also Modem handling and string handling routines.

C.2 WOL Setting

C.2.1 Introduction

Wake on LAN (WOL, sometimes WoL) is an Ethernet computer networking standard that allows a computer to be turned on or woken up remotely by a network message.

C.2.2 System requirements - PC Compatible

Wake on LAN (WoL) support is implemented on the motherboard of a computer. Most modern motherboards with an embedded Ethernet controller support WoL without the need for an external cable. Older motherboards must have a WAKEUP-LINK header onboard and connected to the network card via a special 3-pin cable; however, systems supporting the PCI 2.2 standard coupled with a PCI 2.2 compliant network adapter typically do not require a WoL cable as the required standby power is relayed through the PCI bus.

PCI version 2.2 has PME (Power Management Events). What this means is that PCI cards can send and receive PME via the PCI socket directly, without the need for a WOL cable.

Laptops powered by the Intel 3945 chipset or newer (with explicit BIOS support) allow waking up the machine using wireless (802.11 protocol). This is called Wake on Wireless LAN (WoWLAN).

Wake on LAN must be enabled in the Power Management section of the motherboard's BIOS. It may also be necessary to configure the computer to reserve power for the network card when the system is shutdown.

In addition, in order to get WoL to work it is sometimes required to enable this feature on the card. This can be done in Microsoft Windows from the properties of the network card in the device manager, on the "Power Management" tab. Check "Allow this device to bring the computer out of standby" and then "Only allow management stations to bring the computer out of standby" to make sure it does not wake up on all network activity.

C.2.3 How it works

Wake-on-LAN is not restricted to LAN (Local area network) traffic.

The general process of waking a computer up remotely over a network connection can be explained thusly:

The target computer is shut down (Sleeping, Hibernating or Soft Off, i.e. ACPI state G1 or G2), with power reserved for the network card. The network card listens for a specific packet, called the "Magic Packet." The Magic Packet is broadcast on the broadcast address for that particular subnet (or an entire LAN, though this requires special hardware and/or configuration). When the listening computer receives this packet, the network card checks the packet for the correct information. If the Magic Packet is valid, the network card turns on the computer to full power and boots the operating system.

The magic packet is sent on the data link or OSI-2 layer and broadcast to all NICs (within the network of the broadcast address). Therefore, it does not matter whether the remote host has a fixed or dynamic IP-address (OSI-3 layer).

In order for Wake on LAN to work, parts of the network interface need to stay on. This increases the standby power used by the computer. If Wake on LAN is not needed, turning it off may reduce power consumption while the computer is off but still plugged in.

C.2.4 Magic Packet

The Magic Packet is a broadcast frame containing anywhere within its payload 6 bytes of ones (resulting in hexadecimal FF FF FF FF FF FF) followed by sixteen repetitions of the target computer's MAC address.

Since the Magic Packet is only scanned for the string above, and not actually parsed by a full protocol stack, it may be sent as a broadcast packet of any network- and transport-layer protocol. It is typically sent as a UDP datagram to port 0, 7 or 9, or, in former times, as an IPX packet.

Appendix **D**

WDT Programming

D.1 WDT Programming

1. SMBus Address: Pin 3 internal pull up 100K = 0X9C, External pull up 4.7K = 0X6E2.
2. Enable WDT function: Configuration and function select register Index-03h3.

Table D.1: Index-03h

Bit	Name	P/W	PWR	Description
1-0	PIN10_MODE	R/W	VSB3V	00:GPIO10 01: LED10 IN this mode can use REG Ox06(bit1,0) to select LED frequency.

3. Watchdog Control: Watchdog Timer Control Register - Index 36h.
Power-on default [7:0] =0000_0000b.

Table D.2: Watchdog Timer Index 36h

Bit	Name	P/W	PWR	Description
7	Reserved	RO	VSB3V	Read will return 0.
6	STS WD TMOU	R/W	VSB3V	Watchdog is timeout. When the watchdog is timeout, this bit will be set to one. If set to 1, write 1 will clear this bit. Write 0, no effect.
5	WD ENABLE	R/W	VSB3V	Enable watchdog timer.
4	WD PULSE	R/W	VSB3V	Watchdog output level or pulse. If set 0 (default), the pin of watchdog is level output, if write 1, the pin will output with a pulse.
3	WD UNIT	R/W	VSB3V	Watchdog unit select. Default 0 is select second. Write 1 to select minute.
2	WD HAC-TIVE	RW	VSB3V	Program WD2 output level. If set to 1 and watchdog asserted, the pin will be high. If set to 0 and watchdog asserted, this pin will drive low (default).
1-0	WD_PS WIDTH	RW	VSB3V	Watchdog pulse width selection. If the pin output is selected to pulse mode. The pulse width can be choice. 00b- 1m second. 01b- 20m second. 10b -100m second. 11b- 4 second.

4. Watchdog reset timing control: Watchdog Timer Range Register - Index 37h.
Power-on default [7:0] =0000_0000b

Table D.3: Watchdog Timer Range - Index 37h

Bit	Name	P/W	PWR	Description
7-0	WD_TIME	R/W	VSB3V	Watchdog timing range from 0 - 255. The unit is either second or minute programmed by the watchdog timer control register bits.

Appendix **E**

Programming GPIO

E.1 Programming GPIO

Advantech provides SUSI (Secure & Unified Smart Interface) API for customers. It is a set of user-friendly, intelligent and integrated application programming interfaces, which shortens development time, enhances security and offers add-on value for Advantech platform users. SUSI makes applications easier and simpler to build and operate. For the detailed GPIO register, please refer to below contents.

E.2 GPIO Register

1. Configuration and function select Register - Index 03h.

Table E.1: Index-03h

Bit	Name	P/W	PWR	Description
4-3	PIN12_MODE	RW	VSB3V	00: GPIO12 01: LED12 IN tills mode can use REG OX06(bit5,4) to select LED frequency. 10: IRQ 11:WDTOUT11#:
2	PIN11_MODE	RW	VSB3V	0: GPI011 1: LED11 IN this mode can use REG OX06(brt3,2) to select LED frequency.

2. Configuration and function select Register - Index 04h.

Table E.2: Index-04h

Bit	Name	P/W	PWR	Description
1	PIN5_MODE	RW	VSB3V	0: GPI0171: LED17 IN this mode can use REG OX07(bit7, 6) to select LED frequency.
0	PIN4_MODE	RW	VSB3V	0: GPIO161: LED16 IN this mode can use REG OX07(bit5, 4) to select LED frequency.

3. Configuration and function select Register - Index 05h.

Table E.3: Index-05h

Bit	Name	P/W	PWR	Description
2	PIN23_MODE	RW	VS3V	0: GPIO241: LED24 IN this mode can use REG 0x09 (bit 1, 0) to select LED frequency.
1	PIN21_MODE	RW	VS3V	0: GPIO251: LED25 IN this mode can use REG 0x09 (bit 3, 2) to select LED frequency.
0	PIN21_MODE	RW	VS3V	0: GPIO261: LED26 IN this mode can use REG 0x09 (bit5, 4) to select LED frequency.

4. GPIOIx Output Control Register - Index 10h.

Table E.4: Index-10h

Bit	Name	P/W	PWR	Description
7	GP17JX CTRL	RW	VS3V	GPIO 17 output control. Set to 1 for output function. Set to 0 for input function (default).
6	GP16_O CTRL	RW	VS3V	GPIO 16 output control. Set to 1 for output function. Set to 0 for input function (default).
2	GP12JD CTRL	RW	VS3V	GPIO 12 output control. If this pin serves as IRQ/SMI#. this bit has no effect. Set to 1 for output function. Set to 0 for input function (default).
1	GP11_O CTRL	RW	VS3V	GPIO 11 output control. Set to 1 for output function. Set to 0 for input function (default).mode can use REG 0x09 (bit5, 4) to select LED frequency.

5. GPIO2x Output Control Register - Index 20h.

Table E.5: Index-20h

Bit	Name	P/W	PWR	Description
7	GP27_O CTRL	R/W	VSB3V	GPIO 27 output control. Set to 1 for output function. Set to 0 for input function (default).
6	GP26_O CTRL	R/W	VSB3V	GPIO 26 output control. Set to 1 for output function. Set to 0 for input function (default).
5	GP25_O CTRL	R/W	VSB3V	GPIO 25 output control. Set to 1 for output function. Set to 0 for input function (default).
4	GP24_O CTRL	R/W	VSB3V	GPIO 24 output control. Set to 1 for output function. Set to 0 for input function (default).
3	GP23_O CTRL	R/W	VSB3V	GPIO 23 output control. Set to 1 for output function. Set to 0 for input function (default).
2	GP22_O CTRL	R/W	VSB3V	GPIO 22 output control. Set to 1 for output function. Set to 0 for input function (default).
1	GP21_O CTRL	R/W	VSB3V	GPIO 21 output control. Set to 1 for output function. Set to 0 for input function (default).
0	GP20_O CTRL	R/W	VSB3V	GPIO 20 output control. Set to 1 for output function. Set to 0 for input function (default).

6. GPIOIx Output Data Register - Index 11h.

Table E.6: Index-11h

Bit	Name	P/W	PWR	Description
7	GP17JD DATA	R/W	VSB3V	GPIO 17 output data.
6	GP16_O DATA	R/W	VSB3V	GPIO 16 output data.
5	GP15JD DATA	R/W	VSB3V	GPIO 15 output data.
4	GP14JD DATA	R/W	VSB3V	GPIO 14 output data.
3	GP13JD DATA	R/W	VSB3V	GPIO 13 output data.
2	GP12_O DATA	R/W	VSB3V	GPIO 12 output data. If this pin serves as IRQ/SMI*, this bit has no effect.
1	GP11_O DATA	R/W	VSB3V	GPIO 11 output data.
0	GP10JD DATA	R/W	VSB3V	GPIO 10 output data.

7. GPIOx Input Status Register - Index 12h.

Table E.7: Index-12h

Bit	Name	P/W	PWR	Description
7	GP17_P STS	RO	VS3V	Read the GPIO17 data on the pin.
6	GP16_P STS	RO	VS3V	Read the GPIO16 data on the pin.
5	GP15_P STS	RO	VS3V	Read the GPIO15 data on the pin.
4	GP14_P STS	RO	VS3V	Read the GPIO14 data on the pin.
3	GP13_P STS	RO	VS3V	Read the GPIO13 data on the pin.
2	GP12_P STS	RO	VS3V	Read the GPIO12 data on the pin.
1	GP11_P STS	RO	VS3V	Read the GPIO11 data on the pin.
0	GP10_P STS	RO	VS3V	Read the GPIO10 data on the pin.

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