IIoT Solutions - WISE LPWAN Payload Format

Version: 1.05

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Advantech

History Record:

文件版本	更新日期	更新者	內容
0.90	2019/01/02	Carrie.Tung	Draft version.
1.00	2019/01/08	Carrie.Tung	1. Chapter 3 describes LoRaWAN frame payload. 2. LPWAN payload format is detailed in chapter 4. 3. The endianness of LPWAN payload is little-endian. 4. Add DO data format. 5. Add position data in Device data (I/O type: 0x6). 6. Correct the frame control values in chapter 5 example.
1.01	2019/01/08	Carrie.Tung	1. Insert 1-bit COM port index in the channel byte of coil and register data.
1.02	2019/03/06	Jay.Huang	1. Change device data format and add battery voltage in chapter 4.5
1.03	2019/03/18	Carrie.Tung	1. Modify the sensor data for accelerometer.
1.04	2019/04/09	Jay.Huang	1. Chapter 2 describes Sub-1G frame payload
1.05			2. Add AI Modbus type code information in AI data. 3. Add message type for downlink and ACK in Chapter 2. 4. Add example for WPayload.

Table of Contents

Documentation Conventions

List of abbreviations:

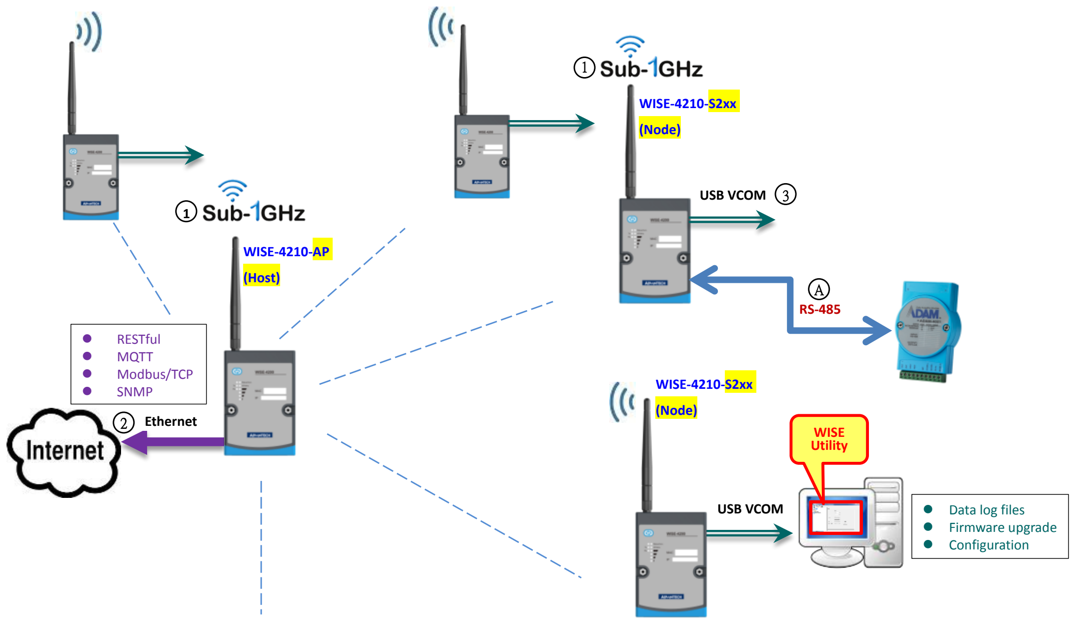
LPWAN	Low-Power Wide-Area Network

1 WISE LPWAN Products

1.1 Sub-1G LPWAN IoT Wireless Sensor Network

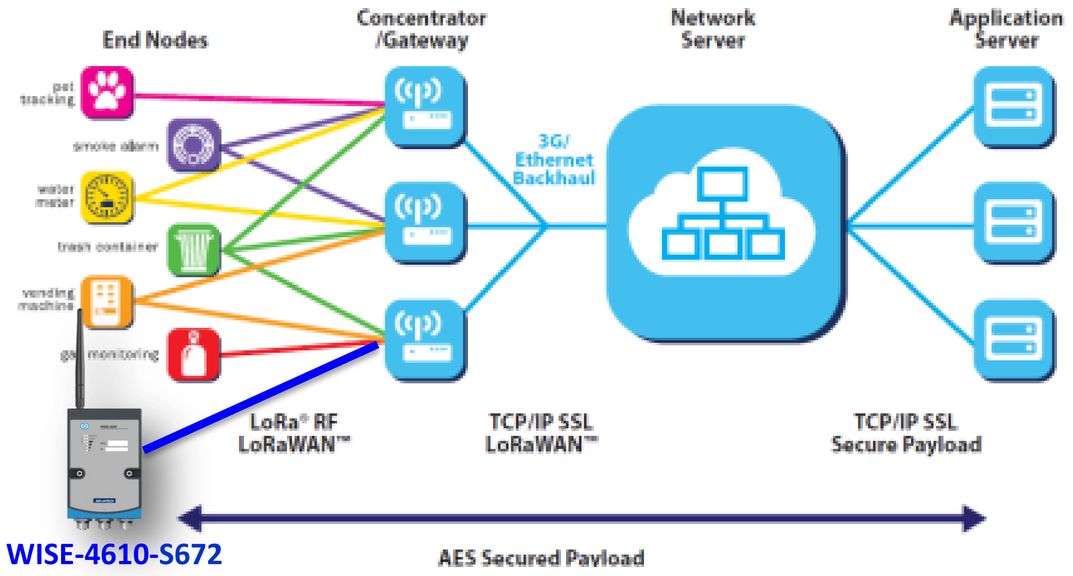
WISE-2210 series nodes

WISE-4210 series AP and nodes

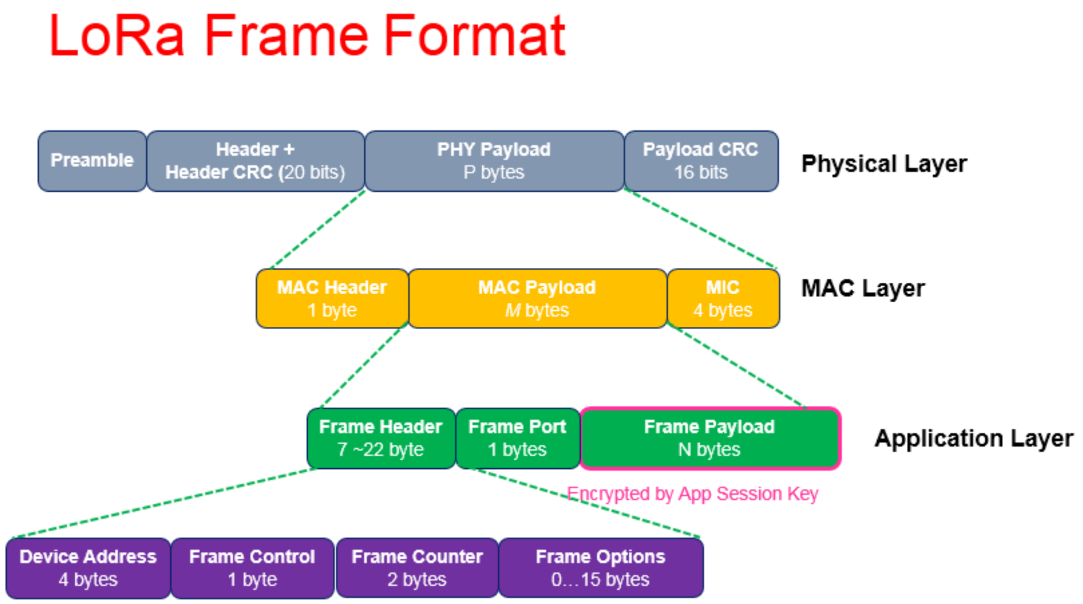


1.2 LoRaWAN

WISE-4610 series LoRaWAN nodes.



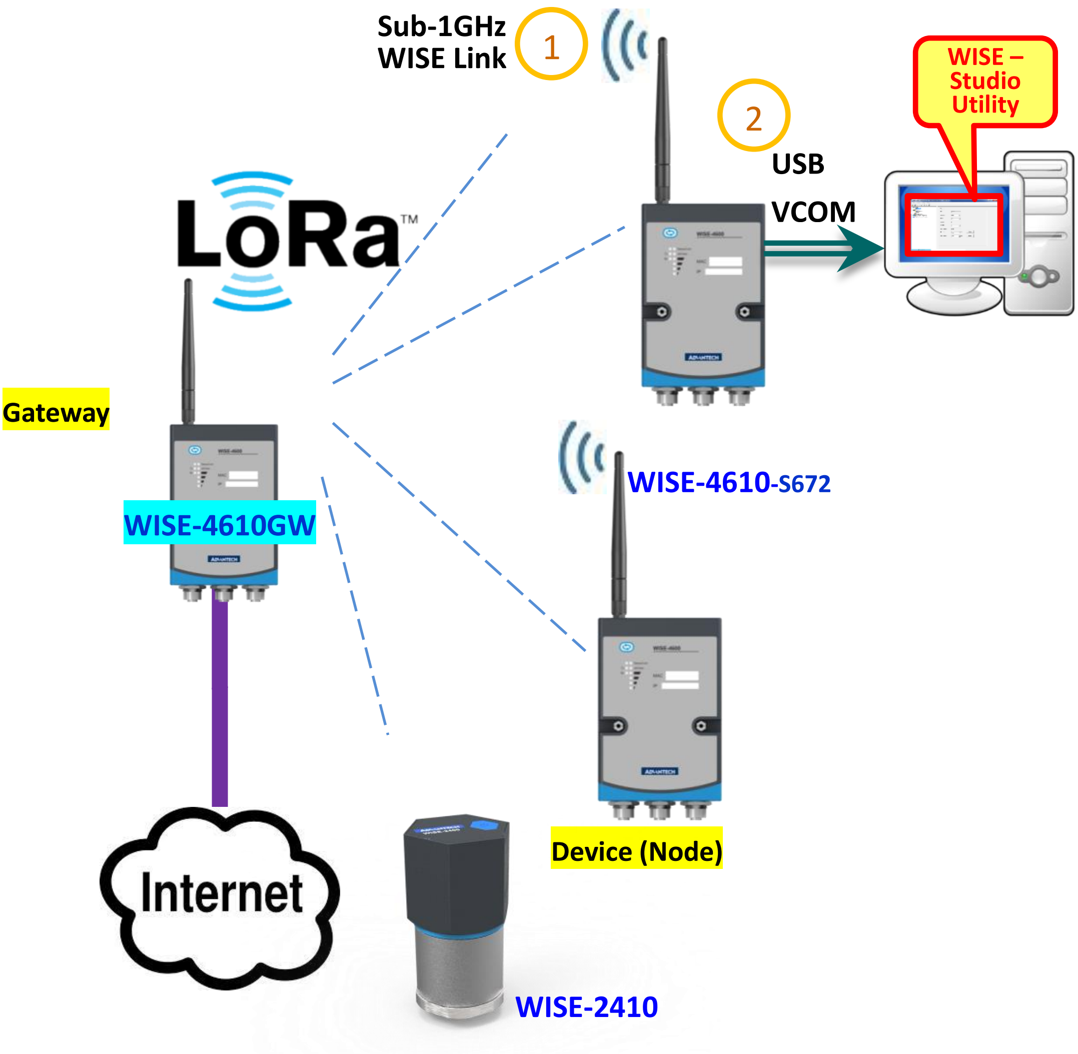
This specification describes the format of LoRaWAN Frame Payload.



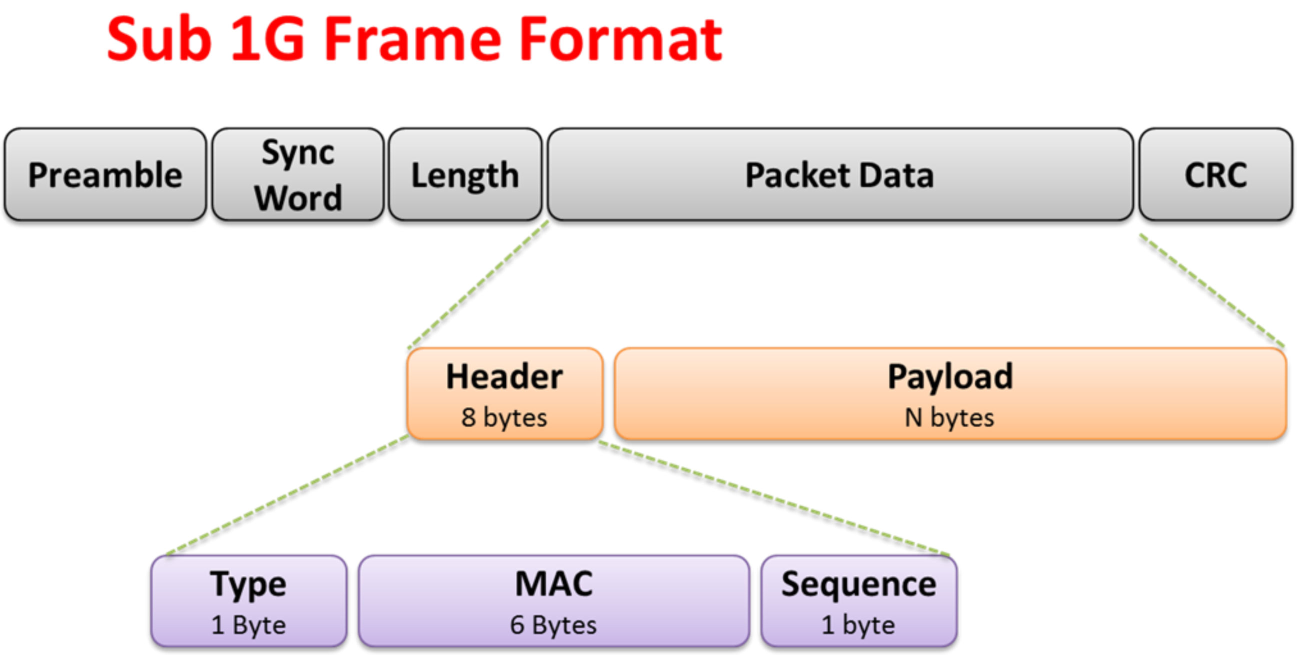
1.3 LoRa Private LPWAN Network

WISE-2410 vibration sensor nodes

WISE-4610 series



2 Sub-1G LPWAN – Frame Payload



The message structure of Sub-1g LPWAN Frame Payload is detailed in this chapter. Each frame payload starting with a several-octets WISE data header (**WHDR**), followed by a WISE LPWAN Payload (**WPayload**). A WISE Payload (WPayload) contains I/O statuses, Device information, and so on.

2.1 WHDR Header

Frame Control: 1 octet

Frame Control					
Value	Message Type	Frame Control			
bit 4 ~ 7		bit 3	bit 2	bit 1	bit 0
0x04	Message Ack	Reserved			ACK
0x06	Site Survey event				
0x07	OTA data	Reserved			
0x09	Get IO data	Write data	Changed data	All data	ACK
0x0A	IO Data	Reserved			ACK

Source MAC address: 6 octets

The Source MAC address of a node is a unique identifier and sent to the gateway to distinguish

Frame Sequence Number: 1 octet, 0 ~ 255

The sequence number of data frame sent uplink to the gateway. Each time an uplink packet transmitted done, the sequence number is increased for the next new uplink.

2.2 WPayload

Site Survey event

No payload data or feedback RSSI value (one octet).

OTA data

Group configuration or firmware image (fellow WISE Series - Open RESTful API Specification doc)

Example:

	Frame Control	Source MAC	Sequence	Payload
Request	**0x60**	66 55 44 33 22 11	00	-
	Frame Control	**Source MAC**	**Sequence**	**Payload**
Response	**0x61**	66 55 44 33 22 11	00	RSSI

IO Data

The **WPayload** structure is detailed chapter 4.

Example:

a. Push data without ACK

	Frame Control	Source MAC	Sequence	Payload
Request	**0xA0**	66 55 44 33 22 11	00	LPWAN Payload

b. Push data with ACK

	Frame Control	Source MAC	Sequence	Payload
Request	**0xA1**	66 55 44 33 22 11	00	LPWAN Payload
	Frame Control	**Source MAC**	**Sequence**	**Payload**
Response	**0x41**	66 55 44 33 22 11	00	-

Downlink data

The **WPayload** structure is detailed chapter 4.

The first 6 octets are destination MAC.

Example:

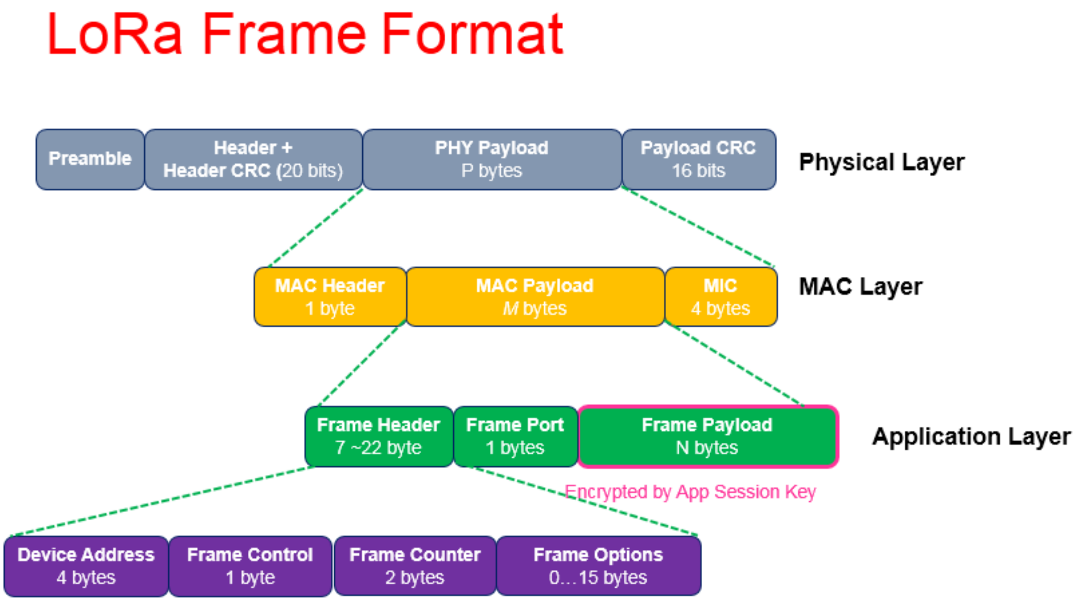
a. Get I/O data

	Frame Control	Source MAC	Sequence	Destination MAC	Payload
Request	**0x92 (All data)** **0x94 (Changed data)**	66 55 44 33 22 11	20	C9 66 00 64 00 46	-
	Frame Control	**Source MAC**	**Sequence**	**Destination MAC**	**Payload**
Response	**0x93 (All data)** **0x95 (Changed data)**	C9 66 00 64 00 46	00	66 55 44 33 22 11	LPWAN Payload

b. Write I/O data

Request	**Frame Control**	**Source MAC**	**Sequence**	**Destination MAC**	**Payload**
	0x98	66 55 44 33 22 11	20	C9 66 00 64 00 46	LPWAN Payload
Response	**Frame Control**	**Source MAC**	**Sequence**	**Destination MAC**	**Payload**
	0x99	C9 66 00 64 00 46	00	66 55 44 33 22 11	-

3 LoRaWAN - Frame Payload



The message structure of LoRaWAN Frame Payload is detailed in this chapter. Each frame payload starting with a several-octets WISE data header (**WHDR**), followed by a WISE LPWAN Payload (**WPayload**), and ending with a single-octet cyclic redundancy check (**CRC**) code. A WISE Payload (WPayload) contains I/O statuses, Device information, and so on.

Frame Payload (FRM Payload)					
Octet: 1	1	0/1	0/2/8	Variable	1
Frame Control	Frame Sequence Number	Total Length	Source Address	WISE LPWAN Payload	CRC
WHDR				WPayload	WCRC

3.1 WHDR Header

Frame Control: 1 octet

Frame Control					
bit 7	6	5	4	3, 2	1, 0
First Segment				Address Mode	Frame Version
0: not first one 1: first seg.	0 Reserved	0 Reserved	0 Reserved	00: No source address 01: the least LSB 2 octets of DevEUI 10 : 8 octets DevEUI	00 : initial version

- **First Segment** bit
  Set the First Segment bit to inform the server that this is the beginning of a packet with Total Length information of WISE payload data.
- **Address Mode** 2-bits
  When the Address Mode bit is unset 00, it indicates no Source Address is encapsulated. If set 01 and 10, the Source Address is the least significant two bytes and eight bytes of DevEUI, respectively.
- **Frame Version** bit
  Two bits for frame structure version.

Frame Sequence Number: 1 octet, 0 ~ 255

The sequence number of data frame sent uplink to the gateway. Each time an uplink packet transmitted done, the sequence number is increased for the next new uplink.

Total Length: 1 octet (optional)

When the First Segment bit of Frame Control is set, the Total Length octet will be added to signal the server the total bytes of WISE payload data.

Source Address: 0/2/8 octets (optional)

None, 2 LSB or 8 bytes of DevEUI according to the Address Mode bit of Frame Control.

If DevEUI is 74FE48FFFF19D121, the sequential order of 2-bytes address starts with D1 21. For complete DevEUI address, the sequence will be 74 FE 48 FF FF 19 D1 21.

3.2 WPayload

The **WPayload** structure is detailed chapter 4.

3.3 WCRC

CRC: 1 octet

An 8-bit CRC-8-CCITT value calculated from WISE Payload data. It's a standard CRC-8, with polynomial x^8+x^2+x+1 and initial value 0xFF.

4 WISE LPWAN Payload Format

The message structure of WISE LPWAN Payload is detailed in this chapter. Each frame payload may contain several channels of I/O statuses and device information. Each I/O type has various data format.

For example, if there are DI 0, DI 2, AI 0, Coil 3, Coil 4, Register 1 and timestamp data to upload, the payload will contain the following segments with various length values.

WISE LPWAN Payload						
Octet: N_{DI}	N_{DI}	N_{AI}	N_{coil}	N_{coil}	N_{reg}	N_{Dev}
DI_0 Data	DI_2 Data	AI_0 Data	Coil_3 Data	Coil_4 Data	Register_1 Data	Timestamp

The endianness in WISE LPWAN Payload is Little-endian, the least significant bytes first.

The I/O Type in each segment is used to identify the I/O or device information message type.

(4 Bit)	Message Type
0x0	DI
0x3	AI
0x5	Sensor
0x6	Device
0x7	Coil
0x8	Register

The details of I/O and device message structures are described below.

4.1 DI data (I/O Type: 0x0)

4 Bit	4 Bit	3 bit	5 bit	1 Byte	4 Byte
IO Type	DI Mode	CH Index	Mask	DI Status	DI Value

DI Payload

- IO Type (bit 7 – 4): 0x0
- DI Mode (bit 3 – 0):

0	DI
1	Counter
2	LowToHighLatch
3	HighToLowLatch
4	Frequency

- CH Index (bit 7 – 5): I/O channel 0 ~ 7
- MASK (bit 4 – 0)

Bit 0	DI Status
Bit 1	DI Value (LSB first)

- DI (channel) Status: 1 octet

DI channel status table	
Bit order	Data
0	Signal Logic Status 1, 0: Input signal is Logic High or Low.
1	Start Counter Read 1: counter is counting 0: not counting Write 1: start counting 0: stop counting
2	Get/Clear Counter Overflow Status Read 1: overflow occurred. 0: no overflow Write 0: clear the overflow status
3	Clear Counter 1 : Clear the counter value
4	Get/Clear L2H Latch Status Read 1: L2H latch occurred. 0: no L2H latch Write 0: clear the L2H latch status
5	Get/Clear H2L Latch Status

	Read 1: H2L latch occurred. 0: no H2L latch Write 0: clear the H2L latch status
6	DI change of status
7	Reserved

- DI Value: 4 octets

It will be the frequency value when DI Mode is Frequency mode. Otherwise, it is DI counter value.

4.2 DO data (I/O Type: 0x1)

4 Bit	4 Bit	3 Bit	5 Bit	1 Byte	4 Bytes	4 Bytes
IO Type	DO Mode	CH Index	Mask	DO Status	Absolute Pulse Value	Incremental Pulse Value

DO Payload

- IO Type (bit 7 – 4): 0x1
- DO Mode (bit 3 – 0):

0	DO
1	Pulse output
2	Low to High delay
3	High to Low delay
4	AI alarm drive

- CH Index (bit 7 – 5): I/O channel 0 ~ 7
- MASK (bit 4 – 0)

Bit 0	DO Status
Bit 1	Absolute Pulse Output Value (LSB first)
Bit 2	Incremental Pulse Output Value (LSB first)

- DO (channel) Status: 1 octet

DO channel status table	
Bit order	Data
0	Signal Logic Status 1, 0: Output signal is Logic High or Low
1	Pulse Output Continue State 1 / 0: Pulse outputting is continuous or not
2	Stop Pulse Output

	1: Stop the pulse outputting.
3	DO change of status
4~7	Reserved

■ Absolute Pulse Output Value: 4 octets

When DO mode is set in Pulse Output mode, this is the absolute pulse value.

■ Incremental Pulse Output Value: 4 octets

When DO mode is set in Pulse Output mode, this is the incremental pulse value.

4.3 AI data (not 16-bit) (I/O Type: 0x2)

4.4 AI data (I/O Type: 0x3)

4 Bit	4 Bit	3 bit	5 bit	1 Byte	2 Byte	2 Byte	2 Byte	2 Byte
IO Type	AI Range	CH Index	Mask	AI Status	AI value	AI event	AI MAX value	AI Min Value

AI Payload

■ IO Type (bit 7 – 4): 0x3

■ AI Range (bit 3 – 0) :

	Modbus Type Code	
0	0x0103	-150mv~150mv
1	0x0104	-500mv~500mv
2	0x0140	-1v~1v
3	0x0142	-5v~5v
4	0x0143	-10v~10v
5	0x0105	0~150mv
6	0x0106	0~500mv
7	0x0145	0~1v
8	0x0147	0~5v
9	0x0148	0~10v
10	0x0180	4mA~20mA
11	0x0181	-20mA~20mA
12	0x0182	0~20mA

- CH Index (bit 7 – 5): I/O channel 0 ~ 7
- MASK (bit 4 – 0)

Bit 0	AI Status
Bit 1	AI Raw Value + resolution
Bit 2	AI Event
Bit 3	AI Max Value
Bit 4	AI Min Value

- AI (channel) status: 1 octet

AI channel status table	
Bit order	Data
0	Low Alarm Status Read 1: low alarm occurred. 0: not occurred Write 0: clear the low alarm status
1	High alarm status Read 1: high alarm occurred. 0: not occurred Write 0: clear the high alarm status
2	Clear Maximum AI Value 1: Clear the maximum AI value
3	Clear Minimum AI Value 1: Clear the minimum AI value
4-7	<Reserved for internal use>

- AI Value: 2 octets

AI value is the measurement raw data with range 0 to 0xFFFF.

- AI Event: 2 octets

AI event status table is shown below.

Bit Order	Description
0	Fail to provide AI value (UART timeout, ADC error)
1	Over Range
2	Under Range
3	Open Circuit (Burnout)
4	Reserved
5	Unavailable Channel Configuration (Channel Disabled, DI Mode

	Used)
6	Reserved
7	ADC initializing/Error
8	Reserved
9	Zero/Span Calibration Error
10~15	Reserved

- AI Max Value: 2 octets
  The maximum of AI raw data with range 0 to 0xFFFF.

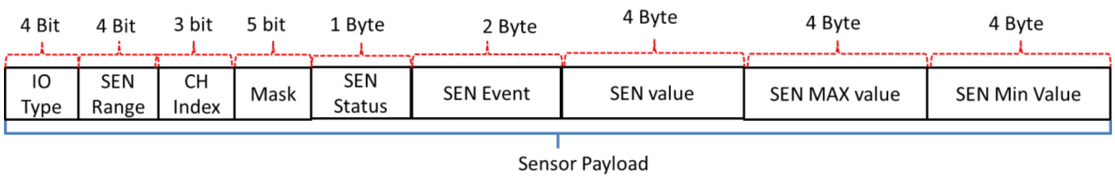
- AI Min Value: 2 octets
  The minimum of AI raw data with range 0 to 0xFFFF.

4.5 Sensor data (I/O Type: 0x5)

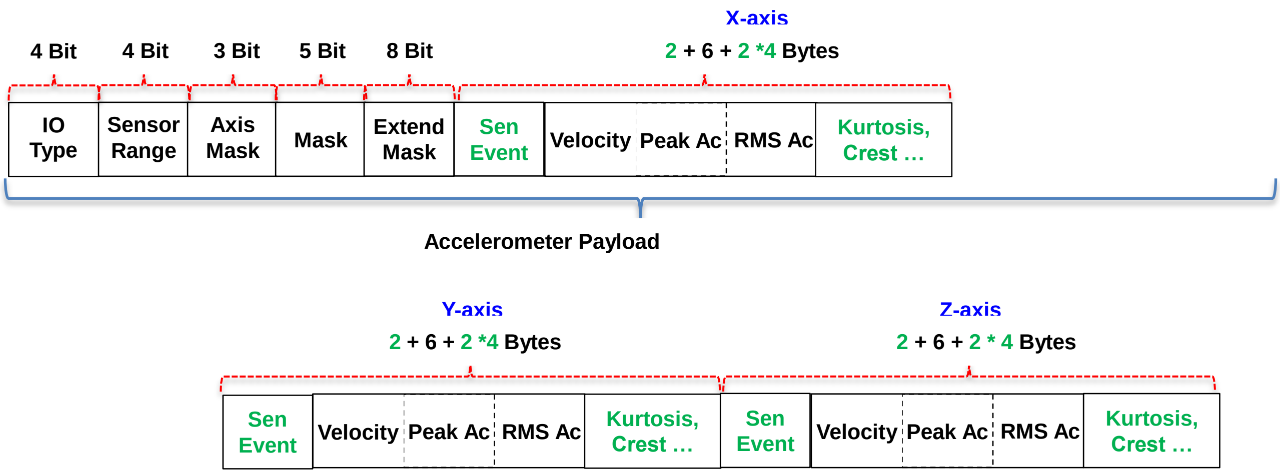
- IO Type (bit 7 – 4): 0x5
- Sensor Range (bit 3 – 0):

(4 bit)	Sensor Type
0x0	4096 - Temperature (℃)
0x1	4097 - Temperature (℉)
0x2	4098 - Temperature (K)
0x3	4128 - Humidity (%)
0x4	4256 - Accelerometer
0x5 – 0xF	(RFU)

<u>Temperature/Humidity</u>:



<u>Accelerometer</u>:



- CH Index/Axis Mask (bit 7 – 5):

	Range: 0x0 – 0x3 Temp./Humidity	Range: 0x4 Accelerometer
Bit 0	0	X-axis
Bit 1	0	Y-axis
Bit 2	0	Z-axis

- MASK (bit 4 – 0):

Bit	Range: 0x0 – 0x3 Temp./Humidity	Range: 0x4 Accelerometer
Bit 0	Sensor Status (1 Byte)	(Reserved)
Bit 1	Sensor Event (2 Bytes)	Sensor Event (2 Bytes)
Bit 2	Sensor Value (4 Bytes)	(Reserved)
Bit 3	Sensor Max Value (4 Bytes)	(Reserved)
Bit 4	Sensor Min Value (4 Bytes)	(Reserved)

Extend MASK (bit 7 – 0)

Bit	Range: 0x0 – 0x3 Temp./Humidity	Range: 0x4 Accelerometer
Bit 0	(No support)	OA Value of Vibration Velocity (0.01 mm/sec) (2 Bytes)
Bit 1		Peak Value of Acceleration (0.001g) (2 Bytes)
Bit 2		RMS of Acceleration (0.001g) (2 Bytes)
Bit 3		Kurtosis (2 Bytes)
Bit 4		Crest factor (2 Bytes)
Bit 5		Skewness (2 Bytes)
Bit 6		Standard deviation (2 Bytes)
Bit 7		(Reserved)

- SEN Status (1 octet):

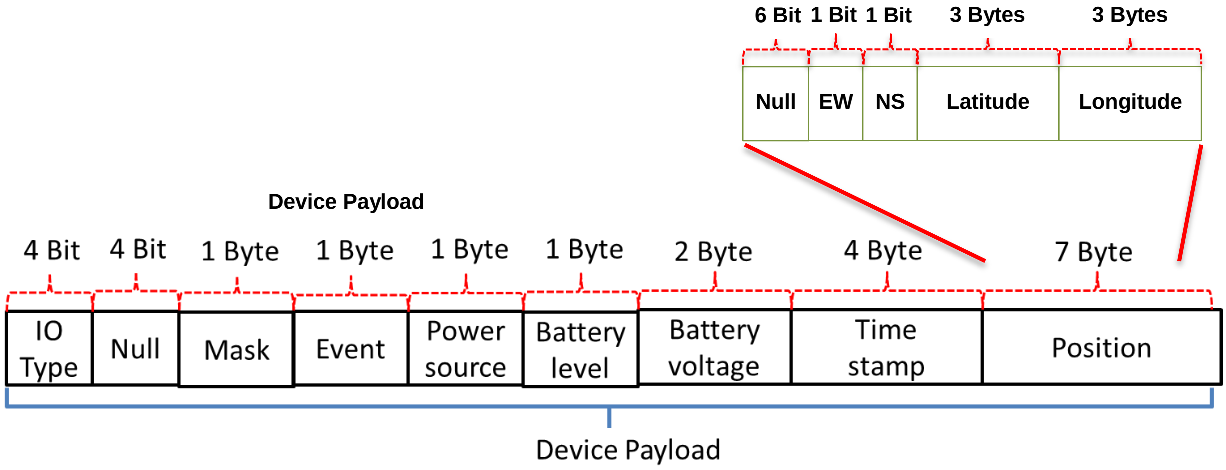
	Range: 0x0 – 0x3 Temp./Humidity
Bit 0	Sensor fail
Bit 1 - 7	Reserved

- SEN Event (2 octets):

Bit	Range: 0x0 – 0x3 Temp./Humidity	Range: 0x4 Accelerometer
Bit 0	High alarm status Read 1: high alarm occurred. 0: not occurred Write 0: clear the high alarm status	High alarm status of velocity RMS Read 1: high alarm occurred. 0: not occurred Write 0: clear the high alarm status
Bit 1	Low Alarm Status Read 1: low alarm occurred. 0: not occurred Write 0: clear the low alarm status	(Reserved)

Bit 2	Clear Maximum Sensor Value 1: Clear the maximum Sensor value	(Reserved)
Bit 3	Clear Minimum Sensor Value 1: Clear the minimum Sensor value	(Reserved)
Bit 4	Alarm update	(Reserved)
Bit 5 ~ 15	(Reserved)	(Reserved)

4.6 Device data (I/O Type: 0x6)



- IO Type (bit 7 – 4): 0x6
- MASK (bit 7 – 0)

Bit 0	Device event
Bit 1	Power source
Bit 2	Battery level
Bit 3	Battery voltage
Bit 4	Timestamp
Bit 5	Position
Bit 6~7	Reserved

- Device Event: 1 octet

Device event status table is shown below.

Bit Order	Description

0	Battery low
1	RTC low
2~7	Reserved

- Power Source: 1 octet

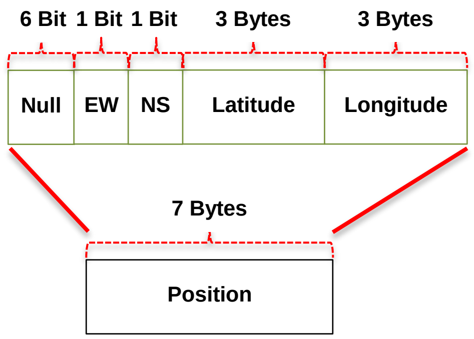
  Power source table is shown below.

Bit Order	Description
0	Power line
1	Battery
2	Solar panels
3~7	Reserved

- Battery Level: 1 octet

  The level of battery with range 0 to 100 (%).
- Battery voltage: 2 octets

  The battery voltage with range 0 to 65.535V.
- Timestamp : 4 octets
- Position : 7 octets



[Note]

*Position (GNSS)

- NS (bit 0)

  Latitude: 0 for N, 1 for S
- EW (bit 1)

  Longitude: 0 for E, 1 for W

- Latitude/Longitude: 3 octets for each

  The format of GPS location is:

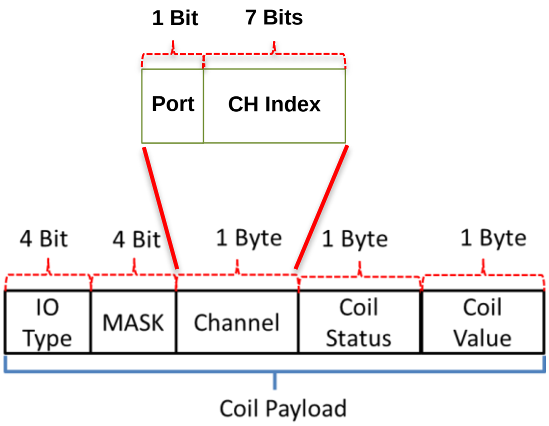
  Latitude dd[degree]mm.mmmm[minutes]

  Longitude ddd[degree]mm.mmmm[minutes]

Each of them is encoded as 3-bytes hexadecimals by diving minutes by 60 and multiplying the result by a factor of 10^5, and use the first byte to indicate their sign values.
For example:
Latitude 4807.038,N => 48d07.038m => (48+07.038/60)*10^5 = 4811730 => 0x496BD2
Longitude 01131.000,W=>11d31000m => (11+31/60)*10^5 = 1151666 => 0x1192B2
Sign 0 for N, 1 for W => (0x0 << 1) | (0x 1) = 0x01;
The position data above results in 7-bytes GPS payload as below:

0x01 0xD2 0x6B 0x49 0xB2 0x92 0x11

4.7 RS-485 Coil data (I/O Type: 0x7)



- IO Type (bit 7 – 4): 0x7
- MASK (bit 3 – 0)

Bit 0	Coil Status
Bit 1	Coil Value

- Channel (1 octet):

COM port number and coil channel index.

Bit 0 ~ 6	Coil Channel Index: 0 ~ 31 or 0~63
Bit 7	COM Port Index: 0 – COM port 1 1 – COM port 2

- Coil status: 1 octet

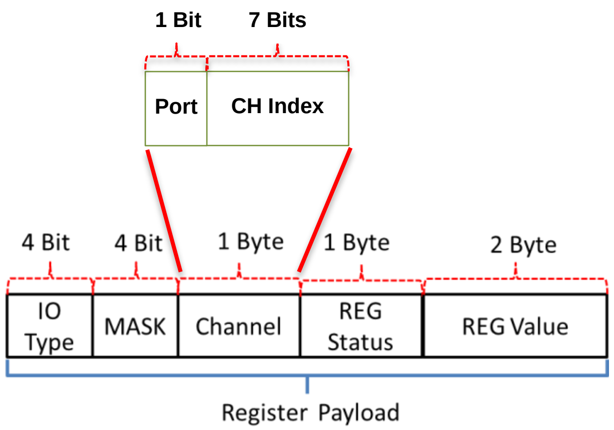
The error status of polling this coil

Status Value	Description
0 (0x00)	No error
1 (0x01)	Illegal function
2 (0x02)	Illegal data address
3 (0x03)	Illegal data value
4 (0x04)	Slave device failure
5 (0x05)	Acknowledge
6 (0x06)	Slave device busy
7 (0x07)	Negative acknowledge
8 (0x08)	Memory parity error
9 (0x09)	Reserved
10 (0x0A)	Gateway path unavailable
11 (0x0B)	Gateway target device failed to respond
12 ~15	Reserved
16 (0x10)	Unavailable
17 (0x11)	Slave response timeout
18 (0x12)	Checksum error
19 (0x13)	Received data error
20 (0x14)	Send request fail
21(0x15)	Unprocessed
22(0x16)	Read only
23(0x17)	In processing

- Coil value: 1 octet

The coil data, 0 or 1

4.8 RS-485 Register data (I/O Type: 0x8)



- IO Type (bit 7 – 4): 0x8
- MASK (bit 3 – 0)

Bit 0	Register Status
Bit 1	Register Value

- Channel (1 octet):

COM port number and register channel index.

Bit 0 ~ 6	Register Channel Index: 0 ~ 31 or 0~63
Bit 7	COM Port Index: 0 – COM port 1 1 – COM port 2

- Register status: 1 octet

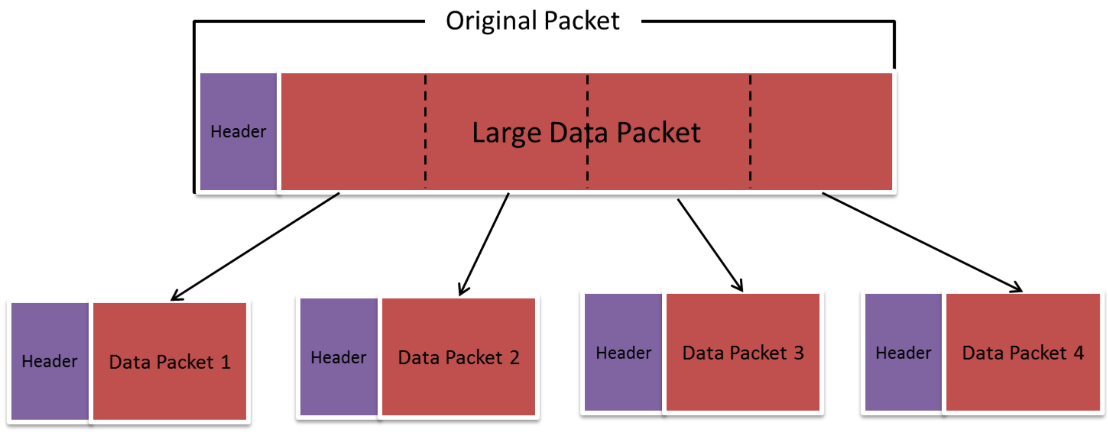
The error status of polling this channel can refer to Coil Status in the previous section.

- REG value: 2 octets

The register data with range 0 to 0xFFFF

5 Packet Fragmentation and Reassembly

Because the data rate is controlled by the network, the length of each uplink is not fixed. The Frame Payload (FRM Payload) will be split into multiple fragments.



A complete frame can be divided into several uplink messages.

Frame Payload (FRM Payload)		
WHDR	WPayload	WCRC

1st message:

WHDR				WPayload*
Octet: 1	1	1	0	Variable
Frame Control	Frame Sequence Number	Total Length	Source Address	A partial of WISE Payload
0x80	S	M		

2nd ~ nth messages

WHDR				WPayload*
Octet: 1	1	0	0	Variable
Frame Control	Frame Sequence Number	Total Length	Source Address	A partial of WISE Payload
0x00	(S+1) ~			

The last message:

WHDR				WPayload*	WCRC
Octet: 1	1	0	0	Variable	1

Frame Control	Frame Sequence Number	Total Length	Source Address	The rest of WISE Payload	CRC
0x00	(S+n)				0x23