

User's Manual

LA-2132 LVDS

LA-2132 Series

LA-2164 Expand

Logic Analyzer

Revision II
Software Win 98/me/2000/xp/Vista Version



CLOCK COMPUTER CORP.

<http://www.clock-link.com.tw>

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Item Checklist

1. The LA-2132 LVDS or LA-2132 Series Plastic unit.

There are two Models is available for LA-2132 LVDS:

LA-2132 LVDS: (32 channels only, can't expand to 64 Channels).

- K2 (250MHz, 256K Memory, 2 Trigger Levels, support LVDS, LPECL).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels, support LVDS, LPECL).

There are nine Models is available for LA-2132 Series:

LA-2132K Series: (Expand to 64 channels is available, without support **LVDS, LPECL**).

- K2 (250MHz, 256K Memory, 2 Trigger Levels).
- K8 (250MHz, 256K Memory, 8 Trigger Levels).
- K512 (250MHz, 256K Memory, 512 Trigger Levels).

LA-2132M Series: (Expand to 64 channels is available, without support **LVDS, LPECL**).

- M2 (500MHz, 1Mega Memory, 2 Trigger Levels).
- M8 (500MHz, 1Mega Memory, 8 Trigger Levels).
- M512 (500MHz, 1Mega Memory, 512 Trigger Levels).

LA-2132G Series: (Expand to 64 channels is available, without support **LVDS, LPECL**).

- G2 (1GHz, 4Mega Memory, 2 Trigger Levels).
- G8 (1GHz, 4Mega Memory, 8 Trigger Levels).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels).

2. One 20 pin flat cable (Length is 25 CM).

[This 20 pin flat cable use for LA-2132 Expand to 64 Channels only].

3. Two harness with each 32 color wires and 50 Easy Hook clips.
4. Ten pieces color wires with Easy Hook clips [**this is for LA-2132 LVDS only**].
5. One LA-2132 LVDS / Series User's Manual.
6. One CD for LA-2132 Series driver.
7. One USB 2.0 cable (Mini Type).
8. One special USB 2.0 cable (Mini Type) with 2 head connector.

[**This special 2 head connector USB 2.0 cable use for LA-2132 Expand to 64 Channels only**].

System Requirements

In order to use the Logic Analyzer, the following equipment is necessary:

- Computer System : Support USB interface (USB 1.1 or 2.0 version)
- Memory : A minimum of 128 Mega free RAM. 512 Mega or 1024 Mega is better.
- Mass Storage : At least one CD drives and hard disk drives.
- Display Adapter : At least one of VGA Adapter.
Two display interface are better [**Resolution 1440 X 900 is better**].
- Monitor : Any monitor compatible with the above display adapter. Two monitor is better.
- Operation System : Windows me / 2000 / XP / Vista.

Installing Hardware

Installing LA-2132 LVDS or LA-2132 Series with USB 2.0 Cable.

Please follow these instructions for installing the Logic Analyzer with USB cable.

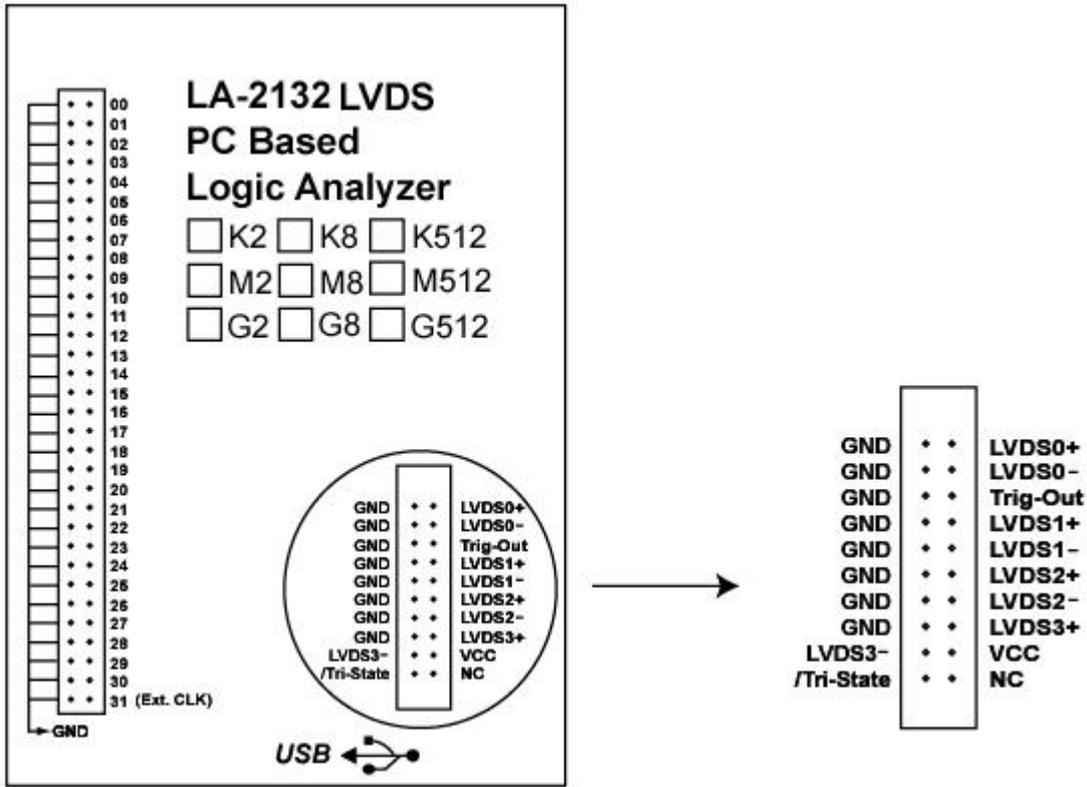
1. Turn off the computer and all peripherals connected. Remove the computer power cord from the wall outlet. Locate an available USB interface (version USB 2.0 or USB 1.1).
2. Connect the included USB cable to USB interface.
3. Connect the other end of the USB cable to the LA-2132 USB port.
4. After checking all connections, turn on the computer and peripherals. You are now ready to install the software.

Installing Software

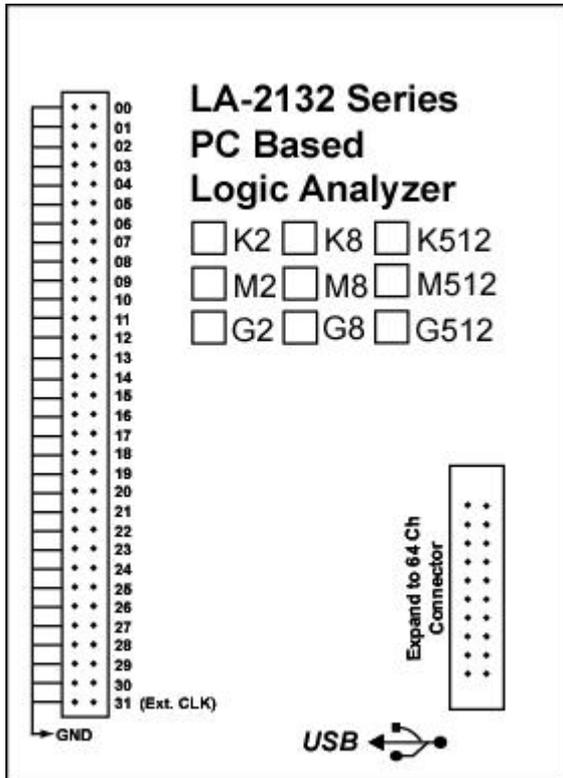
1. Insert the distribution CD into drive E: ("E" is CD driver).
2. Run Windows.
3. Select File menu.
4. Select Run option.
5. Enter file to run setup.exe
6. Follow the on screen instructions.

I/O Pin Location

LA-2132-LVDS: (32 channels only, can't expand to 64 channels).

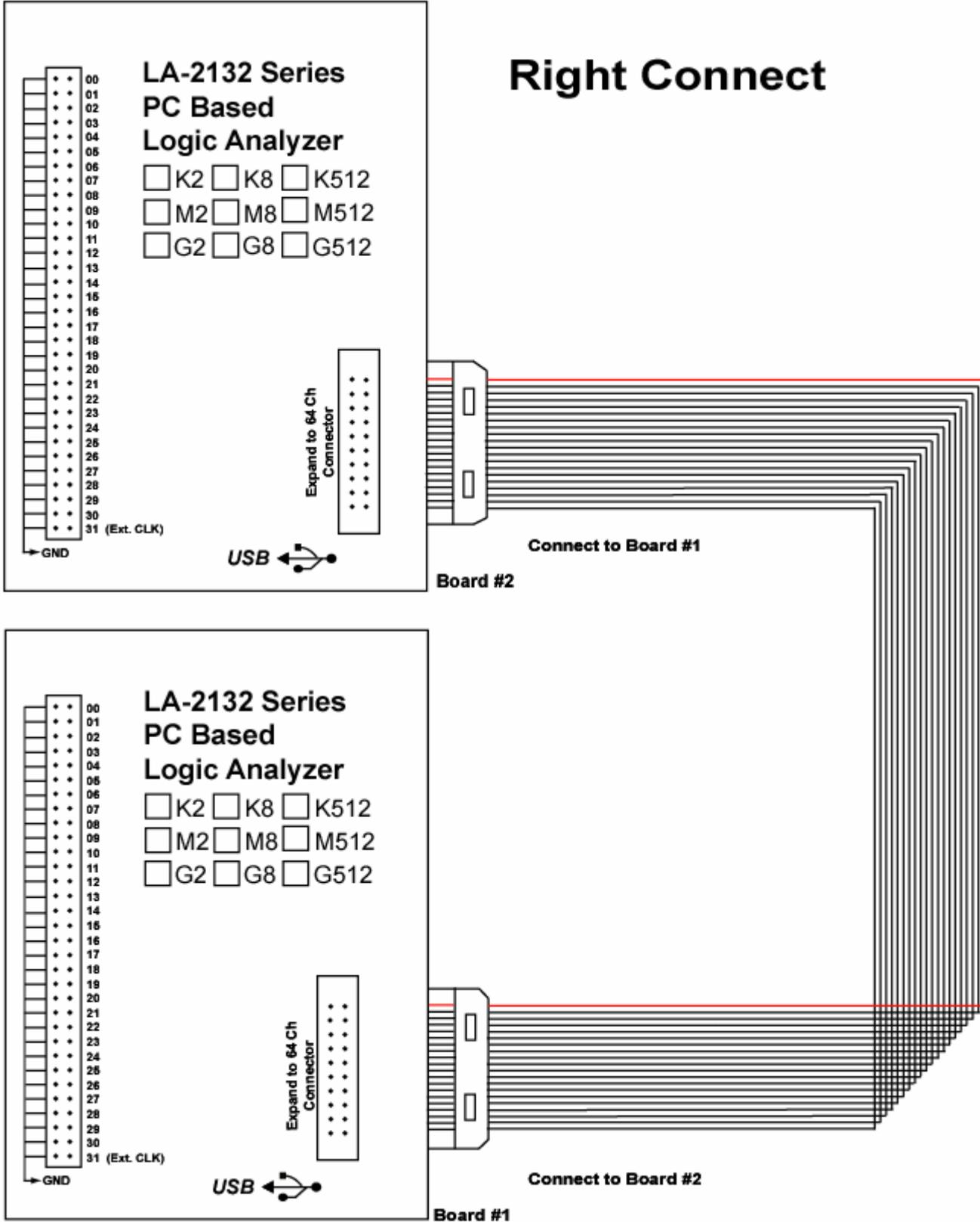


LA-2132 Series: (Expand to 64 channels is available, without support LVDS).



Expand To 64 Channels

The LA-2132 Series can be Expanded to 64 Channels by use one 20 pin flat cable from #1 LA-2132 connect to #2 LA-2132, (it only support 32 channels trigger word even it is 64 channels now).



**Note: It can Expand to 64 channels when the two LA-2132 Series connect together
By one 20 pins flat cable (But LA-2132 LVDS can not Expand to 64 channels).
Please take a notice in order to support enough current, it is better to use
2 head of Special USB 2.0 cable insert to USB 2.0 port of your computer.**

Guide To Operations

Hardware

When making measurements with the Logic Analyzer, meaningful data can only be captured with some prior knowledge of the characteristics of the circuit under test.

Before initiating any capture cycles, the Logic Analyzer must be configured using the control program. See the software section later in the manual for instructions on these procedures.

To connect the Logic Analyzer to the test circuit, a series of mini-clips on the Logic Analyzer input channels. The LA-2132 Logic Analyzer has inputs for 32 channels ch0 to ch31.

the ch31 channel is the external clock input.

At times, it may also be necessary to connect the test circuit to the computer system itself.

This will eliminate more noise in the test application due to ground level differentials. This is especially true when dealing with high speed timing analysis. Use a heavy gauge wire to make a connection between the test circuit ground and the case of the computer.

Connecting Wires to Logic Analyzer

It has 64 pins [dual in line 32 pins posts]. They are organized as follows:

Right side:

00..31 Channels 0..31

ch 31 External clock input

Left side all pins are **Ground** connection

The wires and the clips are modular. the wires and clips can all be disconnected from each other by gently pulling them apart. Removing just the clips, but leaving the wires connected to the pods allows connections to be made to wires and posts of the test circuit of up to 0.64 mm (0.025 in).

Do not insert wires or posts greater than this diameter as that will expand the contacts in the wire beyond the allowed limit, possibly damaging the connector.

LVDS (Low Voltage Differential Signal)

LA-2132 LVDS has another connector header [dual in line 10 pins posts]

it has 4 LVDS signals 1 tri-state control input signal. 1 trigger out.

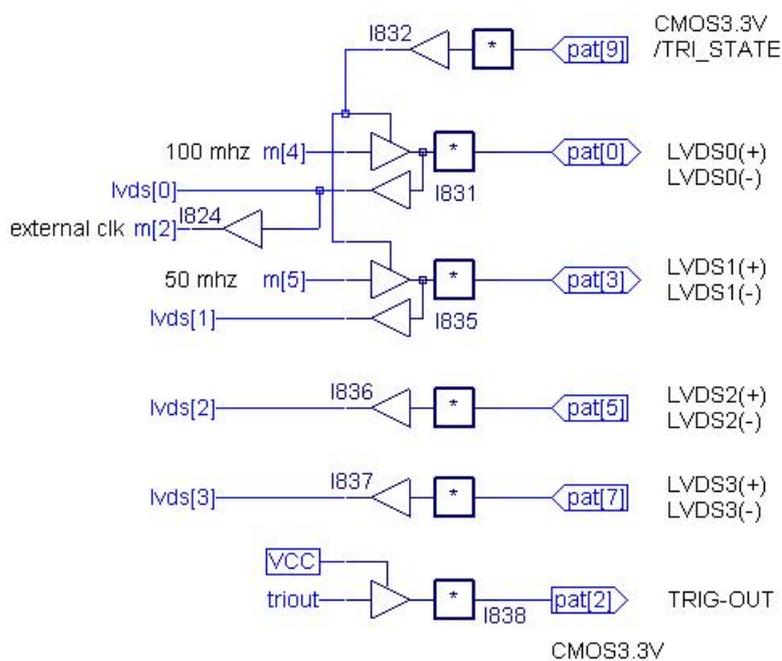
The following diagram show 2 channels bi-direction LVDS with 1 channel tri-state control and 2 channels LVDS input signal and 1 trigger out.

/Tri-State control line is pulled low to 10 Kohm.

It can out 100 MHz and 50 MHz LVDS signal if /Tri-State is pulled high or connected to 5V.

LVDS0, LVDS1, LVDS2, LVDS3 are LVDS signal. LVDS0, LVDS1 has 1 Kohm cross it.

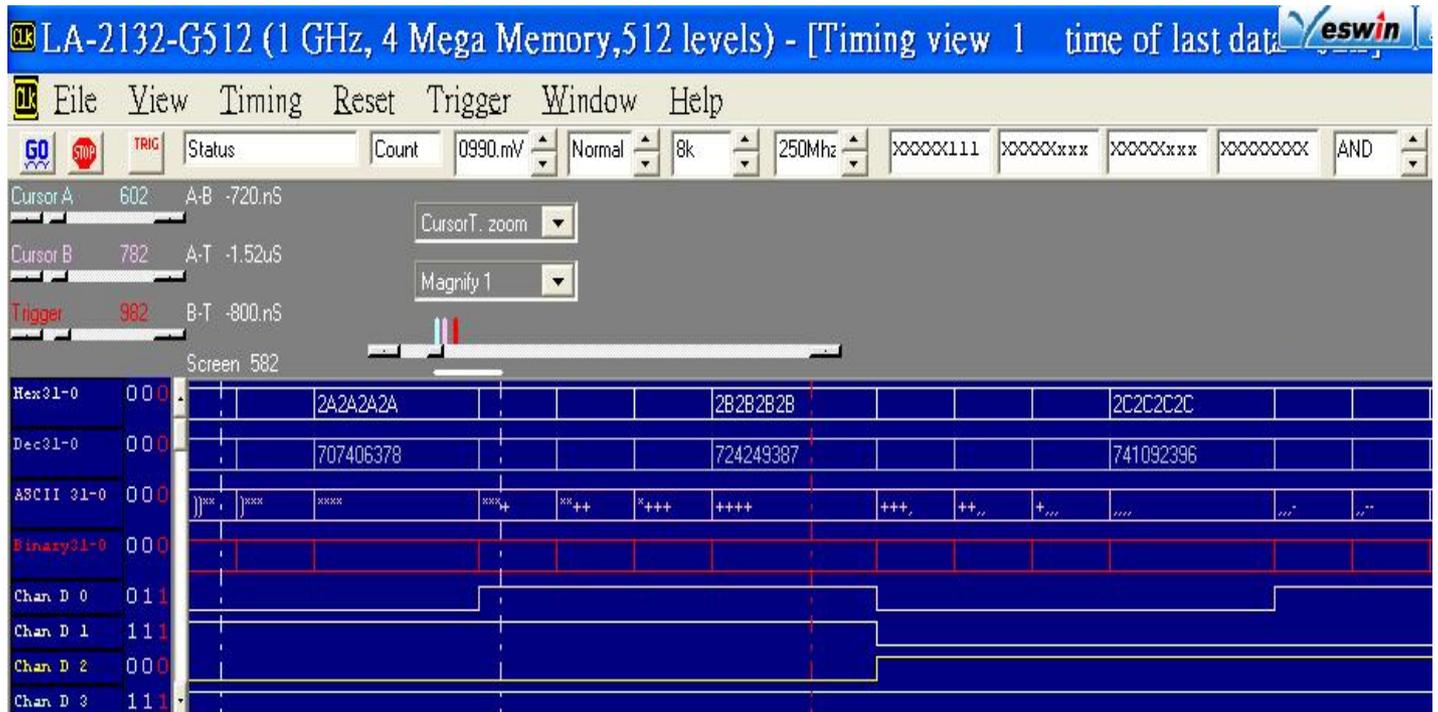
It also can accept LPECL signal. LVDS0 can work as external clock.



Caution: All these signals only accept 0 - 5 Volts, exceed this range will damage this Logic Analyzer.

Vcc inhibit short to ground otherwise your computer will damage.

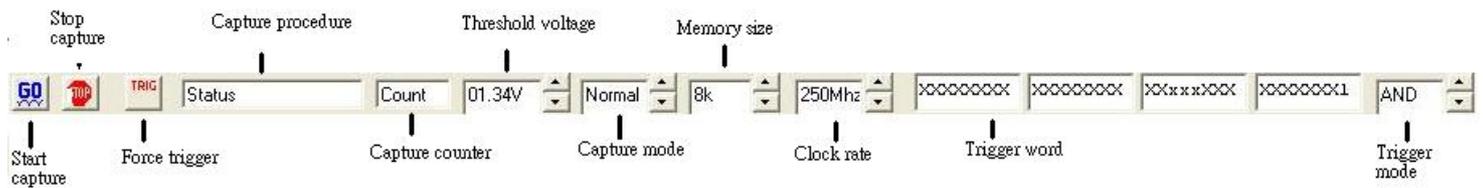
Main Screen



Menu bar



Tool bar

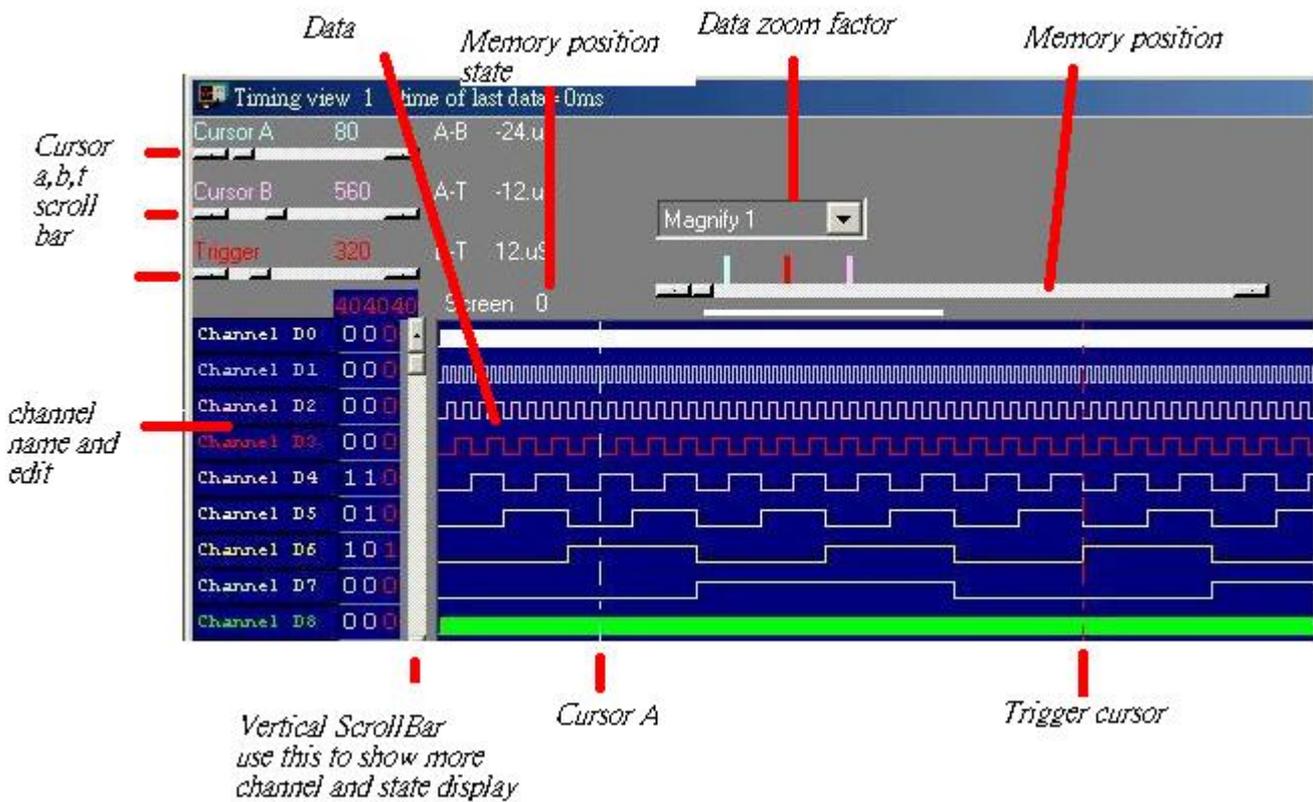


State list

Data is displayed in state list format in this window.

Position	Hexadecimal	Decimal	ASCII	Binary	Example	USER1
0	000000	0		00000000000000000000000000000000	/read	
1	000000	0		00000000000000000000000000000000	/read	
2	000000	0		00000000000000000000000000000000	/read	
3	000000	0		00000000000000000000000000000000	/read	
4	000000	0		00000000000000000000000000000000	/read	
5	000000	0		00000000000000000000000000000000	/read	
6	000000	0		00000000000000000000000000000000	/read	
7	000000	0		00000000000000000000000000000000	/read	
8	000000	0		00000000000000000000000000000000	/read	
9	000000	0		00000000000000000000000000000000	/read	
10	000000	0		00000000000000000000000000000000	/read	
11	000000	0		00000000000000000000000000000000	/read	
12	000000	0		00000000000000000000000000000000	/read	
13	000000	0		00000000000000000000000000000000	/read	

Timing Window



Multi-Window

Software open more timing if system free memory have a lot. So use 512 Mega or 1024 Mega memory will be better.

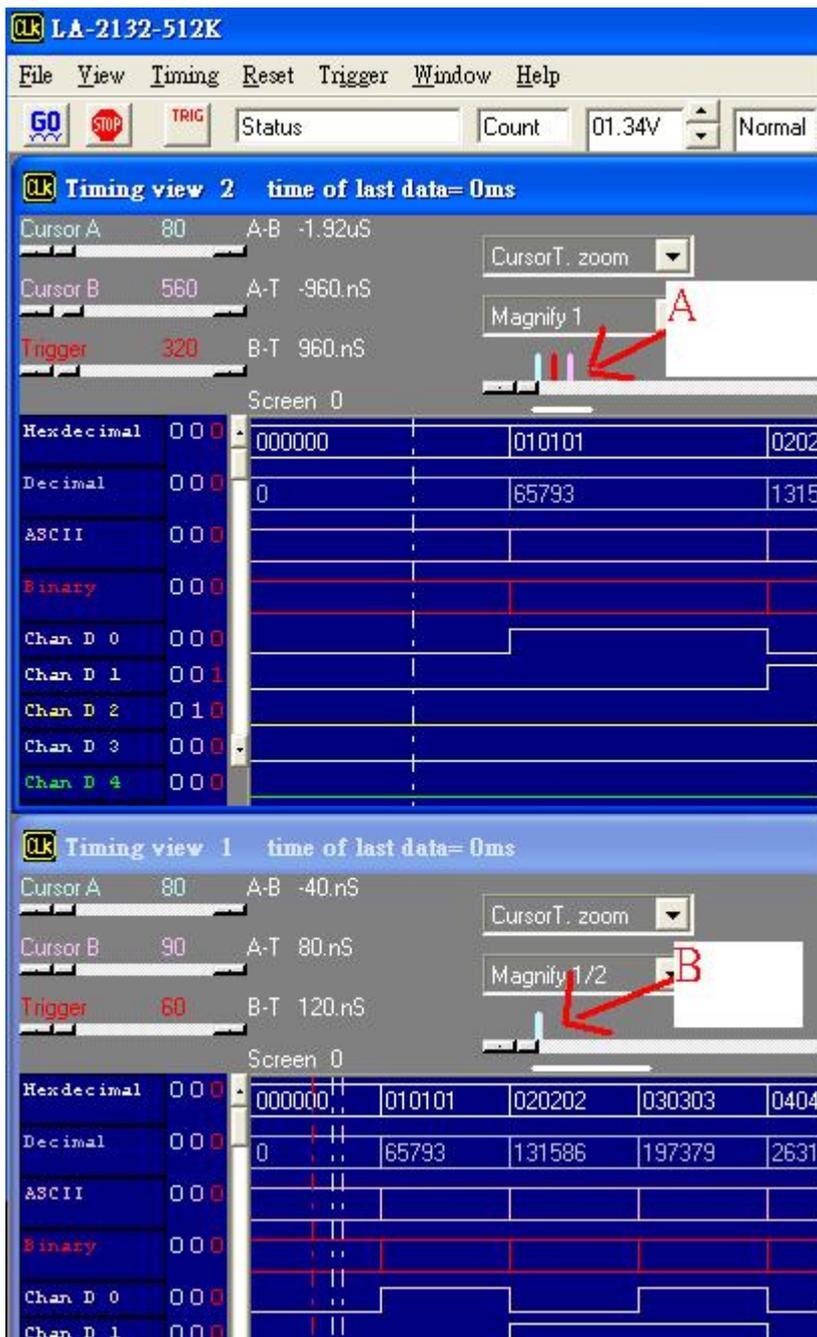
Data1- 4 to timing by point User point which timing memory should be placed for captured data, it can let user captured 2 or 4 set different data to buffer and display, the sequence pointed by user, this function let user have 1Mega*4 memory size.

Data1- 4 to timing by auto The same is true for it, it automatically capture 2 or 4 sets data to buffer, the sequence is 10,9,8,7,6,5,4,3,2 then 1.

Timing1- 4<-data Activate timing display. we suggest user use more than 1 monitor to get better show.

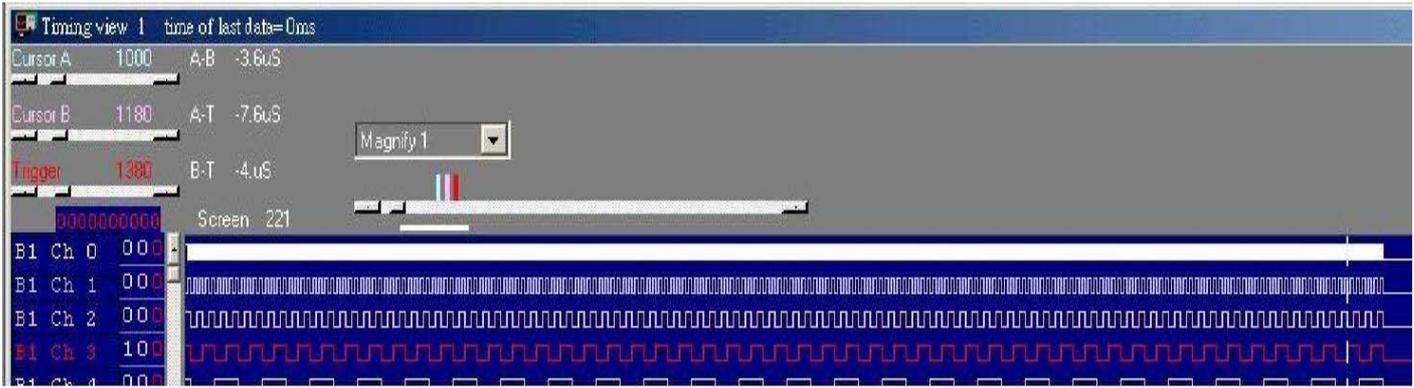
This software is a revolution software, it have a lot of new function, even tradition famous oscilloscope have not these powerful function.

this software show a lot of timing, let user easy to compare and analyzer timing, tradition software no matter it is stand alone or computer base oscilloscope only show one timing, these one timing software only analyzer one segment of buffer, unlike this software it can look buffer in beginning and buffer in middle and buffer in end at the same time. The following picture part A show it is locate at beginning and part B at middle of buffer at the same time, every individual timing also support their own cursor, voltage measurement, zoom factor .. etc.

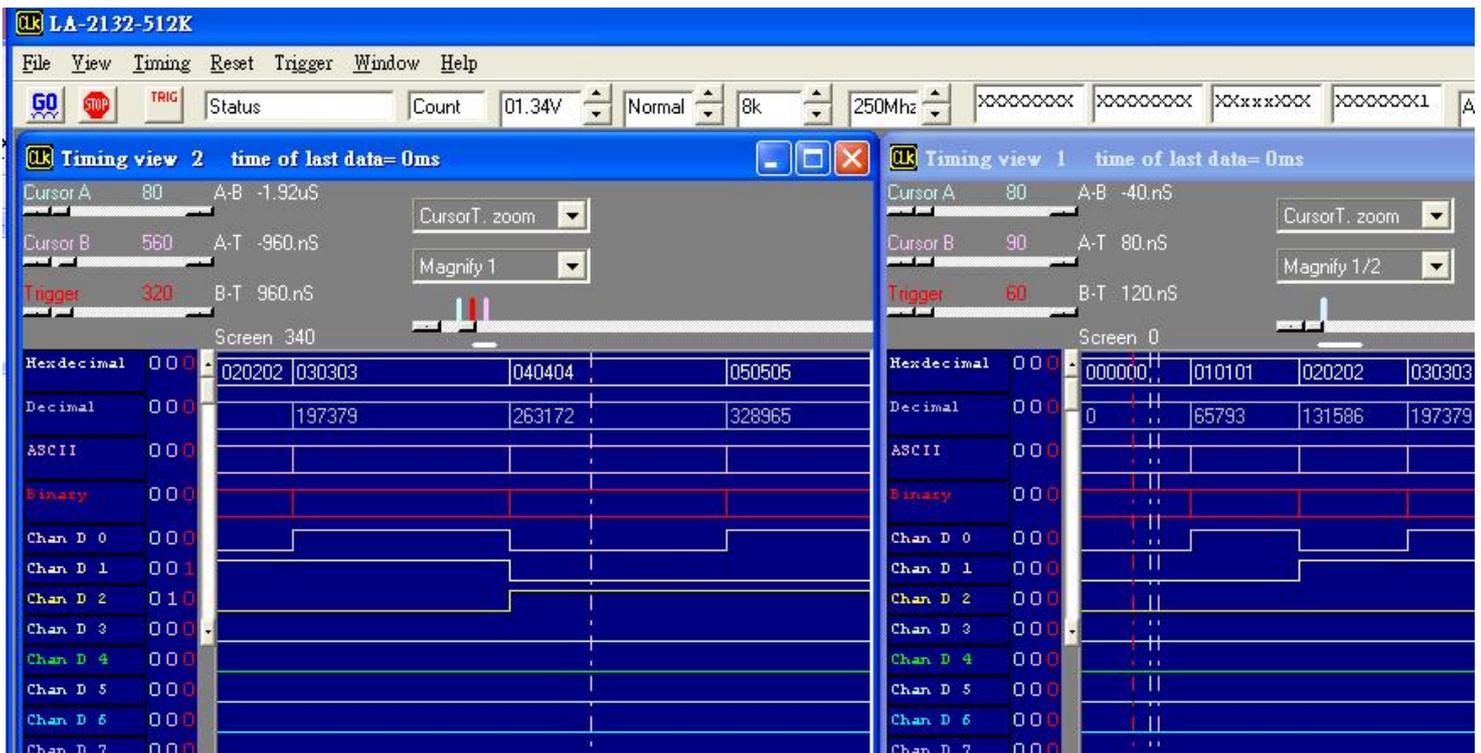


Another new function are let memory expand to 4 times by software, If memory size is 1 Mega size, this software can let it look like have 4 Mega size when user open 4 timing and set 4 timing by auto function. (it need 1024 Mega system memory or more). the method is software continue capture data to these 4 timing, every timing have 1 Mega individual buffer, so user can look almost 4 Mega memory.

it is better than any famous oscilloscope in the world. the third big function are it can show long timing when you have two monitor, the following show two monitor long timing, it can let user easy analyze timing, so the stand alone oscilloscope can not do it, because they only have one monitor.



The fourth function is it can support two different timing at different monitor. the follow picture is left monitor show square waveform with magnify 1 and right monitor show the waveform with magnify 1/2. it easy compare last capture data and current data at different monitor. These function even famous oscilloscope have not support it.



Capture Mode

Set trigger acquisition mode.

- Single The LA looks for the trigger event. When it is found acquire a single buffer worth of data and stop.
- Normal The LA looks for the trigger event. When it is found acquire a buffer worth of data, re-arm and repeat until stop is hit.
- Auto Similar to Normal except that it will acquire regardless of the trigger event.

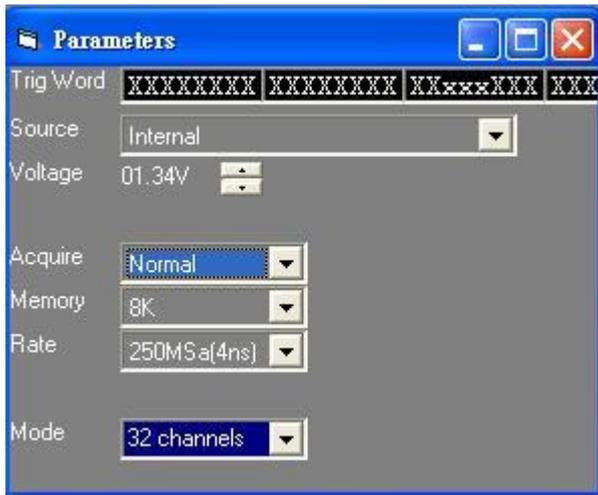
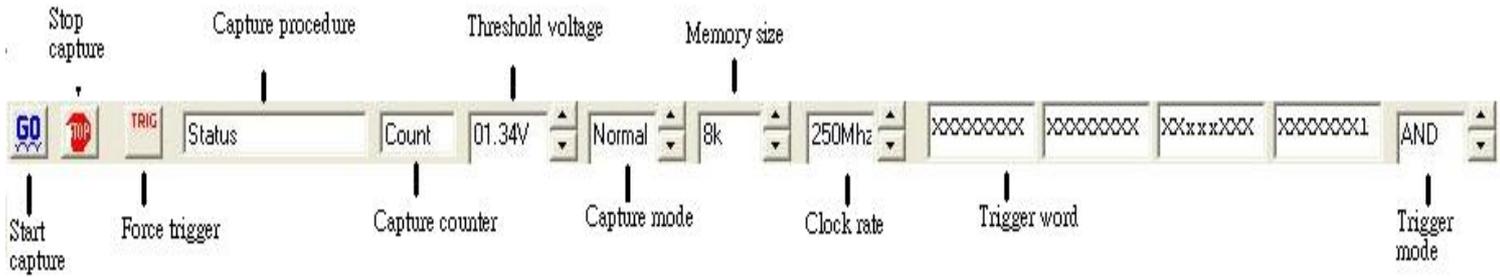
Trigger Mode Setup (Trigger Menu)

Trigger Levels Specifications of LA-2132 Series:

Model	1. LA-2132- K2 (250 MHz, 256 K Memory, 2 Trigger levels) 2. LA-2132- K8 (250 MHz, 256 K Memory, 8 Trigger levels) 3. LA-2132- K512 (250 MHz, 256 K Memory, 512 Trigger levels)	4. LA-2132- M2 (500 MHz, 1 Mega Memory, 2 Trigger levels) 5. LA-2132- M8 (500 MHz, 1 Mega Memory, 8 Trigger levels) 6. LA-2132- M512 (500 MHz, 1 Mega Memory, 512 Trigger levels)	7. LA-2132-G2 (1 GHz, 4 Mega Memory, 2 Trigger levels) 8. LA-2132-G8 (1 GHz, 4 Mega Memory, 8 Trigger levels) 9. LA-2132-G512 (1 GHz, 4 Mega Memory, 512 Trigger levels)
2 Trigger Levels	with IF word xx happen yy times then next level else go to level 0 trigger structure . 1048576 event counter/every level 1 to 1048576* (1 sec to 10nsec) delay time /every levels ----- detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232...) (NO) I ² C serial trigger (NO)	with IF word xx happen yy times then next level else go to level 0 trigger structure. 1048576 event counter/every level 1 to 1048576* (1 sec to 10nsec) delay time /every levels ----- detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232...) (NO) I ² C serial trigger (NO)	with IF word xx happen yy times then next level else go to level 0 trigger structure. 1048576 event counter/every level 1 to 1048576* (1 sec to 10nsec) delay time /every levels ----- detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232...) (NO) I ² C serial trigger (NO)

8 Trigger Levels	with IF word xx happen yy times then next level else go to level 0 trigger structure. 1048576 event counter/every level 1048576*(1 sec to 10nsec) delay time /every levels	with IF word xx happen yy times then next level else go to level 0 trigger structure. 1048576 event counter/every level 1048576*(1 sec to 10nsec) delay time /every levels	with IF word xx happen yy times then next level else go to level 0 trigger structure. 1048576 event counter/every level 1048576*(1 sec to 10nsec) delay time /every levels
	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232.)(difficulty) can work for 3 bit serial stream only I ² C serial trigger (NO)	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232.)(difficulty) can work for 3 bit serial stream only I ² C serial trigger (NO)	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232.)(difficulty) can work for 3 bit serial stream only I ² C serial trigger (NO)
512 Trigger Levels	with IF word xx happen yy times then next level else go to level 0 trigger structure 1048576 event counter / every level 1048576* (1 sec to 10nsec) delay time / every levels.	with IF word xx happen yy times then next level else go to level 0 trigger structure 1048576 event counter / every level 1048576* (1 sec to 10nsec) delay time / every levels.	with IF word xx happen yy times then next level else go to level 0 trigger structure 1048576 event counter / every level 1048576* (1 sec to 10nsec) delay time / every levels.
	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232...) (YES) I ² C serial trigger (YES) all kind of trigger (YES) it is universal trigger structure	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232...) (YES) I ² C serial trigger (YES) all kind of trigger (YES) it is universal trigger structure	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232...) (YES) I ² C serial trigger (YES) all kind of trigger (YES) it is universal trigger structure

A trigger word is the pattern that the Logic Analyzers needs to see before it will start to acquire data. The trigger word is made of a series of "1", "0" and "x" (don't care) bits. AND mode need 32 channels all match trigger condition. OR mode need one of 32 channels match trigger condition. It can set at toolbar or parameters form.



Ch31..24

Edit pattern for channels 31 to 24

Ch23..16

Edit pattern for channels 23 to 16

Ch15..8

Edit pattern for channels 15 to 8

Ch7..0

Edit pattern for channels 7 to 0

Logic

Trigger if condition is true or false.

True logic need trigger condition from false to true.

False logic need trigger condition from true to false.

How to Set Trigger Word

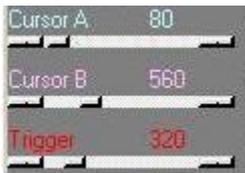
1) You can edit all 32 channels at a time.

Edit the pattern: The LSB is to the right. Each bit can be set to "0", "1" or "x" (don't care, true, false).

2) You can set the trigger logic to "True" (trigger when pattern matches) or "False" (trigger when pattern stops matching).

Trigger Position

The trigger position defines how much data is captured prior to the trigger event and how much data stored after it. You set the Trigger position by moving the trigger cursor. This feature allows you to see the data that led up to the trigger as well as what happened after the trigger.

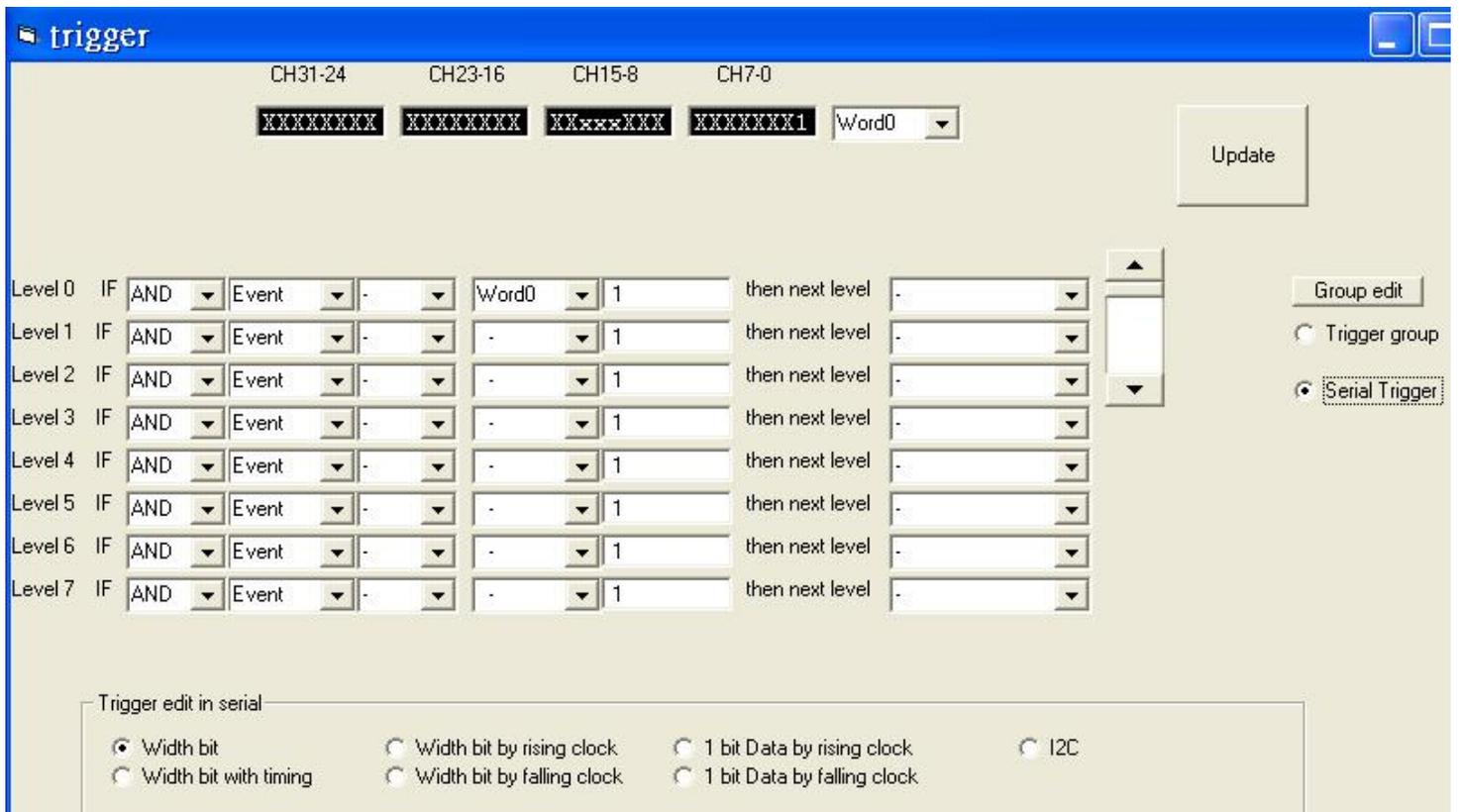
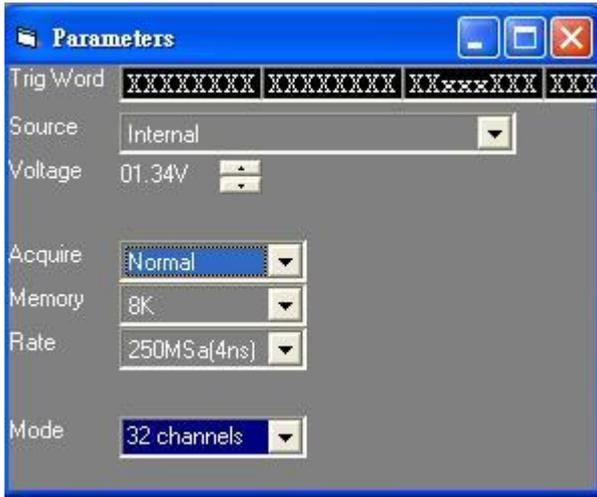


Trigger Word Setup

A sequence of up to 512 trigger words can be set. A trigger word is the pattern that the Logic Analyzers needs to see before it will start to acquire data. The trigger word is made of a series of "1", "0" and "x" (don't care) bits.

It can set trigger word at toolbar or parameter form or trigger form.





This logic analyzer support 2,8,512 trigger levels. Depend on which model user bought it, Because logic word now is very complex, like RS232, I²C.... need a lot of trigger level to complete it. Every trigger level support " if xx happen xx times then next level else go to 0". AND mode need 32 channels all match trigger condition. OR mode need one of 32 channels match trigger condition. Event : allow trigger happen after match trigger condition max 1048576 times.

Delay : wait 1 to 1048576* (1 sec to 10nsec).

You can set the trigger logic to "Enter" (trigger when pattern matches) or "Exit" (trigger when pattern stops matching).

Two trigger check be selected "trigger group" and serial trigger.

Trigger group check : Select which base you want to edit in.

Serial trigger : 7 kind of serial trigger can be selected as following:

Width Bit

Tradition logic analyzer only support 1 trigger level.

Advance logic analyzer can let this trigger word pass n time.

n =1 to 1048576.

In the following example, it will trigger if condition trigger word 55 happen 10 times.

like as 77,44,22,55,66,55,66,55,66,55,66,55,44,55,33,55,22,55,22,55,77,55 ← trigger here.

The screenshot shows the 'trigger' software interface. At the top, there are four channels: CH31-24, CH23-16, CH15-8, and CH7-0. Below them are four input fields: 'XXXXXXXX', 'XXXXXXXX', 'XXXXXXXX', and '01010101'. A dropdown menu is set to 'Word0'. An 'Update' button is on the right.

The main area contains a table of trigger levels:

Level	IF	AND	Event	Enter	Word0	Count	then next level
Level 0	IF	AND	Event	Enter	Word0	10	-
Level 1	IF	AND	Event	Enter	-	1	-
Level 2	IF	AND	Event	Enter	-	1	-
Level 3	IF	AND	Event	Enter	-	1	-
Level 4	IF	AND	Event	Enter	-	1	-
Level 5	IF	AND	Event	Enter	-	1	-
Level 6	IF	AND	Event	Enter	-	1	-
Level 7	IF	AND	Event	Enter	-	1	-

On the right side, there are radio buttons for 'Trigger group' and 'Serial Trigger' (which is selected). A 'Group edit' button is also present.

Below the table is a 'Trigger edit in serial' section with several radio button options:

- Width bit
- Width bit by rising clock
- 1 bit Data by rising clock
- I2C
- Width bit with timing
- Width bit by falling clock
- 1 bit Data by falling clock

At the bottom, there is a list of trigger words. The first one is '0' with a value of '55' and '8 Bit' selected. There are 'Clear trigger' and 'Go to level 0' buttons. A 'Decimal' checkbox is unchecked, and a 'Hex' checkbox is checked.

It also can set delay n time, n =1 to 1048576. time delay unit from 10nsec to 1 sec.

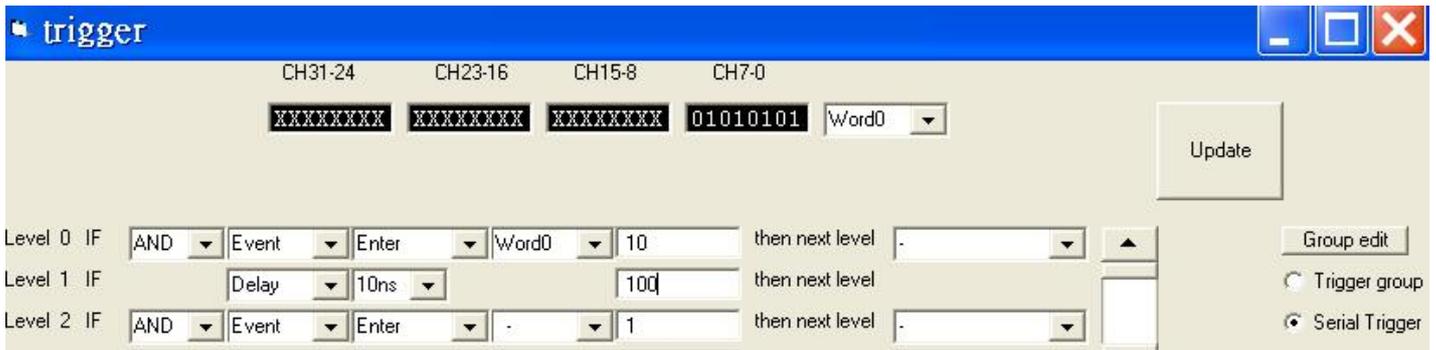
Some time we call this function as **TRIGGER BEFORE DELAY**.

It is useful when we need to look data after reset signal a long period.

In next diagram, it trigger after 10 times trigger word 55 with 10nsec*100 time delay

like as 77,44,22,55,66,55,66,55,66,55,66,55,44,55,33,55,22,55,22,55,77,55 -----1 μ sec delay

← trigger here.



At this time all LA-2132 model can work well because it only use two trigger levels to complete.

LA-2132 has 2,8,512 trigger level model.

It need more than 2 trigger levels to complete next diagram example.

The following model can work for it

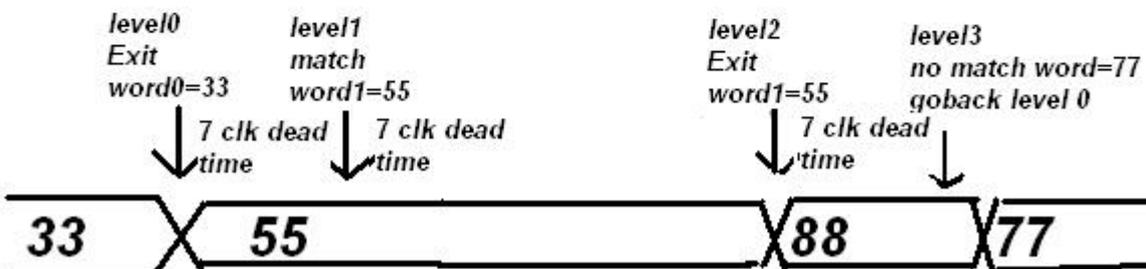
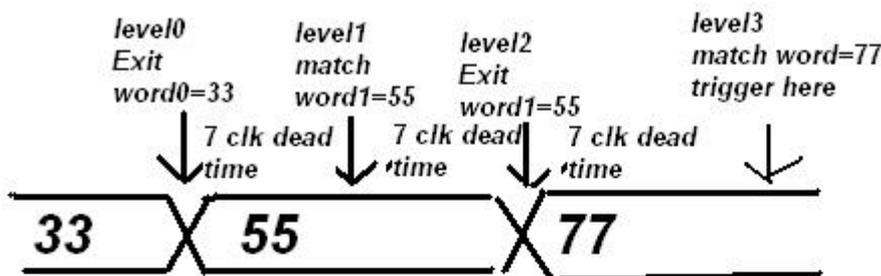
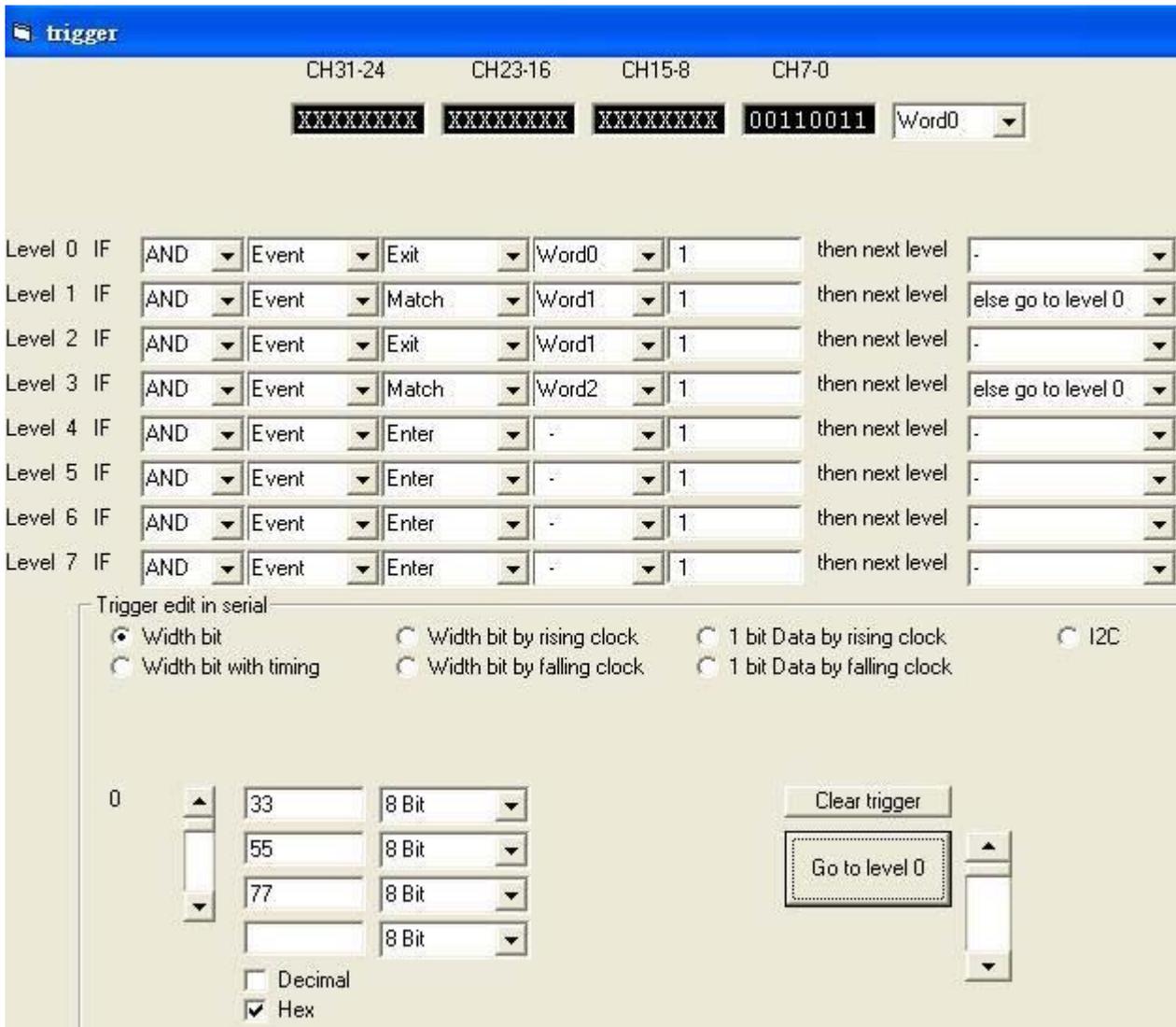
LA-2132-K8 (8 Trigger levels), LA-2132-K512 (512 Trigger levels).

LA-2132-M8 (8 Trigger levels), LA-2132-M512 (512 Trigger levels).

LA-2132-G8 (8 Trigger levels), LA-2132-G512 (512 Trigger levels).

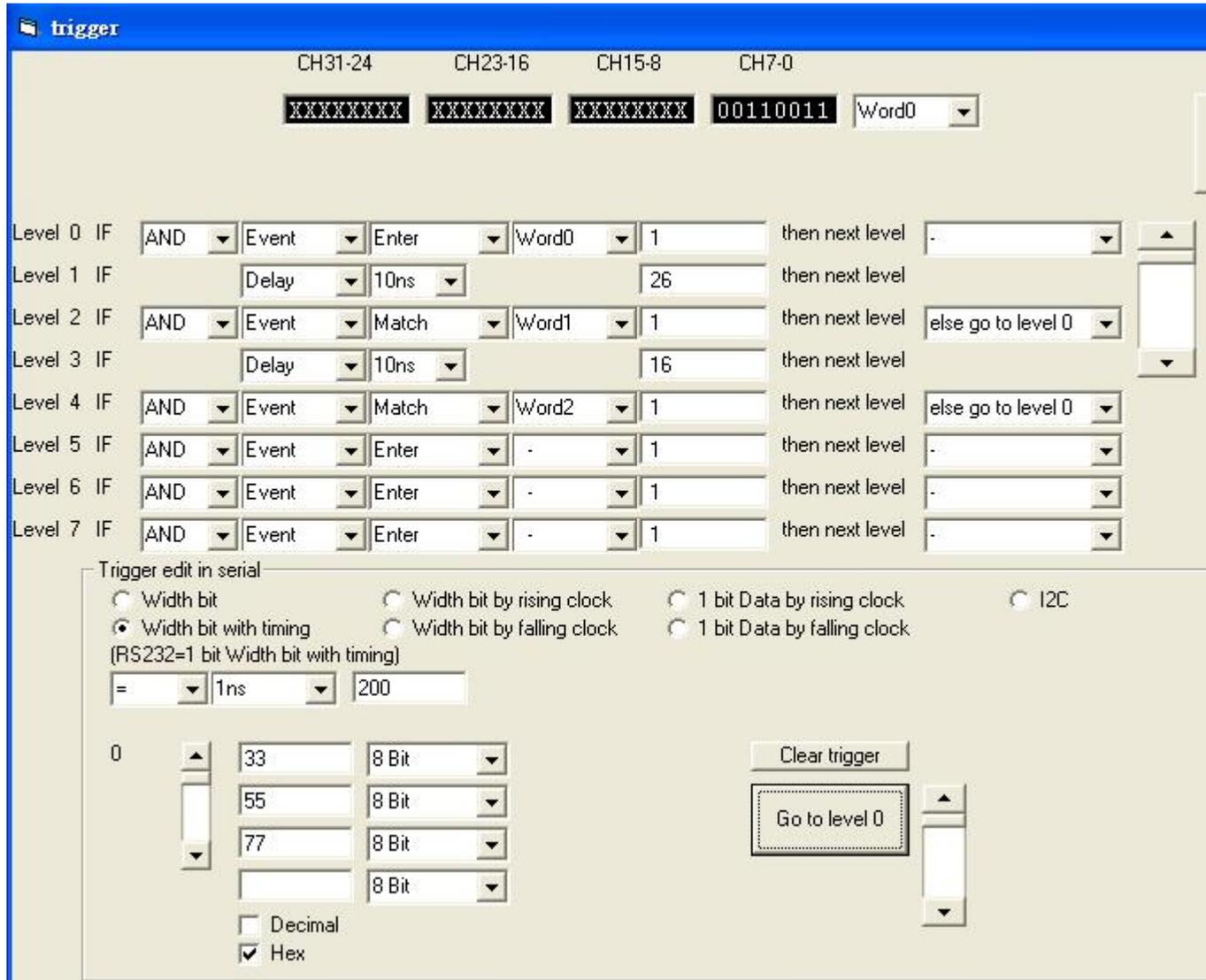
A serial of width bit stream like 33 follow 55 follow 77.

it will not trigger if data stream is 33,66,55,77.



The dead time of trigger level to next level is 7 clocks in 32 channels mode.
 The dead time of trigger level to next level is 14 clocks in 16 channels mode.
 The dead time of trigger level to next level is 28 clocks in 16 channels mode.

Width Bit With Timing



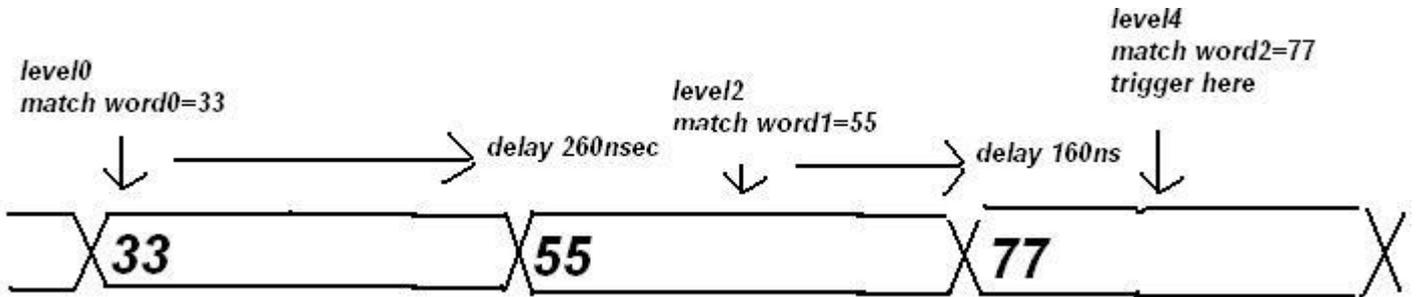
A serial of width bit stream like 33 follow 55 follow 77 by some timing .

It is 200nsec interval in this case.

Trigger commend wait 300nsec after detect trigger word 33 then check it in 200sec every time. 300nsec mean cross trigger word 33 200nsec plus trigger word 55 200nsec/2, equal 300nsec. but system need 7 clock dead time to turn level to level, so it set 260nsec and 160nsec instead. RS232 can be set in this mode, need set to 1 bit width.

The following model can work for it.

LA-2132-K8 (8 Trigger levels), LA-2132-K512 (512 Trigger levels).
 LA-2132-M8 (8 Trigger levels), LA-2132-M512 (512 Trigger levels).
 LA-2132-G8 (8 Trigger levels), LA-2132-G512 (512 Trigger levels).



in this mode, also can detect width pulse in narrow stream.

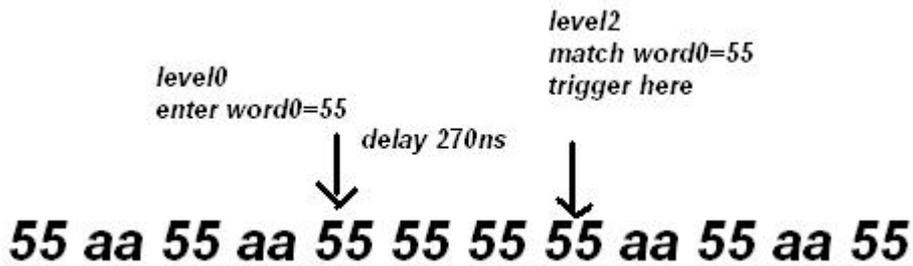
It has width pulse 55 55 55 55 in the following stream.

like as 55 aa 55 aa 55 55 55 55 aa 55 aa 55 aa 55.....

The screenshot shows the 'trigger' configuration window. At the top, there are four channel groups: CH31-24, CH23-16, CH15-8, and CH7-0. Below them are four data fields: 'XXXXXXXXXX', 'XXXXXXXXXX', 'XXXXXXXXXX', and '01010101'. A 'Word0' dropdown menu is set to 'Word0'. Below this is a table of trigger levels:

Level	IF	AND	Event	Enter	Word0	then next level	
Level 0	IF	AND	Event	Enter	Word0	1	then next level
Level 1	IF		Delay	10ns		27	then next level
Level 2	IF	AND	Event	Match	Word0	1	then next level
Level 3	IF	AND	Event	Enter	.	1	then next level
Level 4	IF	AND	Event	Enter	.	1	then next level
Level 5	IF	AND	Event	Enter	.	1	then next level
Level 6	IF	AND	Event	Enter	.	1	then next level
Level 7	IF	AND	Event	Enter	.	1	then next level

Below the table is the 'Trigger edit in serial' section. It has several radio button options: 'Width bit', 'Width bit with timing' (selected), 'Width bit by rising clock', 'Width bit by falling clock', '1 bit Data by rising clock', '1 bit Data by falling clock', and 'I2C'. There are also input fields for '>', '1ns', and '300'. Below that, it says 'Ch0 as data ,Ch1 as clock' and shows a list of values (0) with '55' in the first field and '8 Bit' in the dropdown. There are 'Clear trigger' and 'Go to level 0' buttons. At the bottom, there are checkboxes for 'Decimal' and 'Hex' (checked).



The same is true for detecting narrow pulse in width stream when set < nn time.

like 55 55 55 55 aa aa aa aa 55 55 55 55 aa aa aa aa **55 aa 55 aa** 55 55 55 55 aa aa aa aa 55 55 55 55

All LA-2132 can work for it because it need two trigger level only.

But need adjust properly time delay.

Width Bit By Rising (Falling) Clock

A serial of width bit stream synchronous with clock. channel 31 default as clock.

channel 0-30 as data.

Data flow 77,00,55 synchronous with ch31 clock rising edge as following diagram.

Word 3 set to 1xxxxxxxxx.....

It detect data 77 after ch31 clock rising edge else go to trigger level 0 to judge continuously.

it also can select LSB out first or MSB out first

for example a stream 001111, LSB out first mean data flow is 111100.

MSB out first mean data flow is 001111.

trigger

CH31-24 CH23-16 CH15-8 CH7-0

XXXXXXXX XXXXXXXX XXXXXXXX 01110111 Word0

Level 0	IF	AND	Event	Enter	Word3	1	then next level	.
Level 1	IF	AND	Event	Match	Word0	1	then next level	else go to level 0
Level 2	IF	AND	Event	Enter	Word3	1	then next level	.
Level 3	IF	AND	Event	Match	Word1	1	then next level	else go to level 0
Level 4	IF	AND	Event	Enter	Word3	1	then next level	.
Level 5	IF	AND	Event	Match	Word2	1	then next level	else go to level 0
Level 6	IF	AND	Event	Enter	.	1	then next level	.
Level 7	IF	AND	Event	Enter	.	1	then next level	.

Trigger edit in serial

Width bit
 Width bit by rising clock
 1 bit Data by rising clock
 I2C
 Width bit with timing
 Width bit by falling clock
 1 bit Data by falling clock

Ch31 As clock

0 ▲ 77 8 Bit ▼

00 8 Bit ▼

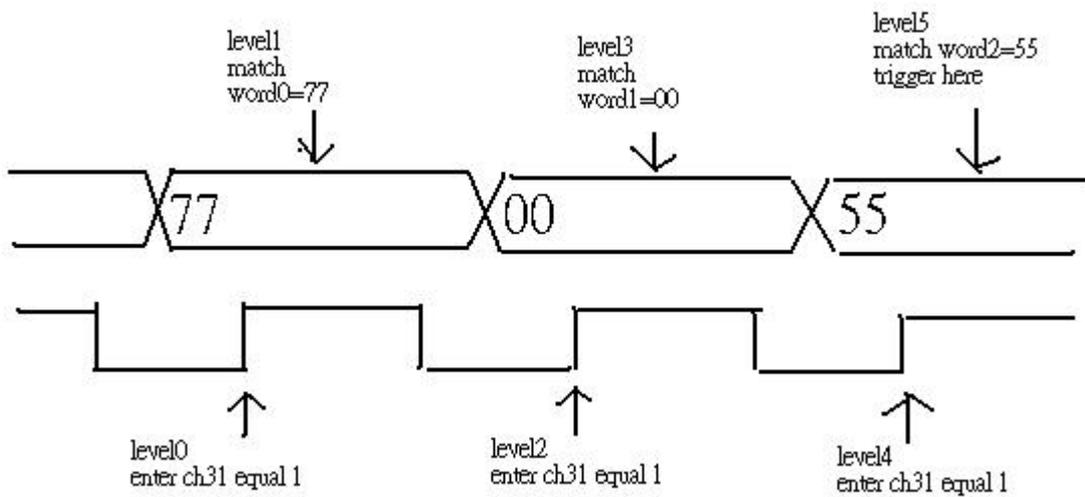
55 8 Bit ▼

8 Bit ▼

Decimal
 Hex

Clear trigger

Go to level 0



The same is true for falling clock.

The following model can work for it

LA-2132-K8 (8 Trigger levels), LA-2132-K512 (512 Trigger levels).

LA-2132-M8 (8 Trigger levels), LA-2132-M512 (512 Trigger levels).

LA-2132-G8 (8 Trigger levels), LA-2132-G512 (512 Trigger levels).

1 Bit Data By Rising Clock

A serial of bit stream synchronous with clock.

Channel 0 default as data, channel 1 default as clock.

It is same as "width bit by rising clock".

but it detect one bit only when clock is rising.

to avoid unnecessary start bit. leve0-2 let clock can work at first bit.

The screenshot shows a software interface titled "trigger" with a blue header. Below the header, there are four channel labels: CH31-24, CH23-16, CH15-8, and CH7-0. Each label has a corresponding display area showing "XXXXXXXX" and a "Word0" dropdown menu. Below these are eight trigger levels (Level 0 to Level 7) with various configuration options like "AND", "Event", "No Match", "Word1", "1", "then next level", and "else go to level 0".

Under the trigger levels, there is a section titled "Trigger edit in serial" with several radio button options:

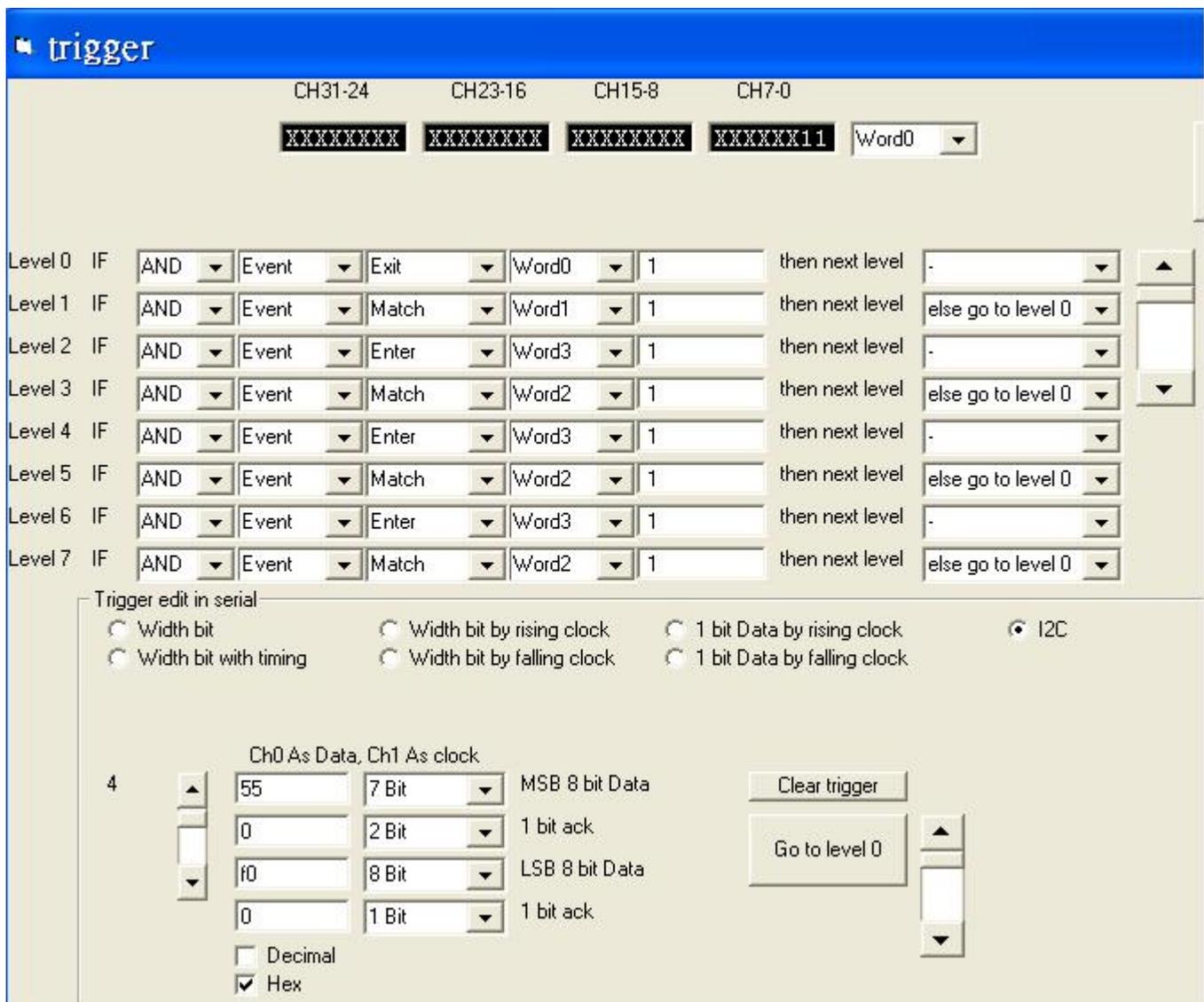
- Width bit
- Width bit by rising clock
- 1 bit Data by rising clock
- I2C
- Width bit with timing
- Width bit by falling clock
- 1 bit Data by falling clock

Below the radio buttons, there is a section titled "Ch0 As Data, Ch1 As clock" with a list of four items, each with a value of "33" and a dropdown menu set to "8 Bit". To the right of this list are two buttons: "Clear trigger" and "Go to level 0". At the bottom, there are checkboxes for "Decimal", "Hex", "LSB sensor first", and "MSB sensor first".

The same is true for falling clock.
 The following model can work for it
 LA-2132-K512 (512 Trigger levels).
 LA-2132-M512 (512 Trigger levels).
 LA-2132-G512 (512 Trigger levels).

I²C

It is same as "one bit by rising clock"
 a serial of bit stream synchronous with clock. channel 0 default as data,
 channel 1 default as clock in I²C format.
 Level 0 -1 is I²C start format.



I²C need 73 trigger levels to complete trigger.
That is why LA-2132 need design 512 trigger levels.
The following model can work for it
LA-2132-K512 (512 Trigger levels).
LA-2132-M512 (512 Trigger levels).
LA-2132-G512 (512 Trigger levels).

Threshold Voltage Setup

it can set threshold voltage at toolbar or parameter form.
The range of threshold voltage is from -3.7V to 1.9V in 35mV step.
In general, 5V TTL need set 1.4V.
ECL (-1.3V)
LVC1.5V (0.75V)
LVC1.8V (0.9V)
LVC2.5V (1.2V)
LVC3.3V (1.4V)
SSTL2|| 2.5V (1.25V)
SSTL3|| 3.3V (1.4V)
Adjust threshold voltage can remove unnecessary signal like noise sometime.
LA-2164 support two sets threshold voltage.

Clock Menu

Select an internal clock rate or an external clock for sampling.
It can set clock rate at toolbar or parameter form.
1 GHz (1 ns) when select 8 channel mode only.
500 MHz (2 ns) when select 8 channel or 16 channel mode only.
250 MHz (4 ns) below 250mhz can be used for all clock mode.
100 MHz (10 ns)
50 MHz (20 ns)
20 MHz (50 ns)
10 MHz (100 us)
5 MHz (200 us)
2 MHz (500 us)
1 MHz (1 us)
500 KHz (2 us)
200 KHz (5 us)
100 KHz (10 us)

50 KHz (20 us)
20 KHz (50 us)
10 KHz (100 us)
5 KHz (200 us)
2 KHz (500 us)
1 KHz (1 ms)
500 Hz (2 ms)
200 Hz (5 ms)
100 Hz (10 ms)
50 Hz (20 ms)
20 Hz (50 ms)
10 Hz (100 ms)
5 Hz (200 ms)
2 Hz (500 ms)
1 Hz (1 s)

LA-2164 can support all kind of clock rate as above except only support 1 GHz and 400 MHz
At 16 channels mode.

External Clock

4 kind of external clock can be selected.

Channel 31 external clock rising.

Channel 31 external clock falling .

Channel 31 both of external clock rising and falling. it let external clock frequency double.

LVDS0 is external clock in LVDS signal.

The software only transfers data to the PC when the buffer is full. If you are using a slow clock it might take a long time to fill the buffer. Recording time/Acquisition time/Capture time/Buffer Length.

The Logic analyzer will acquire data for time equal to Buffer length * clock rate.

Example:

If buffer length = 512K and sample rate = 100KHz. The LA will record for (512K * 10 us)

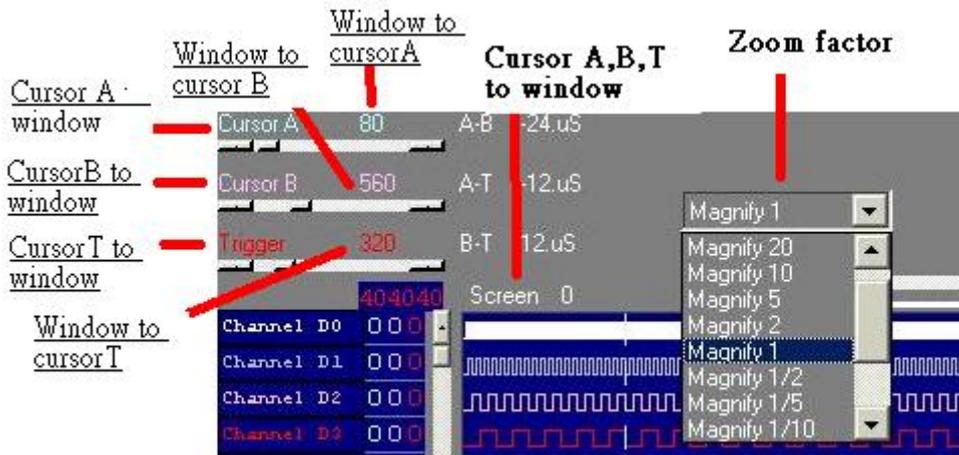
Magnify (Timing)

Select a zoom ratio for the timing window. You can display the timing data in a compressed or expanded format. Zooming in lets you see great detail. Zooming out lets you see large abundant of data.

Zoom can be changed in the following ways:

1. A clicking on the combo brings up a magnify factor list.
2. Select what you want.

Zoom Combo



In the timing window you can do the following:

Zoom

Zoom in or out by selecting zoom factor combo

- Window to cursor A : Zoom around cursor A
- Window to cursor B : Zoom around cursor B
- Window to cursor T : Zoom around cursor T (trigger cursor)
- cursor A to Window : shift cursor A to window
- cursor B to Window : shift cursor B to window
- cursor T to Window : shift cursor T to window
- cursor A, B, T to Window : shift cursor A, B, T to window

Timing Window

This window shows the data in a timing waveform style display. The channel names will be on the left edge with the data going horizontally. To the right of the channel names are the values of data at each cursor (it is color coded to match the cursors). The vertical scrollbar moves the window up and down to display more channels. The horizontal scrollbar moves the data forward and backward in time. The channel order can be changed by the color form. The size of the window can be changed by grabbing an edge of the window and dragging it.

When the Timing window is selected (title says "active window")

Left and right arrows scroll data with respect to time, or grabbing timing to shift data.

Up and down arrows scroll data with respect to channels.

Window to cursor A :	Zoom around cursor A
Window to cursor B :	Zoom around cursor B
Window to cursor T :	Zoom around cursor T (trigger cursor)
cursor A to Window :	shift cursor A to window
cursor B to Window :	shift cursor B to window
cursor T to Window :	shift cursor T to window
cursor A, B, T to Window :	shift cursor A, B, T to window

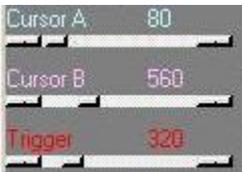
Note:

This only works on the selected window.

Click on the window to select it.

Cursor using

Cursors are used to mark points of interest in the data, to measure time between events and to define pre/post trigger position.

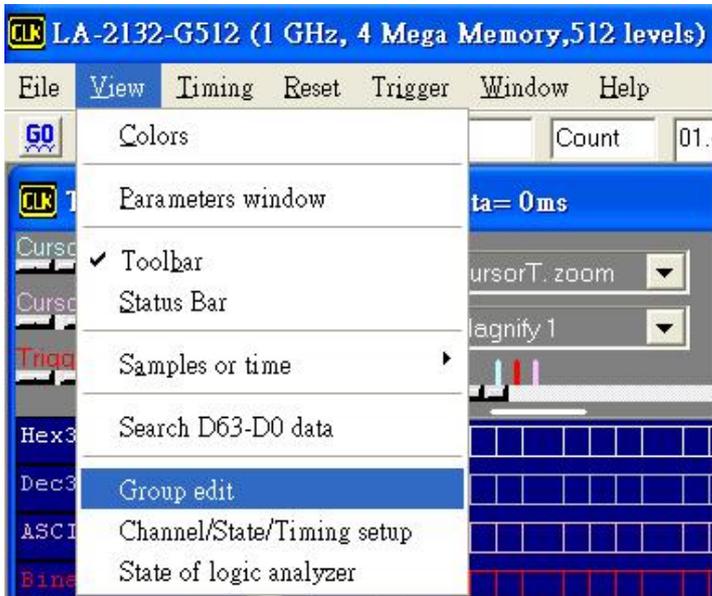


Moving a cursor:

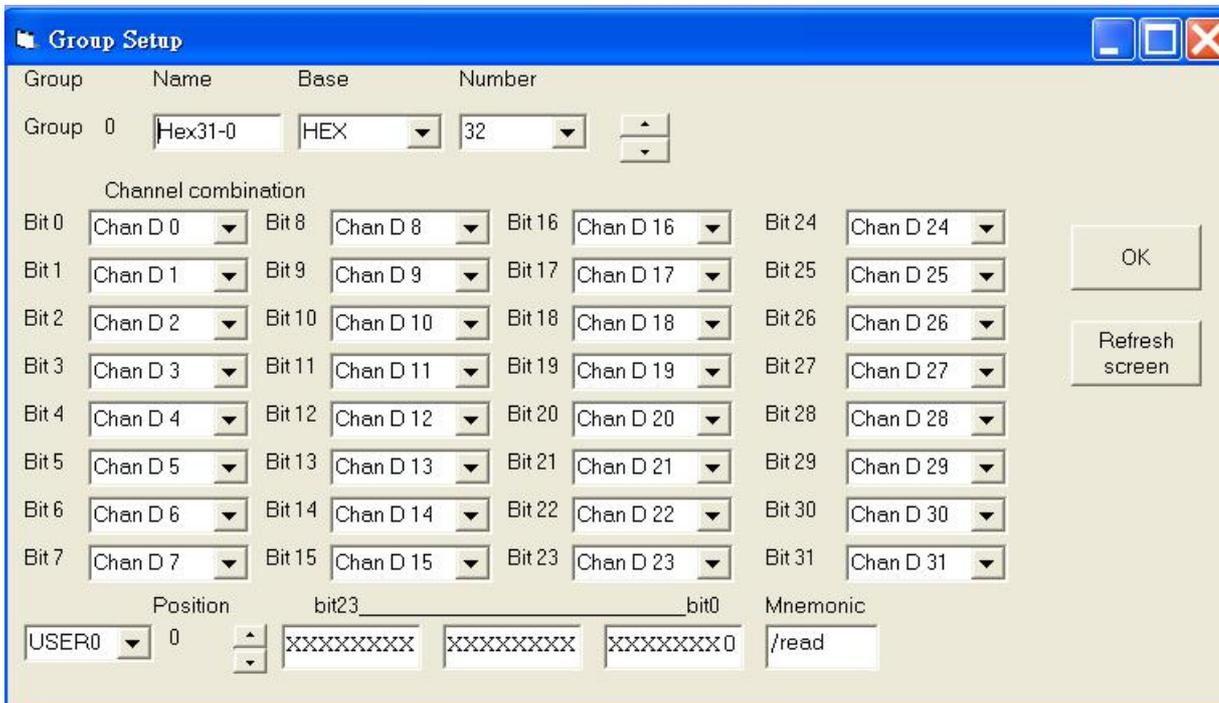
1. In the timing you can select a cursor by using the arrow buttons in the timing move it.
2. You can also "grab" the cursor by left clicking on it in the timing and then move it by "dragging" it to a new location.
3. The timing cursor A, B, T have selections that allow you to bring the cursors onto their views.

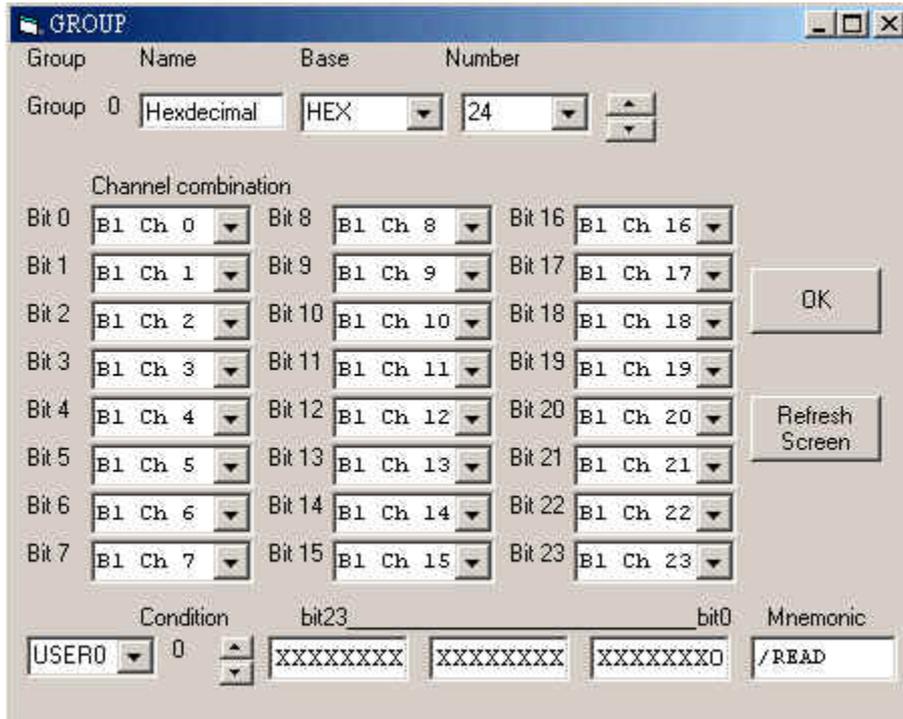
Setting Up Group

set following after select group edit.

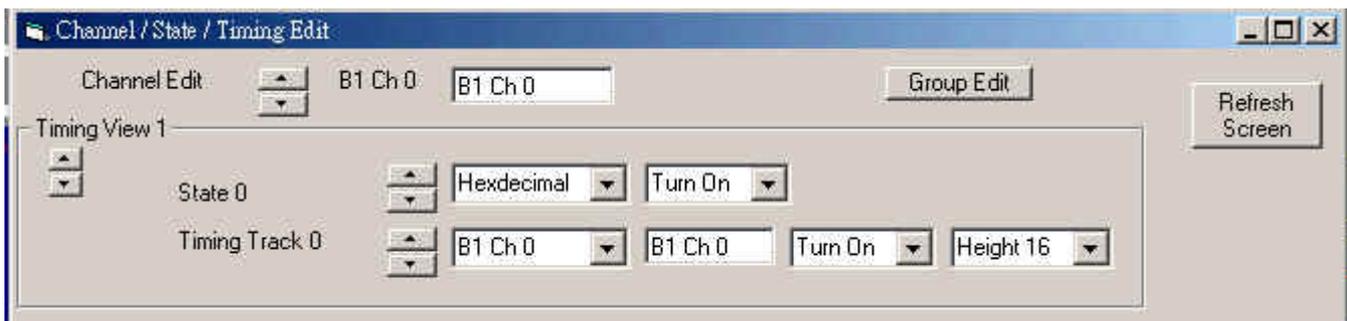
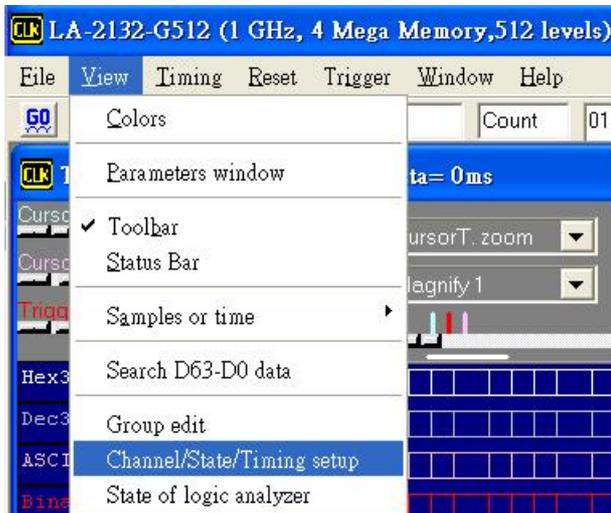


1. Select which group to display. Groups can be in different bases.
2. Set Base.
3. Set channel combination.





Setting Up The State/Timing Window



Setting up the state/timing display.

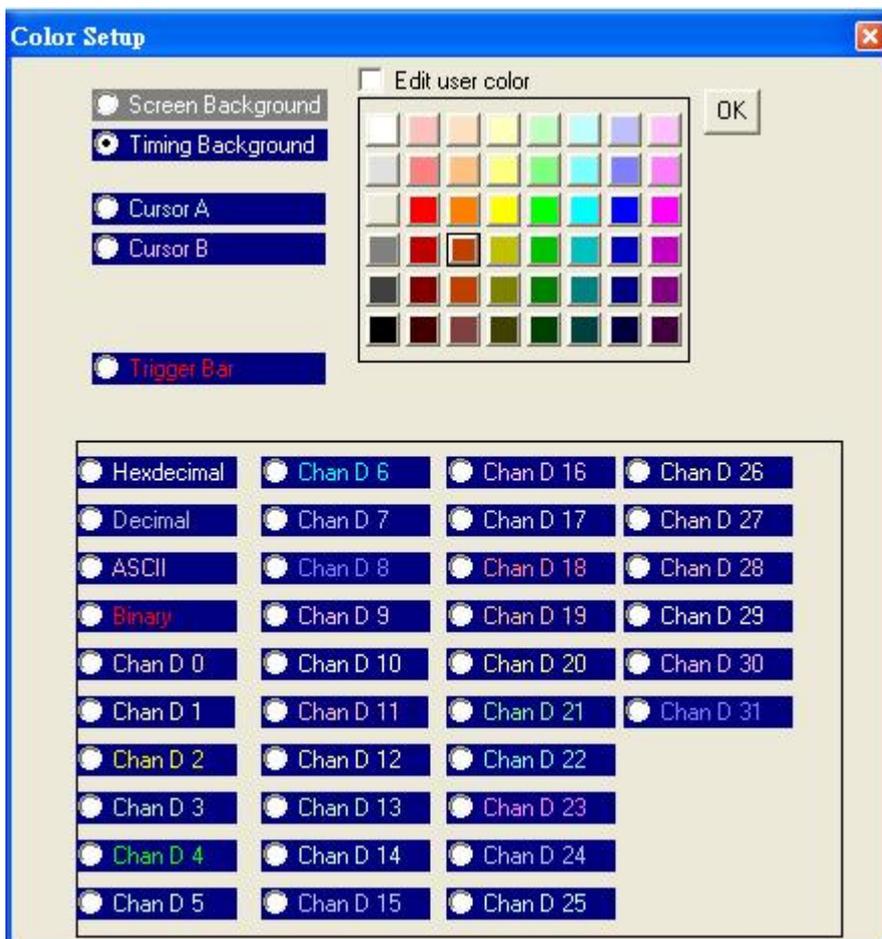
1. Set group.
2. Select which group to display. Groups can be in different bases.
3. Select display channel on or off. Timing display also can define timing height.

Setting Channel Names And Colors

Channel names can edit at timing window directly.

Channel names should be edited at color form.

Color form also can set all cursor color.

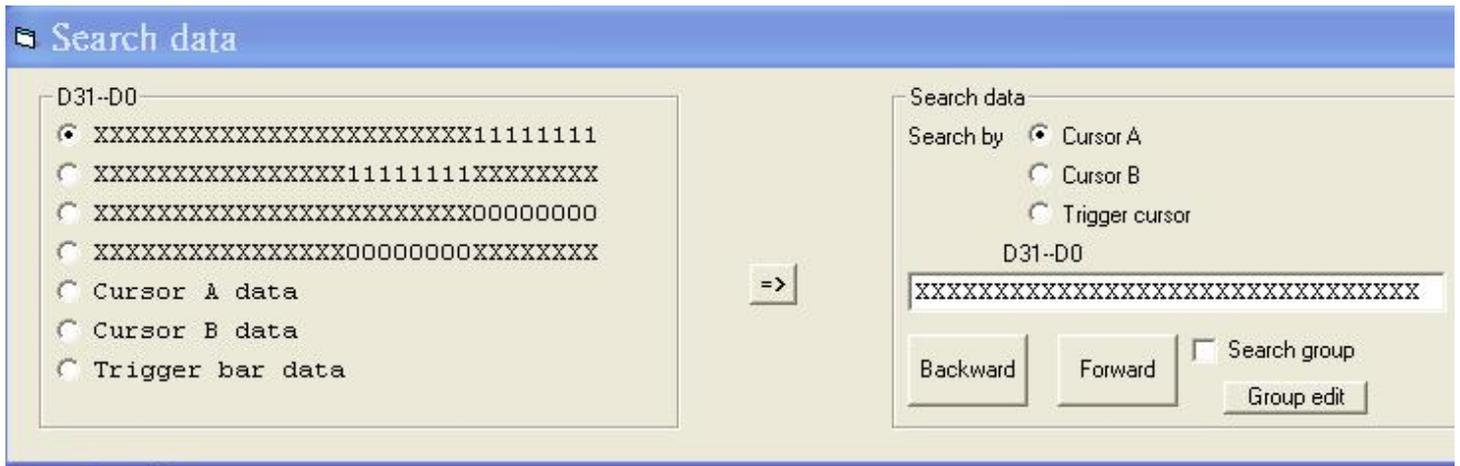


Search By Cursor

Select one of cursor A, B, T and specific word.

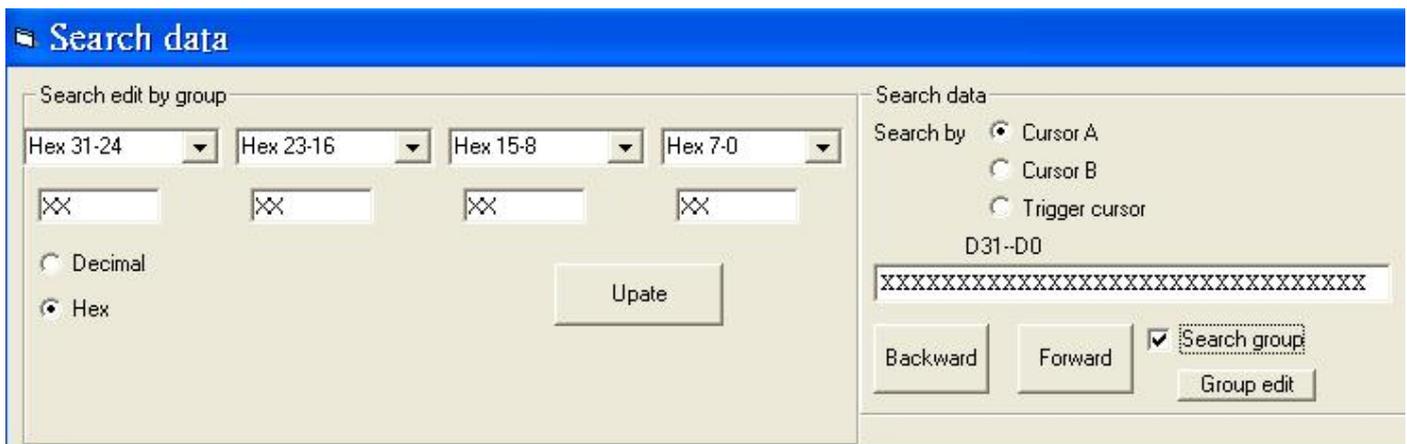
or edit search word directly.

It will search all memory and channel after Push forward or backward.



Search By Group

The same is true for search by group after selecting search group check item. It use group definition to quickly edit search word.



Export (File Menu)

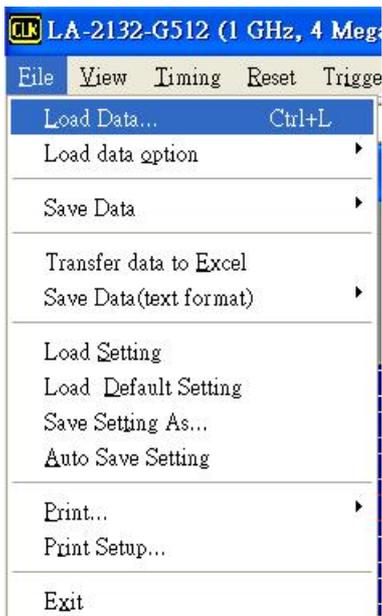
Use this to output data to other programs.



How to use:

- 1) Data: Select which data to output: Individual group or all channels
Select base to output data in.
- 2) Start and End: Select data address range.
- 3) Click OK to save data.

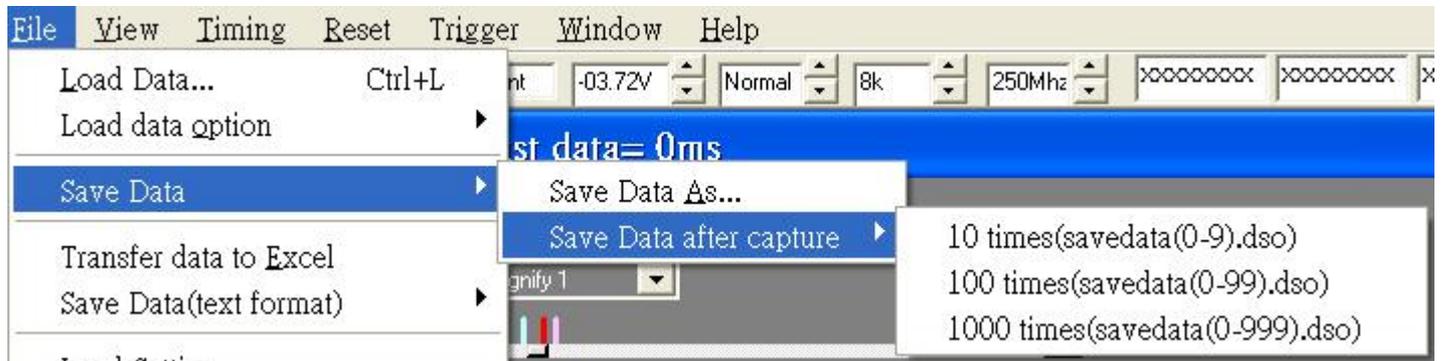
File Menu Commands



The File menu offers the following commands:
Load : Opens an existing file (data or settings).

Save : Save a file to a specified file name. Save settings or data files.

Save data after capture: it save to hard disk from 10-1000 times. if you need records mass data. but you need check your hard disk free capacity.



Export: Export data to excell programs format, or text format.

Auto save setting: If checked settings will be saved when you exit the program. then loaded when you load the program.

Print: Prints data in Timing format.

Print Setup: Selects a print mode, printer and printer connection.

Exit: Exit.

The following is source code of LA-2132 save and load data visual c program.

Sometime user want to analyze data by themselves. it is useful for user to understand how program write and read data.

Every binary code describe 1 channel. For example 00110001 data mean channel 0 is high, channel 1 is low...etc at first record.

```
_declspec (dllexport)void _stdcall vc_savedata (uchar *buflogic0, int length, LPSTR sfile,uchar *model,unsigned char *LAPorts8)
{
int result,ii,ll;
FILE *fp;
fp = fopen ( sfile, "w+b" );
if (model[0]== clk2132_1m){
ll=1025;
}
if (model[0]== clk2132){
ll=513;
}
if (model[0]== clk2132_256K){
ll=257;
```

```

}
if (LAPorts8[channelmode]==0){
for(ii=0;ii<3;ii++) {
result = fwrite ( &buflogic0[1024*ii], length, 1, fp );
}
}
if (LAPorts8[channelmode]==1){
for (ii=0;ii<1;ii++) {
result = fwrite ( &buflogic0[1024*ii*2], length, 1, fp );
}
}
if (LAPorts8[channelmode]==2){
result = fwrite ( &buflogic0[0], length, 1, fp );
}
fclose ( fp );
}
_declspec (dllexport) void _stdcall vc_loaddata (uchar *buflogic0, int length ,LPSTR sfile,int position)
{
int result;
FILE *fp;
fp = fopen ( sfile, "r+b" );
result = fseek (fp, length*position,0);
result = fread ( &buflogic0[0], length, 1, fp );
fclose ( fp );
}

```

Hardware Specifications

There are two Models is available for LA-2132 LVDS:

LA-2132 LVDS: (32 channels only, can't expand to 64 channels).

- K2 (250MHz, 256K Memory, 2 Trigger Levels, support LVDS).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels, support LVDS).

There are nine Models is available for LA-2132 Series:

LA-2132K Series: (Expand to 64 channels is available, without support LVDS).

- K2 (250MHz, 256K Memory, 2 Trigger Levels).
- K8 (250MHz, 256K Memory, 8 Trigger Levels).
- K512 (250MHz, 256K Memory, 512 Trigger Levels).

LA-2132G Series: (Expand to 64 channels is available, without support LVDS).

- M2 (500MHz, 1Mega Memory, 2 Trigger Levels).
- M8 (500MHz, 1Mega Memory, 8 Trigger Levels).
- M512 (500MHz, 1Mega Memory, 512 Trigger Levels).

LA-2132G Series: (Expand to 64 channels is available, without support LVDS).

- G2 (1GHz, 4Mega Memory, 2 Trigger Levels).
- G8 (1GHz, 4Mega Memory, 8 Trigger Levels).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels).

Expand to 64 Channels Is Available

When use 20 pin flat cable connect two LA-2132 Series, it can expand to 64 channels.
Please see page 6 (Expand to 64 channels) diagram.

LA-2132 LVDS Series Hardware Specifications

Model	LA-2132 LVDS (K2) 250MHz, 256K Memory	LA-2132 LVDS (G512) 1GHz, 4Mb Memory
Internal Sampling Rate Number of Channel Record Length	32 channels from 1Sa/s to 250MSa/s 256 K memory	32 channels from 1Sa/s to 250MSa/s 1 Mega memory
		16 channels from 1Sa/s to 500MSa/s 2 Mega memory
		8 channels from 1Sa/s to 1 GSa/s 4 Mega memory
	2 channels bi-direction LVDS 2 channels input LVDS Expand to 64 Channels is not available	2 channels bi-direction LVDS 2 channels input LVDS Expand to 64 Channels is not available
External Clock Rate	Up to 125 MSa/s, DC to 200 MHz for LVDS	
I/O Bandwidth	CH 0 ~ 31 DC to 125 MHz, DC to 200 MHz for LVDS	
Input Impedance	200 K Ω // 2pf (Tip to ground)	
Input Voltage	Max. -110 V to +110 V for CH 0 ~ 31 0 to 5V only for all LVDS signals (it will burn out if input voltage is exceed this range)	
Threshold Voltage	-2V to 1.9V by 25mV step ECL (-1.3V) LVC1.5V (0.75V) LVC1.8V (0.9V) LVC2.5V (1.2V) LVC3.3V (1.4V) SSTL2 2.5V (1.25V) SSTL3 3.3V (1.4V)	
Channel Skew	Typical < 200 ps	
Trigger position	Any position for user defined	
Max. Trigger Speed	250 MHz (4ns)	
Trigger Quality	0, 1, x (don't care) settings for all Digital channels, 2, 8, 512 Trigger Levels	
Power Supply	No External Power Source Require	
Net Weight	120 Grams	
Size (Dimension)	107mm x 77mm x 16mm	
Accessories	Harness Color Wires 32 Pin x 2 pcs. USB 2.0 Two Head Cable. Easy Hook 50 pcs, Software CD, User's Manual.	

LA-2132 Series Hardware Specifications

Model	LA-2132 K Series 250MHz, 256K Memory	LA-2132 M Series 500MHz, 1Mb Memory	LA-2132 G Series 1GHz, 4Mb Memory
Internal Sampling Rate	32 channels from 1Sa/s to 250MSa/s 256 K memory	32 channels from 1Sa/s to 250MSa/s 512 K memory	32 channels from 1Sa/s to 250MSa/s 1 Mega memory
Number of Channel		16 channels from 1Sa/s to 500MSa/s 1 Mega memory	16 channels from 1Sa/s to 500MSa/s 2 Mega memory
Record Length			8 channels from 1Sa/s to 1 GSa/s 4 Mega memory
	Not support LVDS Two LA-2132 connect by a 20Pin flat cable, it can be expand to 64 channels.	Not support LVDS Two LA-2132 connect by a 20Pin flat cable, it can be expand to 64 channels.	Not support LVDS Two LA-2132 connect by a 20Pin flat cable, it can be expand to 64 channels.
External Clock Rate	Up to 125 MSa/s		
I/O Bandwidth	CH 0 ~ 31 DC to 125 MHz		
Input Impedance	200 Kohm // 2pf (Tip to ground)		
Input Voltage	Max. -110 V to +110 V for CH 0-31		
Threshold Voltage	-2V to 1.9V by 25mV step ECL (-1.3V) LVC1.5V (0.75V) LVC1.8V (0.9V) LVC2.5V (1.2V) LVC3.3V (1.4V) SSTL2 2.5V (1.25V) SSTL3 3.3V (1.4V)		
Channel Skew	Typical < 200 ps		
Trigger position	Any position for user defined		
Max. Trigger Speed	250 MHz (4ns)		
Trigger Quality	0, 1, x (don't care) settings for all Digital channels, 2, 8, 512 Trigger Levels		
Power Supply	No External Power Source Require		
Net Weight	120 Grams		
Size (Dimension)	107mm x 77mm x 16mm		
Accessories	Harness Color Wires 32 Pin x 2 pcs. USB 2.0 Two Head Cable. Easy Hook 50 pcs, Software CD, User's Manual.		

LA-2164 Series Hardware Specifications

Model	LA-2164 K Series 250MHz, 256KMemory	LA-2164 M Series 500MHz, 1Mb Memory	LA-2164 G Series 1GHz, 4Mb Memory
Internal Sampling Rate Number of Channels Record Length	64 channels from 1Sa/s to 250MSa/s 256 K memory	64 channels from 1Sa/s to 250MSa/s 512 K memory	64 channels from 1Sa/s to 250MSa/s 1 Mega memory
		32 channels from 1Sa/s to 500MSa/s 1 Mega memory	32 channels from 1Sa/s to 500MSa/s 2 Mega memory
			16 channels from 1Sa/s to 1 GSa/s 4 Mega memory
	Not Support LVDS	Not Support LVDS	Not Support LVDS
External Clock Rate	Up to 125MSa/s		
I/O Bandwidth	CH 0 ~ 63 DC to 125MHz		
Input Impedance	250Kohm // 2pf (Tip to ground)		
Input Voltage	Max. -110 V to +110 V for CH 0 ~ 63		
Threshold Voltage	-2V to 1.9V by 35mV step ECL (-1.3V) LVC1.5V (0.75V) LVC1.8V (0.9V) LVC2.5V (1.2V) LVC3.3V (1.4V) SSTL2 2.5V (1.25V) SSTL3 3.3V (1.4V)		
Channel Skew	Typical < 200ps		
Trigger position	Any position for user defined		
Max. Trigger Speed	250MHz (4ns)		
Trigger Quality	0, 1, x (don't care) settings for all Digital channels 2, 8, 512 Trigger Levels		
Power Supply	No External Power Source Require		
Net Weight	120 Grams		
Size (Dimension)	107mm x 77mm x 16mm		
Accessories	Harness Color Wires 32 Pin x 4 pcs. USB 2.0 Two Head Cable. Easy Hook 100 pcs, Software CD, User's Manual, 20 Pin Flat Cable 1 pcs.		

Window USB Driver Install

Windows 98/ME USB driver install

When USB2.0 control interface be connected to computer, screen will display



Click Next to continue



Edit or browse path to ...\\USB20driver\\win98_ME\\gene.inf
(here D: is CD location, dso25216A may be dso29xx or la5000b or la2124a)

Click Next to continue



Click Next to continue



Completing install

Windows 2000 USB driver install

When USB2.0 control interface be connected to computer, screen will display



Click Next to continue



Click Next to continue



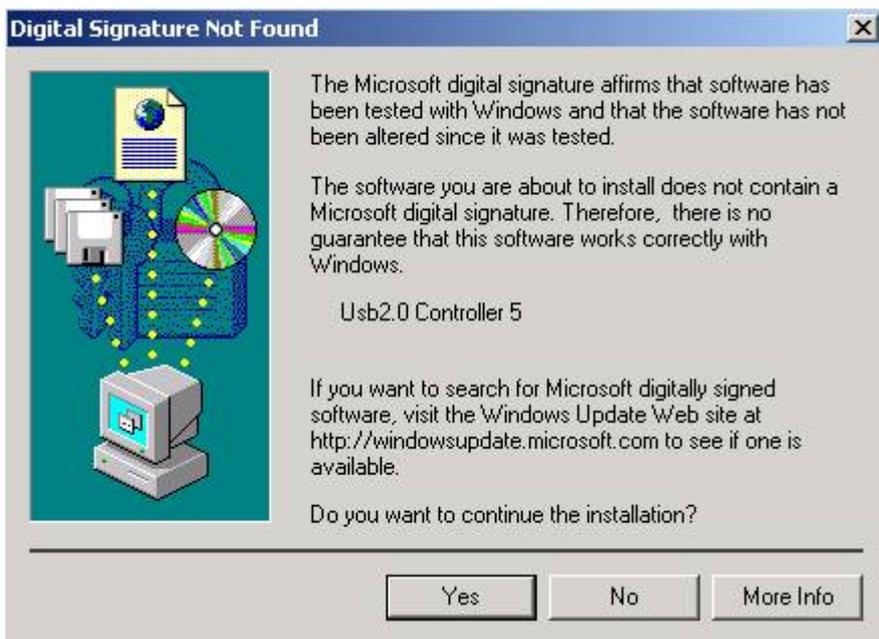
Click Next to continue



Edit or browse path to ...\USB20driver\win2000_XP\gene.inf
(here F: is CD location, dso25216A may be dso29xx or la5000b or la2124a)
Press OK



Click Next to continue



Click Yes to continue



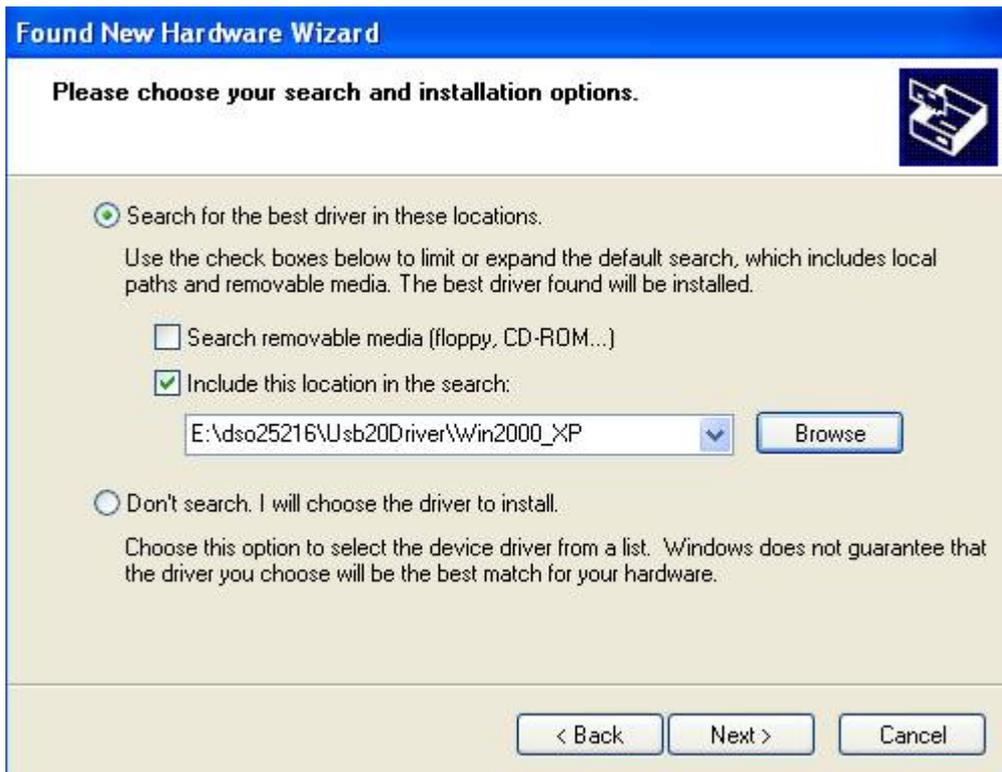
Completing install

Windows XP USB driver install

When USB2.0 control interface be connected to computer, screen will display



Click Next to continue



Edit or browse path to ...\USB20driver\win2000_XP\gene.inf
(here E: is CD location, dso25216A may be dso29xx or la5000b or la2124a)
Click Next to continue



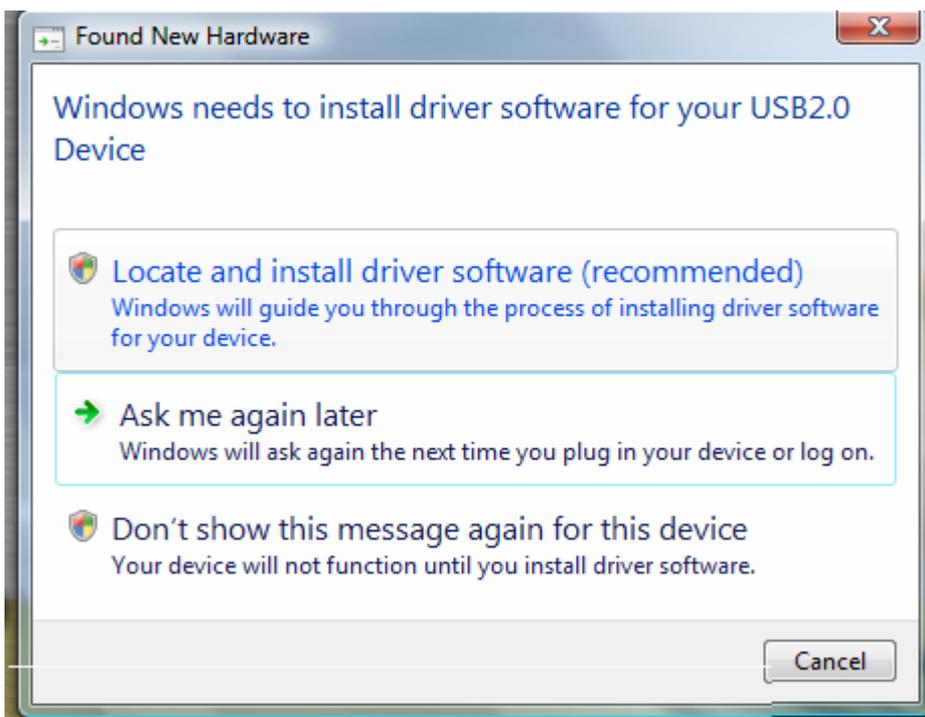
Press Continue Anyway



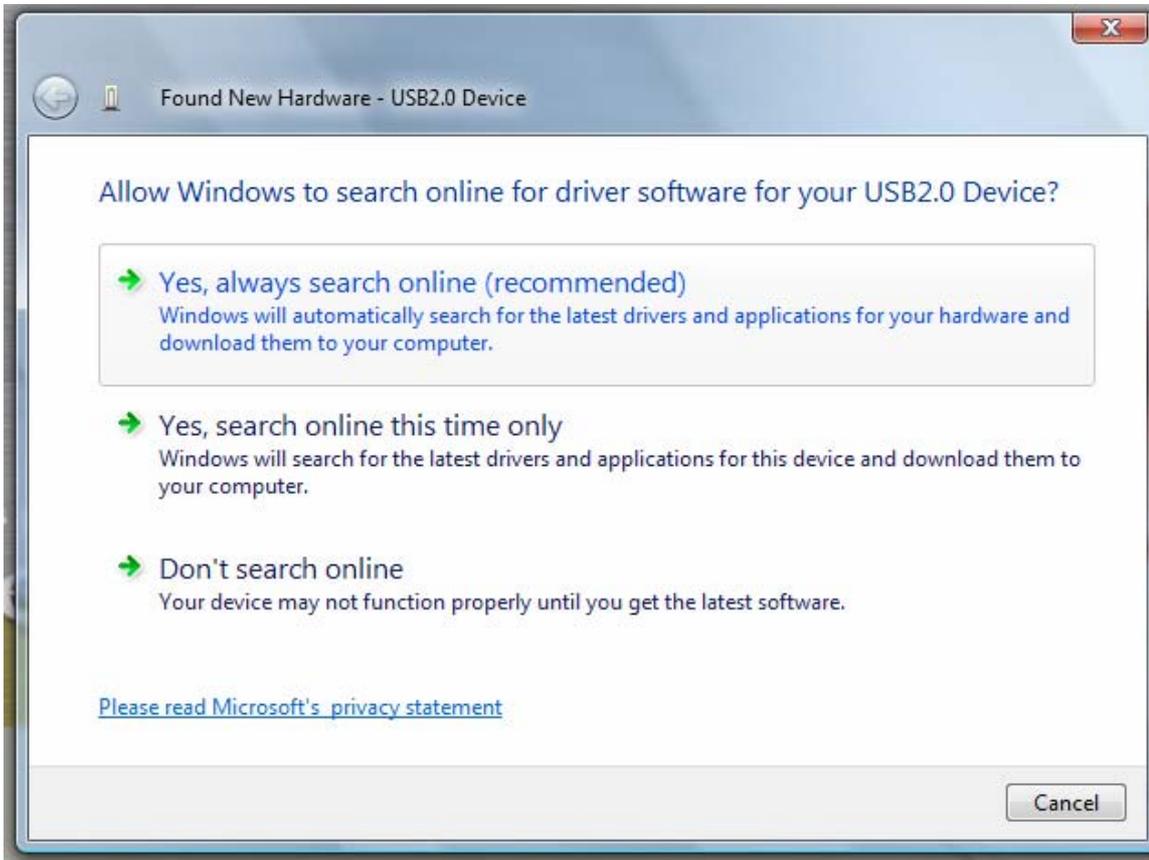
Completing install

Windows Vista USB driver install

When USB2.0 control interface be connected to computer, screen will display as following:



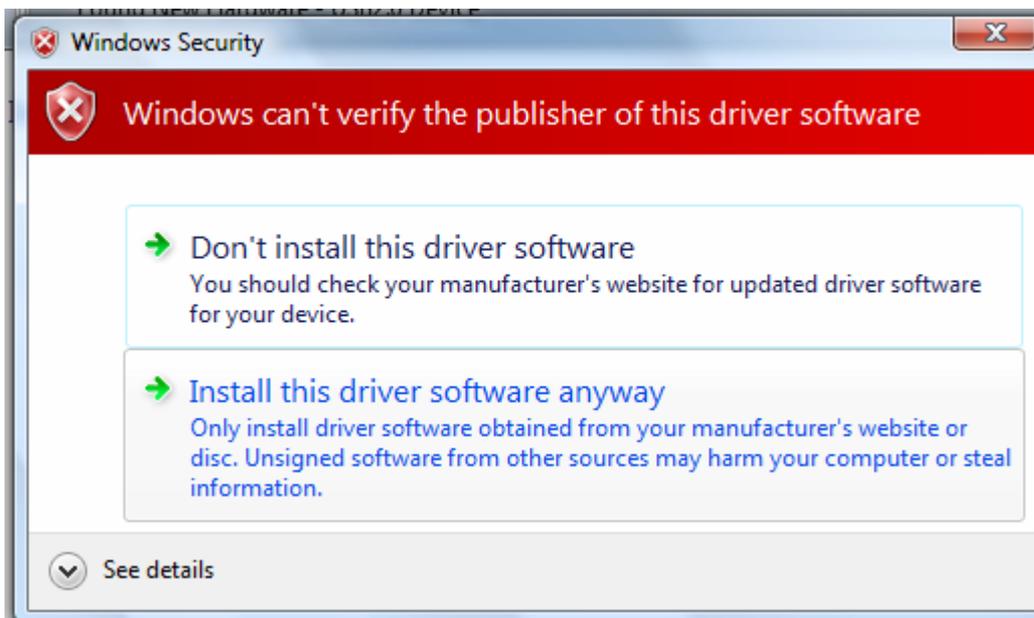
Press **Locate and install driver software (recommended)** Continue Anyway



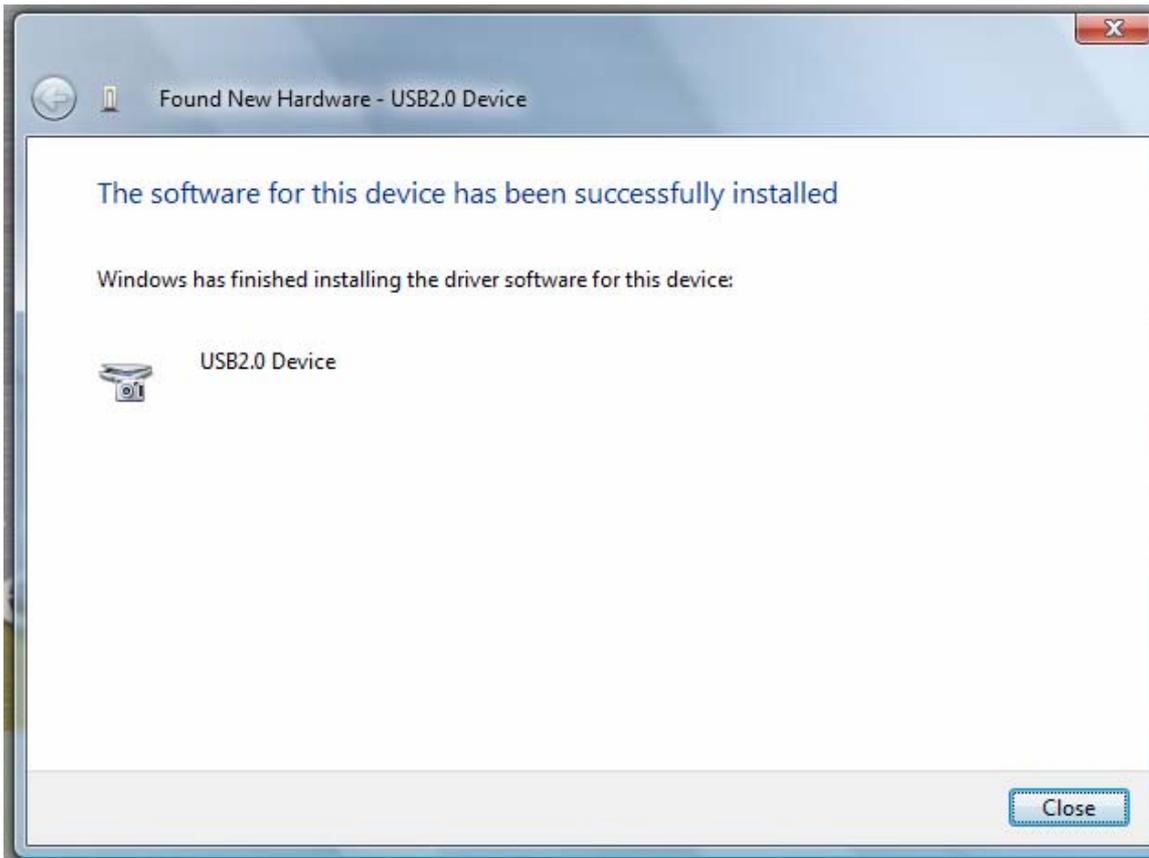
Press Continue Anyway



Press **Insert the disc that came with your USB2.0 Device**
Click Next to continue



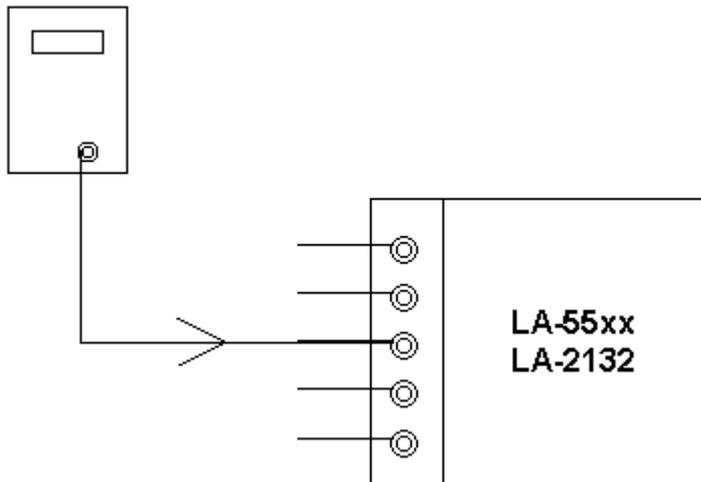
Press **Install this driver software anyway** to Continue



Completing install

Threshold Voltage Calibration

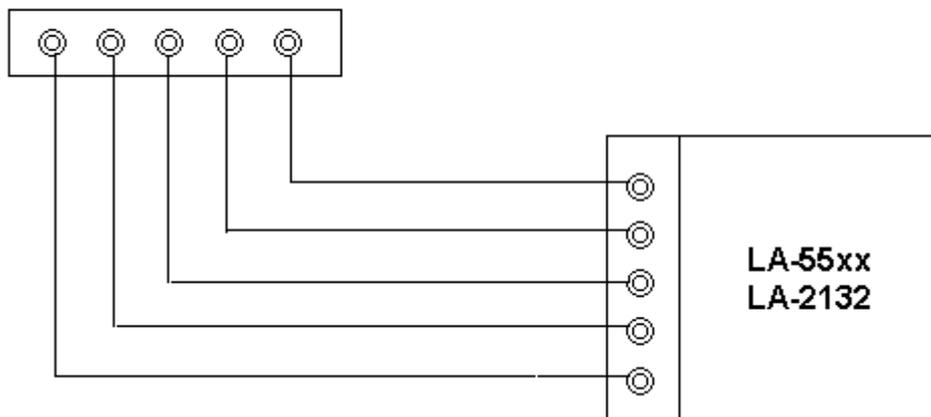
Signal Generator



Let signal generator output a square wave from -5V to 5V.
Set threshold from -4.8 to 4.8V, it should get square waveform.
Set threshold to 5.2V, it should get low signal.
Set threshold to -4.8V, it should get high signal.

Trigger Word and Position Calibration

LA-55160 Pattern Generator PG-32400

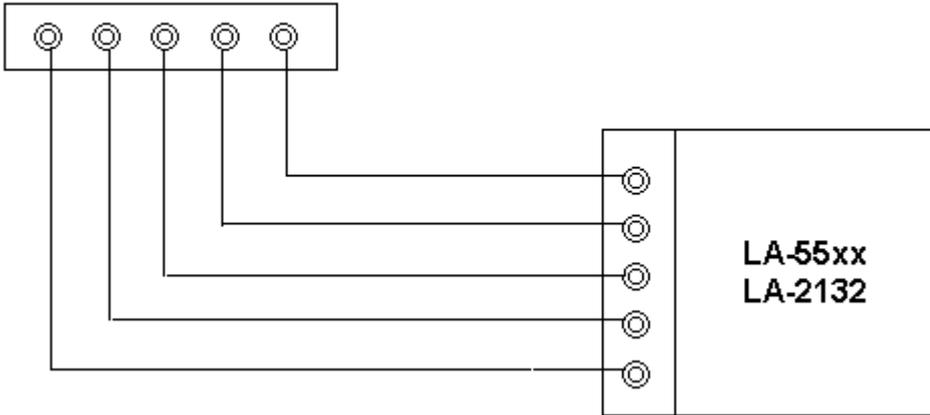


LA-55xx use software let trigger position always lock in 100% accuracy position, even you zoom in the waveform, still lock in 100 % accuracy position.
Use LA-55160 arbitrary pattern generator to output some specific word like 01010101
00001111 10001101 11111111 00000000... etc.
then set trigger word. it should get trigger word at proper position.

it should test more than ten sets trigger word.

Trigger Sequential Calibration

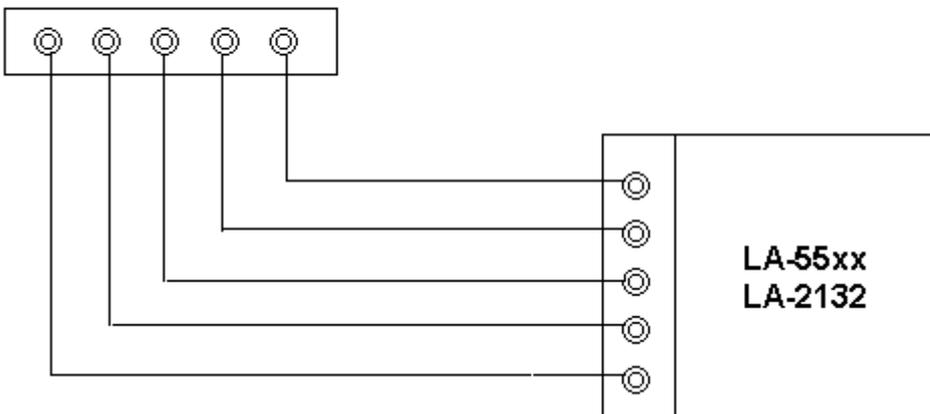
LA-55160 Pattern Generator
PG-32400



Use LA-55160 arbitrary pattern generator to output some specific word like 01010101
00001111 10001101 11111111 00000000... etc.
then set trigger word from 1 to 15 sequential. it should get trigger word at proper position.
it should test more than ten sets trigger word.

Clock Source Calibration

LA-55160 Pattern Generator
PG-32400



It has two clock source, one is internal clock, another is external clock .
Use LA-55160 arbitrary pattern generator to output some 1/2 1/4 ... etc pattern .
the LA-55160 output sample rate is 1 to 100 MHz, for 1/2 pattern, it can get 1/2 Hz to 50

MHz square wave form. then set logic analyzer internal clock to proper sample rate to get data, measure the data frequency should be 1/2 to 50 MHz. the same is true for external clock.

Technical Support

Technical Support can be reached at



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Software Updates

Software can be downloaded from our website.

Web: www.clock-link.com.tw

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