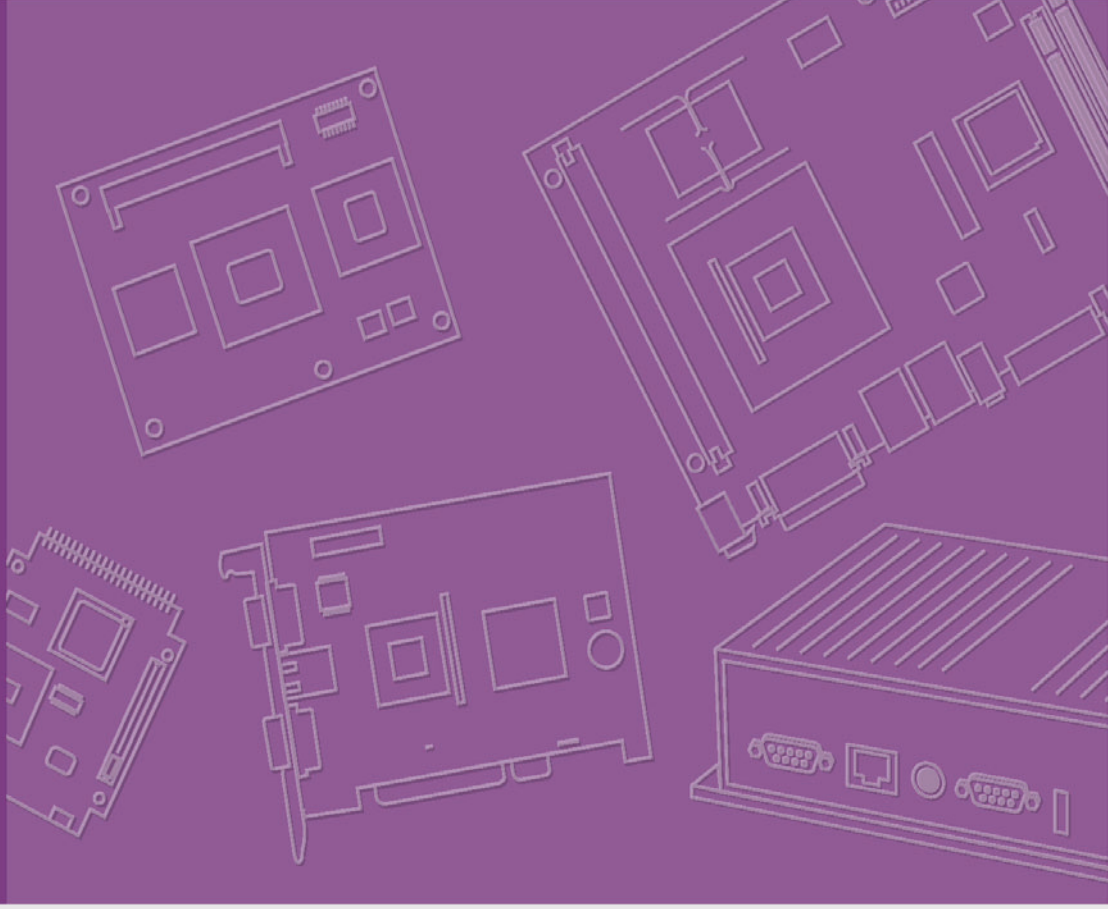

User Manual

EVA-X4150

System Design Guide

Trusted ePlatform Services

ADVANTECH

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Part No. 2006X41520 Edition 1

Printed in Taiwan August 2008

Contents

Chapter 1

Overview

1.1 Overview

The EVA-X4150 is a fully static 32-bit x86-based processor that is compatible with a wide-range of PC peripherals, applications and operating systems, such as DOS, WinCE, Linux, and most popular 32-bit RTOSs (Real Time OS). It enables maximum software re-use based on its feature of legacy compatibility. The EVA-X4150 integrates 16 KB write-through direct map L1 cache, a PCI bus interface at 33 MHz, an 8/16-bit ISA bus interface, SDRAM, a ROM controller, IPC (Internal Peripheral Controllers) with DMA and interrupt timer/counter included, FIFO UART, I2C, SPI (Serial Peripheral Interface), LPC (Low Pin Count), a USB 1.1/2.0 host controller, an Ethernet MAC, and an IDE controller within a single 456-pin BGA package to form an SoC (System-on-Chip) processor. The EVA-X4150 integrates comprehensive features and rich I/O flexibility within a single System-on-Chip, to reduce board design complexity and shorten product development schedules. Taking advantage of ultra low power consumption, the EVA-X4150 is able to operate in a wide range of temperatures without additional thermal design. With the commitment of long term supply guaranteed for the EVA-X4150, customers can extend product life cycle and receive a maximum return on investment. Implement the perfect x86-based SoC for diverse embedded applications with the EVA-X4150.

The EVA-X4150 provides an ideal solution for embedded system and communication products producing optimal performance.

This system design guide provides detailed usage information of the highly integrated EVA-X4150 SoC processor.

Chapter 2

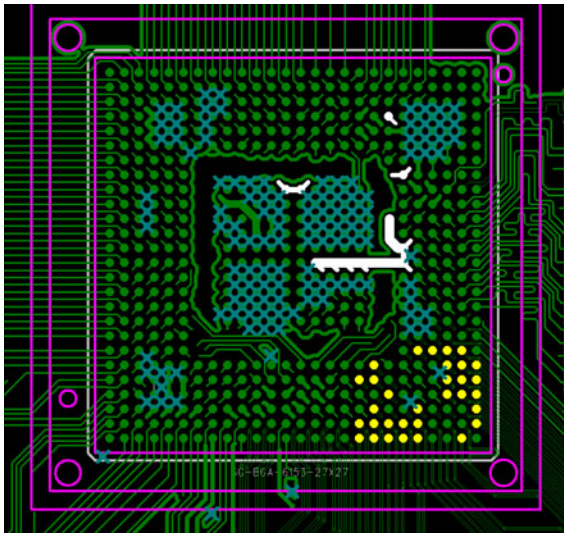
Layout Guide

2.1 BGA Layout Guideline

The EVA-X4150 package is a 456-ball PBGA. The ball diameter is 0.6 mm (24 mil), ball pitch is 1 mm (40 mil). There are 5 rows of balls arranged along the edge of the package.

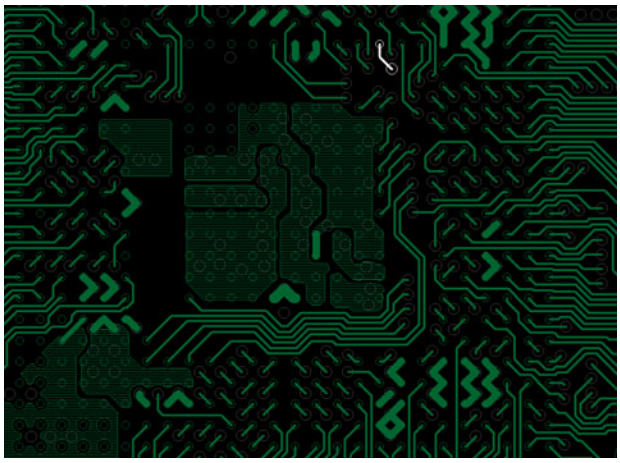
For 6-layer:

- **Ball pad diameter: 24 mil**
- **Traces width/ spacing for Signals: 5.5/ 5** mil
- **Trace width for Power and Ground: 20** mils
- **Vias PAD/ Drill diameter for all Signals: 14/ 8** mil
- **Via**-to-via spacing (center to center): **40** mil
- **Via**-to-pad spacing (center to center): **30** mil



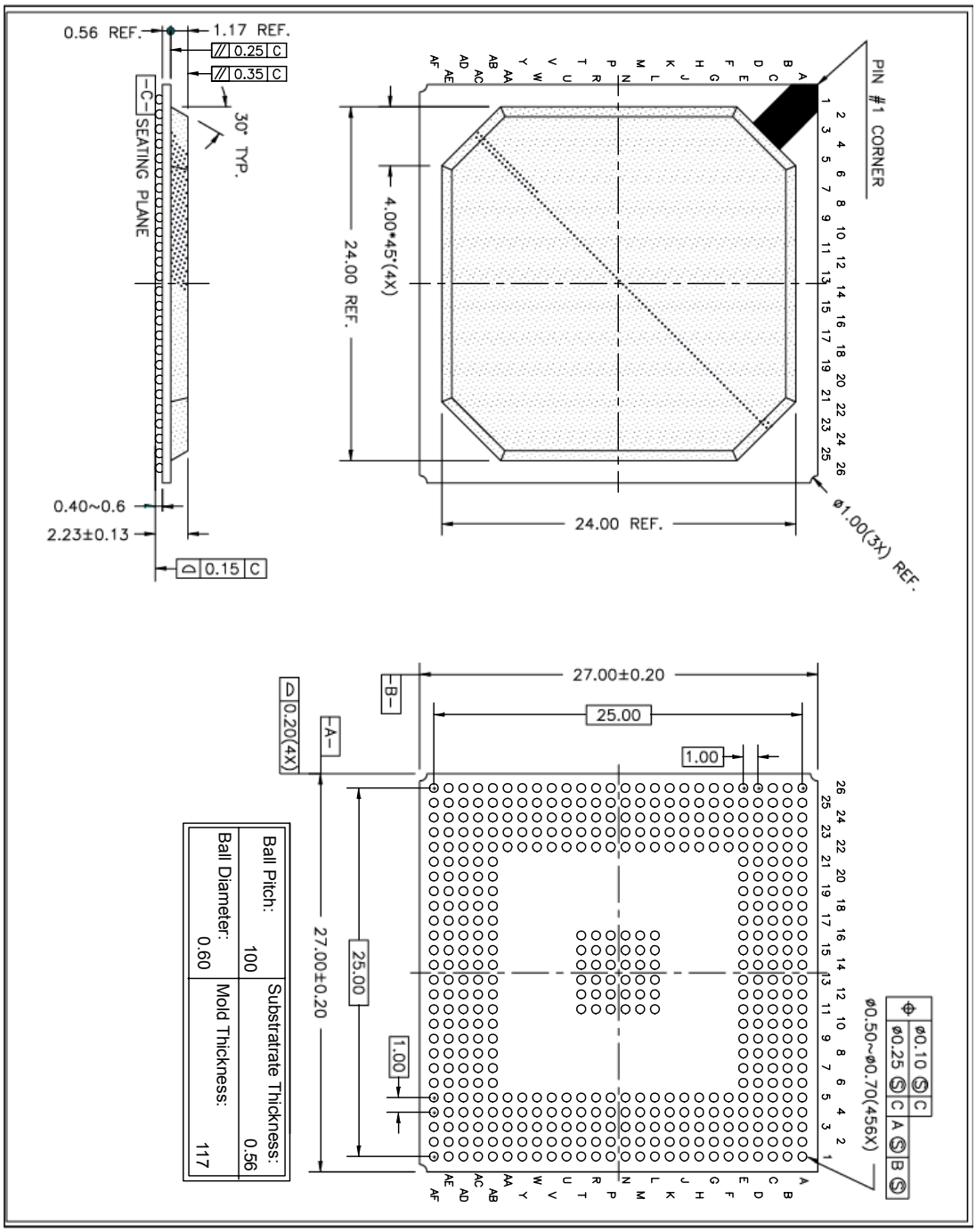
For 4-layer:

- **Ball pad diameter: 14 mil**
- **Traces width/ spacing for Signals: 5/ 5** mil
- **Trace width for Power and Ground: 20** mils
- **Vias PAD/ Drill diameter for all Signals: 22 / 12** mil
- **Via**-to-via spacing (center to center): **40** mil
- **Via**-to-pad spacing (center to center): **30** mil



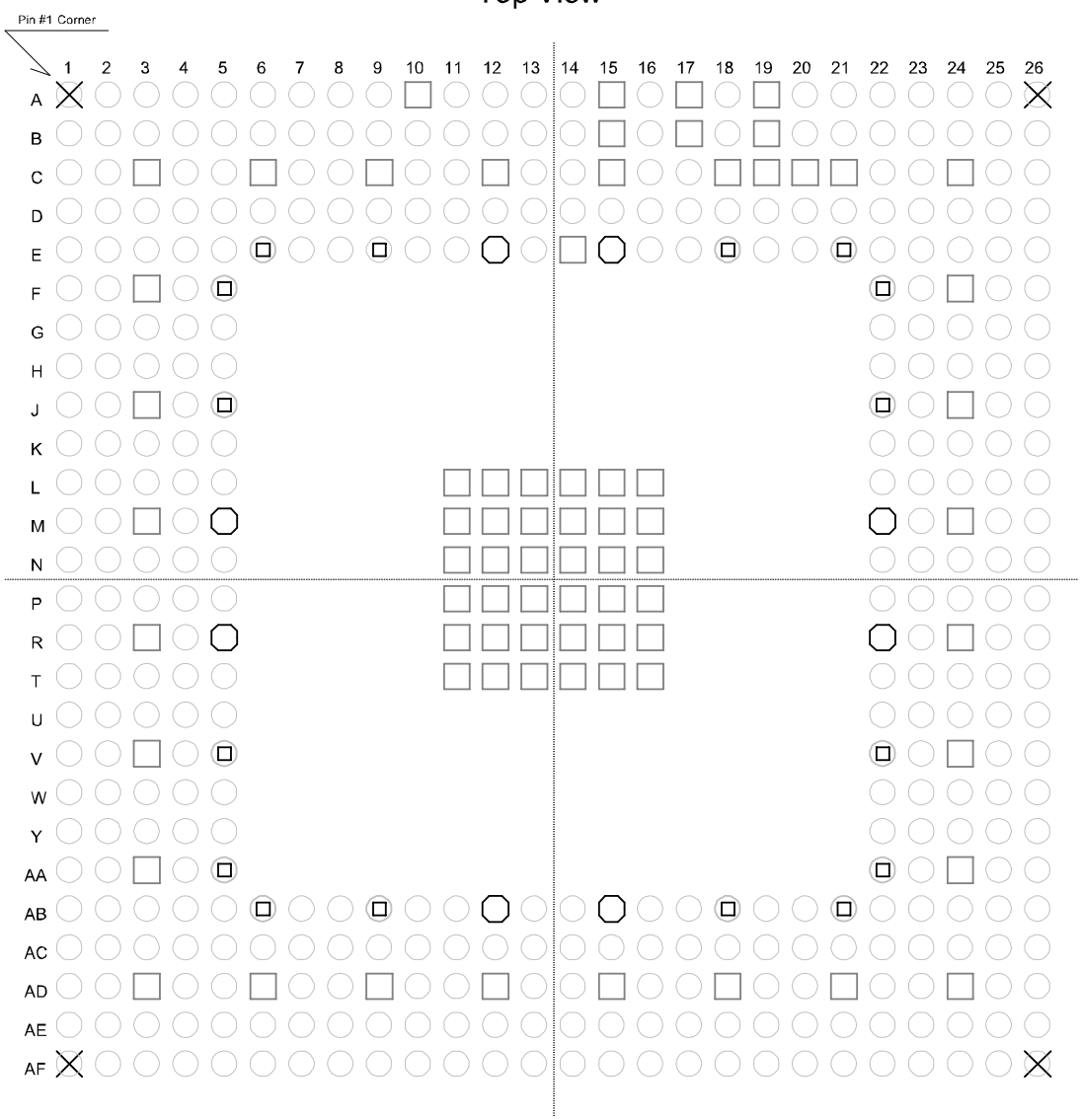
Note! *All the Vias must be covered by solder mask. To minimize inductance, power vias should be as large as possible and take good care of the inadvertently cut of the ground and power planes.*

2.2 Package Outline



2.3 Signal Arrangement

Top View



GND :A10,A15,A17,A19,B15,B17,B19,C3,C6,C9,C12,C15,C18,C19,C20,C21,C24,F3,F24,J3,J24,L11~L16,M3,M11~M16,M24
N11~N16,P11~P16,R3,R11~R16,R24,T11~T16,V3,V24,AA3,AA24,AD3,AD6,AD9,AD12,AD15,AD18,AD21,AD24,E14

1.8V Power: E12,E15,M5,M22,R5,R22,AB12,AB15

3.3V Power: E6,E9,E18,E21,F5,F22,J5,J22,V5,V22,AA5,AA22,AB6,AB9,AB18,AB21

N.C. Pin : A1,A26,AF1,AF26

Signal Pin :

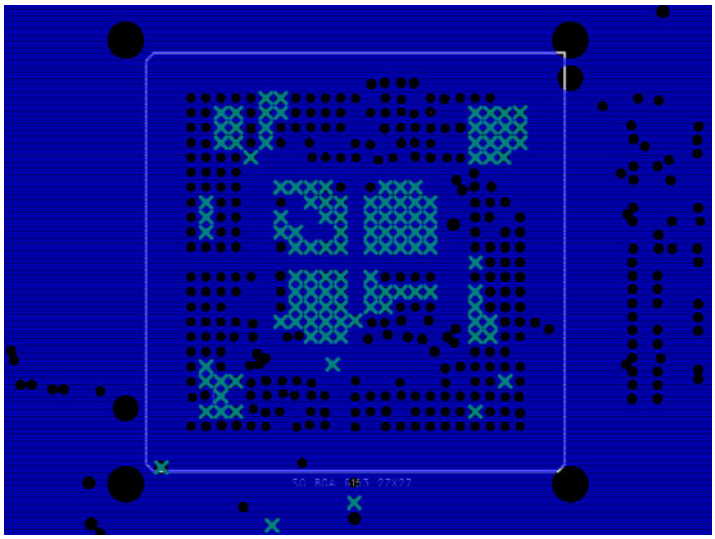
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	TDO	TMS	SDA	GPIO_PORT0[4]	GPIO_PORT0[0]	LAD[3]	LAD[0]	CLK24MOUT	GND	Vss33_PLL	XIN_14318	Vss18_PLL
B	INTC_	TDI	TCK	SCL	GPIO_PORT0[5]	GPIO_PORT0[1]	LFRAME_	LAD[1]	RTC_AS/ GPIO_PORT1[3]	CLK25MOUT	Vss18_PLL	XOUT_14318	Vss18_PLL
C	INTA_	INTD_	GND	WDTTI/ GPIO_PORT3[4]	GPIO_PORT0[6]	GND	LDRQ_	LAD[2]	GND	PWR-GOOD	Vdd33_PLL	GND	Vdd18_PLL
D	GNT_[0]	REQ_[2]	REQ_[0]	INTB_	GPIO_PORT0[7]	GPIO_PORT0[3]	KBRST_	SERIRQ	RTC_WR_/ GPIO_PORT1[1]	RTC_RD_/ GPIO_PORT1[2]	Vdd33_PLL	Vss18_IO	Vdd18_PLL
E	PCICLK[0]	PCIRST_	GNT_[1]	GNT_[2]	GNT_[3]	3.3V POWER	GPIO_PORT0[2]	A20GATE_	3.3V POWER	IRQ8/ GPIO_PORT1[0]	SPEAKER	1.8V POWER	Vdd18_IO
F	AD[30]	PCICLK[1]	GND	PCICLK[2]	3.3V POWER								
G	AD[27]	AD[26]	AD[28]	AD[29]	AD[31]								
H	AD[24]	AD[25]	CBE[3]	AD[23]	AD[22]								
J	AD[21]	AD[19]	GND	AD[20]	3.3V POWER								
K	AD[18]	AD[17]	AD[16]	CBE[2]	IRDY_								
L	FRAME_	TRDY_	DEVSEL_	STOP_	PAR						GND	GND	GND
M	CBE[1]	AD[15]	GND	AD[14]	1.8V POWER						GND	GND	GND
N	AD[13]	AD[12]	AD[11]	AD[10]	AD[9]						GND	GND	GND
P	AD[8]	CBE[0]	AD[7]	AD[6]	AD[5]						GND	GND	GND
R	AD[4]	AD[3]	GND	AD[2]	1.8V POWER						GND	GND	GND
T	AD[1]	AD[0]	RTS3_/ SRST	GPIO_PORT2[7]/ SDD[7]	GPIO_PORT3[7]/ SDD[10]						GND	GND	GND
U	GPIO_PORT3[5]/ SDD[8]	GPIO_PORT2[6]/ SDD[6]	GPIO_PORT3[6]/ SDD[9]	GPIO_PORT2[5]/ SDD[5]	SOUT3/ SDD[12]								
V	GPIO_PORT2[4]/ SDD[4]	SIN3/ SDD[11]	GND	GPIO_PORT2[3]/ SDD[3]	3.3V POWER								
W	GPIO_PORT2[2]/ SDD[2]	SIN4/ SDD[13]	GPIO_PORT2[1]/ SDD[1]	SOUT4/ SDD[14]	RI3_/ SIORDY								
Y	GPIO_PORT2[0]/ SDD[0]	SIN5/ SDD[15]	DCD3_/ SDRQ	CTS4_/ SIOW	DSR3_/ SCBLID								
AA	CTS3_/ SIOR	DTR3_/ SDACK	GND	RTS4_/ SINT	3.3V POWER								
AB	RI4_/SA1	DCD4_/ SA2	DTR4_/ SA0	DSR4_/ SCS1	PDD[9]	3.3V POWER	PIOR_	PCBLID	3.3V POWER	MD[1]	MD[4]	1.8V POWER	Vdd18_DLL
AC	SOUT5/ SCS0	PRST	PDD[7]	PDD[5]	PDD[13]	PDRQ	PA[1]	PCS_[0]	MD[0]	MD[2]	MD[5]	MD[7]	Vss18_DLL
AD	PDD[6]	PDD[8]	GND	PDD[12]	PDD[0]	GND	PINT	SPI_DO/ GPIO_PORT1[6]	GND	MD[3]	MD[6]	GND	DQM[1]
AE	PDD[10]	PDD[4]	PDD[11]	PDD[1]	PDD[15]	PIORDY	PA[0]	PCS_[1]	SPI_CS_/ GPIO_PORT1[4]	MD[14]	MD[12]	MD[10]	MD[8]
AF	NC	PDD[3]	PDD[2]	PDD[14]	PIOW_	PDACK_	PA[2]	SPI_CLK/ GPIO_PORT1[5]	SPI_DI/ GPIO_PORT1[7]	MD[15]	MD[13]	MD[11]	MD[9]
	1	2	3	4	5	6	7	8	9	10	11	12	13

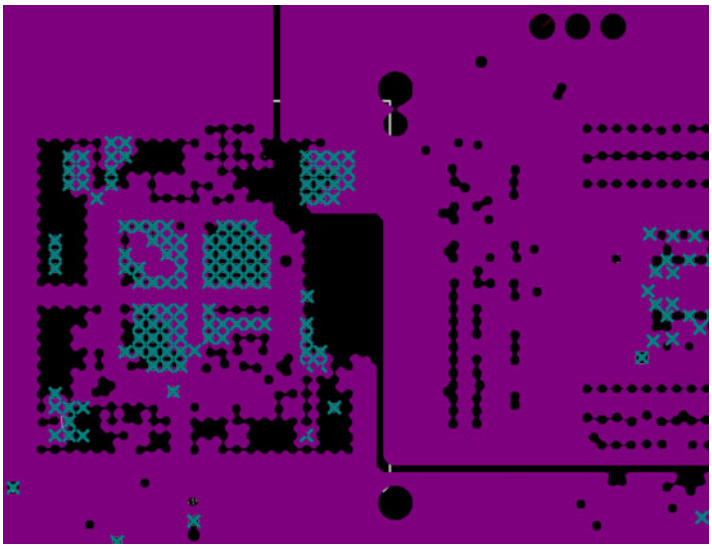
14	15	16	17	18	19	20	21	22	23	24	25	26	
RTC_PS	GND	DM0	GND	DM1	GND	SE_DI	SE_CS	TXD0[1]	RXD0[3]	RXD0[0]	TXEN1/ SOUT2	NC	A
RTC_XOUT	GND	DP0	GND	DP1	GND	SE_DO	SE_CLK	TXD0[0]	RXDV0	RXC0	MDC	TXD1[2]/ GPIO_ PORT3[2]	B
VBatGnd	GND	AVSS0	AVSSPLL	GND	GND	GND	GND	TXC0	RXD0[2]	GND	TXD1[3]/ GPIO_ PORT3[3]	TXD1[1]/ GPIO_ PORT3[1]	C
VBat	RTC_XIN	AVDD0	AVDDPLL	AVSS1	AVDD1	TXEN0	TXD0[2]	TXD0[1]	MDIO	TXD1[0]/ GPIO_ PORT3[0]	TXC1/ DCD2_	RXD1[2]/ DTR2_	D
GND	1.8V POWER	AVDD33	REXT	3.3V POWER	OVRCUR	TXD0[3]	3.3V POWER	COL0	RXDV1/ RI2_	RXD1[3]/ SIN2	RXD1[1]/ DSR2_	RXD1[0]/ CTS2_	E
								3.3V POWER	COL1/ TXD_EN2	GND	TXD_EN1	DTR1_/ GPIO_ PORT4[5]	F
								RXC1/ RTS2_	DCD1_/ GPIO_ PORT4[0]	DSR1_/ GPIO_ PORT[6]	CTS1_/ GPIO_ PORT4[7]	RTS1_/ GPIO_ PORT4[2]	G
								RI1_/ GPIO_PO RT4[3]	SOUT1/ GPIO_ PORT4[1]	SIN1/ GPIO_ PORT4[4]	ROMCS_	GPCS1_	H
								3.3V POWER	SD[15]	GND	SD[14]	SD[13]	J
								GPCS0	SD[12]	DACK_[7]	SD[11]	DRQ[6]	K
GND	GND	GND						DRQ[7]	SD[10]	DACK_[6]	SD[9]	DRQ[5]	L
GND	GND	GND						1.8V POWER	SD[8]	GND	DACK_[5]	MEMW_	M
GND	GND	GND						DRQ[0]	MEMR_	DACK_[0]	LA[17]	IRQ[14]	N

GND	GND	GND						LA[18]	IRQ[15]	LA[19]	IRQ[12]	LA[20]	P
GND	GND	GND						1.8V POWER	IRQ[11]	GND	LA[21]	IRQ[10]	R
GND	GND	GND						LA[22]	LA[23]	IOCS16_	MEMCS16_	SBHE_	T
								SA[0]	OSC14.318	SA[2]	SA[1]	BALE	U
								3.3V POWER	TC	GND	SA[4]	SA[3]	V
								IRQ[4]	IRQ[3]	SA[6]	DACK_[2]	SA[5]	W
								SA[10]	IRQ[7]	IRQ[5]	SA[8]	SA[7]	Y
								3.3V POWER	SA[11]	GND	IRQ[6]	SA[9]	AA
Vdd18_DLL	1.8V POWER	CAS_	BA[1]	3.3V POWER	0WS_	SD[0]	3.3V POWER	SA[18]	DRQ[3]	SA[12]	REFRESH_	SYSCLK	AB
Vss18_DLL	WE_	RAS_	MA[10]	MA[11]/ Strap[11]	SD[5]	DRQ[2]	SD[2]	AEN	SMEMR_	SA[14]	DRQ[1]	SA[13]	AC
CS_[1]	GND	CS_[0]	MA[0]/ Strap[0]	GND	SD[7]	SD[6]	GND	SD[1]	SA[19]	GND	SA[15]	DACK_[1]	AD
SDRAM-CLK	MA[9]	MA[7]/ Strap[7]	MA[5]/ Strap[5]	MA[1]/ Strap[1]	MA[3]/ Strap[3]	IOCHCK_	IRQ[9]	SD[3]	SMEMW_	IOW_	IOR_	DACK_[3]	AE
DQM[0]	BA[0]	MA[8]/ Strap[8]	MA[6]/ Strap[6]	MA[4]/ Strap[4]	MA[2]/ Strap[2]	MA[12]	PSTDRV	SD[4]	IOCHRDY	SA[17]	SA[16]	NC	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

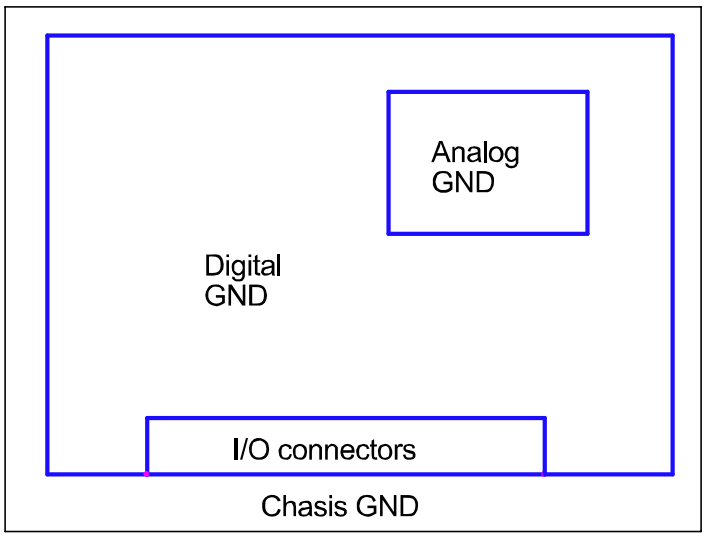
2.4 General Layout Rule

1. Keep all traces as SHORT as possible.
2. **Decoupling** is to remove the RF energy injected into the power distribution network from high-speed switching devices.
3. **Bypassing** is to divert unwanted common-mode RF noise from components or cables coupling from one area to another.
4. Place 0.01µF~0.1µF decoupling capacitors across each pair of VCC and GND pins. Use the shortest and thickest trace between decoupling capacitor and the VCC/GND pins.
5. Bulk capacitors ensure that a sufficient amount of DC voltage and current is available for digital components. At least one bulk capacitor should be located by:
   - Every VLSI device
   - Power connector(s)
   - Daughter card slots
   - Location furthest from the power connector
   - Clock generation circuitry
6. The voltage rating of the bulk capacitors should be 50% higher than the actual voltage level to prevent self-destruction and/ or voltage surge.
7. For decoupling of SDRAM interface, please check the SDRAM section for more details.
8. In digital circuits, conductors may be treated as transmission lines if the propagation time (T_{delay}) is equal to or greater than the pulse transition time (T_{rise} or T_{fall}).
9. The propagation speed on typical PCB is about 170 pS/inch (50 Ω Stripline), 150 pS/inch (50 Ω Microstrip).
10. There are 4 properties that affect the performance of the transmission line:
    - Impedance: reflection/ distortion
    - Time delay
    - High-Frequency Loss: limit signal bandwidth and transmission distance
    - Crosstalk: coupling
11. It is recommended to add serial damping resistors to all high-speed signals, especially the clock signals, to reduce high frequency energy and EMI. **These resistors should be placed as close to the driving source as possible.**
12. The clock signals should be the first routed trace in any PCB design. Adjacently routed (guard) ground traces provide shielding and signal return path. These ground shielding traces should be connected to the ground plane by vias at both ends. It is best to run all clock signals on the signal plane above a solid ground plane (on a multi-layer board).
13. If clock/ high-speed signals must make a layer jump, route ground trace adjacent to the signals and connect both ends of the ground trace to the GND plane, to form a RF return path of the signals.
14. The split power planes may cause serious EMI and signal integrity problems for high-speed signals which run adjacent to the power planes. To minimize these problems, some decoupling capacitors should be placed between these split power planes, to enhance RF return current path.
15. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through stitches of vias.
16. Example for BGA Power/ Ground routing:





17. Every I/O connector must be isolated from the digital ground and power planes. A clean or quiet ground must be located at the point where interconnects leave the system. Connect (“Bridge”) those grounds with only one connection. Only those signals required for operation or interconnect can run into the isolated area.



Note: the interconnects between GNDs were not shown.

18. Ensure that any signal passing between those sections runs ONLY through the “bridge”, and run the signals on a layer adjacent to the bridge to maintain RF return path.
19. If analog or digital power is not required in the isolated area, the unused power plane can be redefined as a second ground plane, referenced to the main ground plane by stitches of vias within the isolated area.
20. Connect system Power-on and H/W Reset to “Power-good” input of EVA-X4150, then use “/PCI_RST” output of EVA-X4150 to reset ALL peripherals.
21. The power-on-strap pins are combined with the memory address bus, which belong to DRAM power category. So the pull-high resistors should connect to the same supply (VCCO) of DRAM interface.
    For details of the power-on-straps function, please refer to the EVA-X4150 technical manual.
22. Follow the power-on sequence to prevent excessive current from the power supplies during power-up and power-down periods:
    – Power-up core supply (Vdd_core), and then power-up the I/O supply (Vdd_IO).
    – Power-down I/O supply (Vdd_IO), and then power-down the core supply (Vdd_core).
23. Recommend Termination

Signal	Zs (Ω)	Termination(Ω)	Trace Impedance (Ω)
Clocks: 14.318 M	28.1	22	50
Clocks: 24 M, 25 M	14	33	50
PCI clock	7.2	50	60
PCI signal	13.2	47	60
DRAM Clocks	19	33	60
DRAM signal	19	33	60

24. Recommended PCB stack up

a. 4 Layers:

Layer	Type	Description	Material/ Thickness
1	Signal	Top Routing	Copper/ 0.5 ~ 1 oz
		FR4/ 5mil	
2	Plane	**Ground**	Copper/ 1 oz
		FR4/ 40mil	
3	Plane	Power	Copper/ 1 oz
		FR4/ 5mil	
4	Signal	Bottom Routing	Copper/ 0.5 ~ 1 oz

b. 6 Layers:

Layer	Type	Description	Material/ Thickness
1	Signal	Top Routing	Copper/ 0.5 ~ 1 oz
		FR4/ 5mil	
2	Plane	**Ground**	Copper/ 1 oz
		FR4/ 5mil	
3	Plane	**Power**	Copper/ 1 oz
		FR4/ 40mil	
4	Signal	Internal Routing	Copper/ 1 oz
		FR4/ 5mil	
5	Plane	**Ground**	Copper/ 1 oz
		FR4/ 5mil	
6	Signal	Bottom Routing	Copper/ 0.5 ~ 1 oz

2.5 Crystal / External Oscillator

The EVA-X4150 requires a 14.318 MHz clock to generate all the internal and external clocks. Connect an external 14.318 MHz crystal (Parallel-resonant) between Xtal_I and Xtal_o pins to operate as a Pierce oscillator. The EVA-X4150 specification requires a frequency tolerance of ±30 parts per million (PPM).

The other way is to use an external 14.318MHz oscillator, and directly route the oscillator's output into XTALi pin of EVA-X4150. A serial damping resistor and a bypass capacitor are recommended for EMI reduction. The XTALo pin should leave unconnected. The requirement of the clock's duty cycle should be between 40% ~ 60%.

2.5.1 Crystal Specification

Parameter	Specification	Note
Type	Parallel Resonant	
Frequency	14.318 Mhz	±30 ppm
Equivalent Series Resistance	25 Ω	Max.
Load Capacitance	18 pF	Typ.
Case Capacitance	7 pF	Max.

2.5.2 Recommended Layout

- Route the signal traces of the crystal to EVA-X4150 as SHORT as possible.
- When using an external crystal with EVA-X4150 internal oscillation circuitry to work as clock oscillator, be sure to put all the related components close to EVA-X4150 chip. The ground area under the crystal circuitry should be physically insolated from the system ground plane with only a small bridge between them for signals crossing. This isolation prevents noise located elsewhere on the PCB from corrupting the oscillator circuitry.
- The power plane under the crystal/ oscillator area should be void, when not in use, or insolated with exactly the same pattern of ground plane.
- Do NOT run any signals under this area, for EMI and interference enhancement.

2.6 SDRAM Interface

1. It is assumed that the reader is familiar with the specification and the basic electrical operation of the SDRAM interface.
2. EVA-X4150 SDRAM interface substrate conductors' length for signal integrality:

EVA-X4150 Substrate Conductor Length

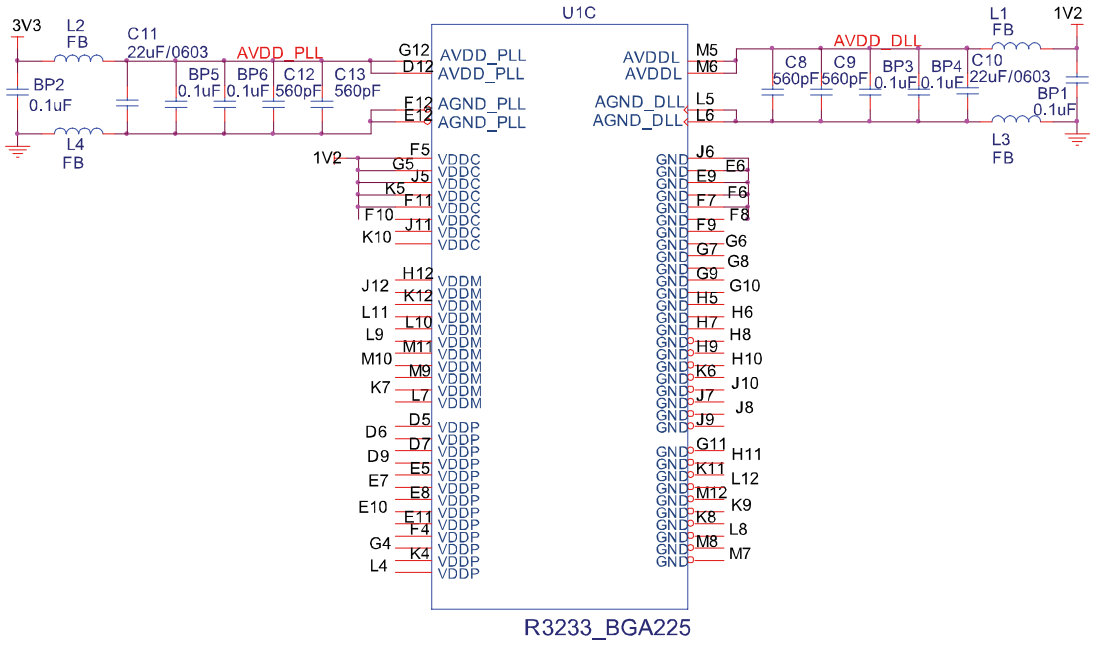
Net Name	Length in microns
MA[0]	13283.31
MA[1]	12989.16
MA[2]	8745.03
MA[3]	10321.07
MA[4]	10173.85
MA[5]	11728.8
MA[6]	12466.29
MA[7]	11480.64
MA[8]	7638.44
MA[9]	10753.84
MA[10]	13659.62
MA[11]	9367.04
MA[12]	7999.4
MD[0]	12939.2
MD[1]	12379.26
MD[2]	12218.38
MD[3]	12868.28
MD[4]	13327.88
MD[5]	11731.55
MD[6]	11817.28
MD[7]	11681.94
MD[8]	11494.07
MD[9]	10379.54
MD[10]	10577.86
MD[11]	11902.14
MD[12]	11610.42
MD[13]	10048.32
MD[14]	10981.68
MD[15]	12062.12
BA0	10484.24
BA1	9914.61
/CAS	9668.98
/CS0	10088.02
/CS1	10430.52
DQM0	12436.31
DQM1	10402.02
MCLK	6700.98
/RAS	11307.98
/WE	10909.61

3. In order to meet the maximum interface speed (150 MHz), memory device drive strength should be set 100% strength. This requires the series terminations to avoid excessive Under/Over-shoot. **We highly recommend reserve terminations for ALL high speed signals. It is much easier to remove terminations than adding them after the PCB has been found to fail EMI.**
4. It is critical that all signal routing layers have a ground reference plane, meaning that there is a full, contiguous ground plane next to every SDRAM routing layer.

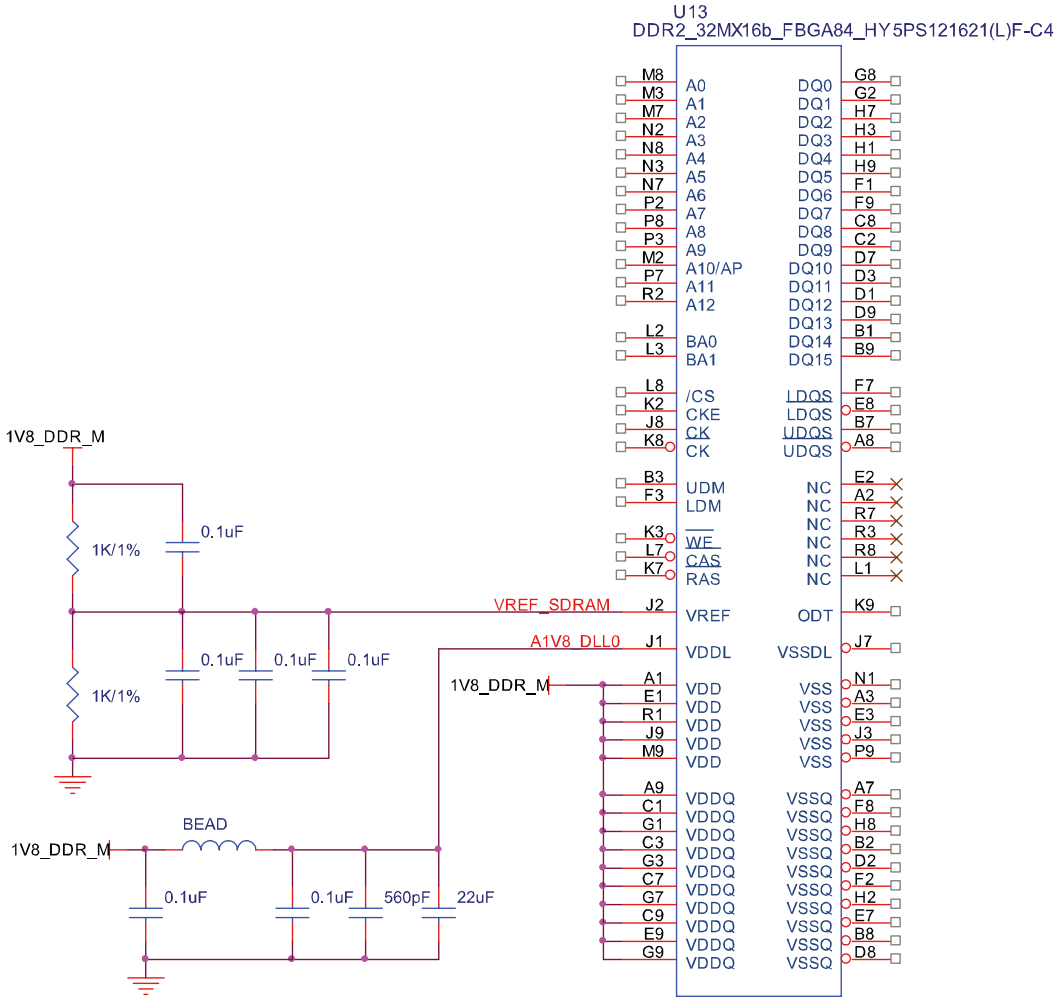
The purpose is to provide a path for return currents to minimize crosstalk and EMI.

5. The SDRAM devices should be placed as close to EVA-X4150 as possible. The distance between SDRAM devices and EVA-X4150 should less than **3** inches.
6. Other devices should be kept away to ensure other signals do not interfere with the SDRAM interface.
7. All signals avoid crossing over an unrelated plane or different power plane. Six or more layers of PCB could eliminate these problems by routing SDRAM signals in the layer that is adjacent to the ground plane(s).
8. Route traces with minimal layer transitions and minimize the total number of turns and vias.
9. Decoupling capacitors are critical to the reliable operation of the SDRAM interface. The decoupling capacitors should be **0402** size or smaller.
10. Bulk capacitors ensure that a sufficient amount of DC voltage and current is available for SDRAM devices. At least one bulk capacitor should be located for each SDRAM device.
11. DO NOT share the vias for decoupling capacitors, due to the inductance of the vias.
12. To minimize inductance, power vias should be as large as possible, but take good care of the inadvertently cut of the ground and power planes.
13. The PLL and DLL power supply pins draw small currents, but they are noise sensitive. Each supply should be filtered by **π-filter** networks. Use Ferrite Bead, NOT inductor.

i. EVA-X4150:



ii. SDRAM:



14. Recommended Terminations for SDRAM interface:

Signal	Impedance (Ω)	Value (Ω)	Note
Clock	Differential, 90	33	Near EVA-X4150
A[0…12], BA[0...1], Controls	60		Near EVA-X4150
DQM			Near EVA-X4150
DQ[0...15]			Near SDRAM
MD[0...15]			Near EVA-X4150

Note! *Termination value may have to be adjusted according to manufacturing condition.*

15. Recommended layout:

Trace length (include the substrate & PCB trace length) routing:

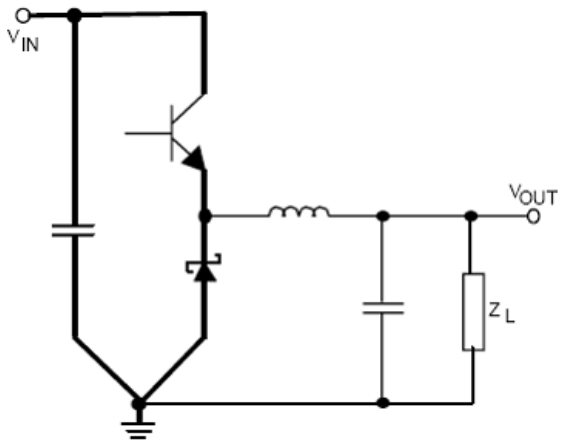
(a) All signals avoid crossing over an unrelated plane or different power plane.

(b) Route traces with minimal layer transitions and minimize the total number of turns & vias.

Signal	Width/ Spacing/ Isolation	Maximum Length	Note
Data Mask	5 mil/ >5 mil/ 15 mil	3 inches	
Data Bus	5 mil/ >5 mil/ 5 mil		
Clock	5 mil/ >20 mil/ 20 mil		
Address	5 mil/ >5 mil/ 5 mil	Kept to a minimum	
Command	5 mil/ >5 mil/ 5 mil Width > 20 mil		
Power/ GND			

2.7 Switching Power

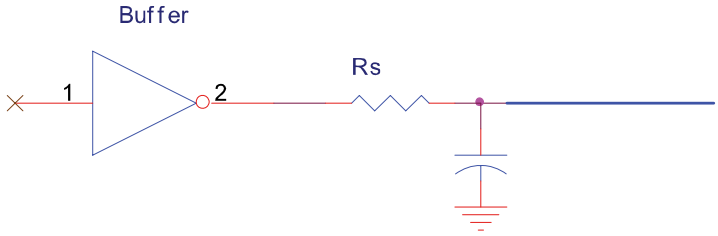
1. Please check section 2.3 and SDRAM data sheet for the detailed requirements of the power for SDRAM system.
2. In a step-down switching regulator, the input bypass capacitor, the main power switch and the freewheeling diode carry discontinuous currents with high dt / di. For jitter-free operation, the size of the loop formed by these components should be minimized.



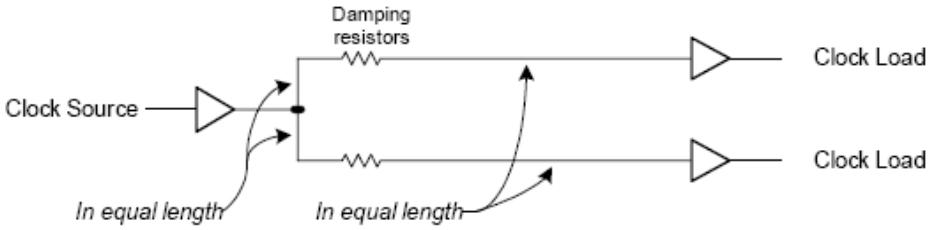
3. The input bypass capacitors should be placed close to the VIN pins. Shortening the traces of the SW node reduces the parasitic trace inductance at these nodes. This not only reduces EMI but also decreases switching voltage spikes at these nodes.
4. Some switching devices have an exposed pad which should be soldered to a large analog ground plane, as the analog ground copper acts as a heat sink. To ensure proper adhesion to the ground plane, avoid using vias directly under the device.
5. For more detailed design information, please refer to the switching regulator's data sheet.

2.8 PCI Interface

1. **We highly recommend reserve terminations for ALL PCI signals. It is much easier to remove terminations than add them after the PCB has been found to fail EMI.**
2. The trace length for all PCI signals must be limited to 7 inches.
3. The trace length for PCI Clocks must be short for on-board PCI devices to minimize the clock skew.
4. The PCI clock traces should be parallel to their reference plane, usually ground planes. That means the clock traces should be right beneath or on top of their reference plane.
5. There is NO board impedance specified in the PCI bus specification. We recommend the trace impedance to be **60 Ω ± 10%**, with a **trace width/spacing** design of **5 mil/10 mil**.
6. Add serial termination resistor and bypassing capacitor (tens of pF) to PCI clock signals to match the trace impedance and enhance EMI.



7. Avoid running PCI clocks in parallel with other signals for a long distance, for interference and coupling.
8. The user may need to drive two or more source-terminated clock lines with single output. However, the following condition must be achieved:
i. The clock traces' length must be as equal as possible, to guarantee the arriving time of the reflected pulses.
ii. The loads must be balanced, to guarantee the same shape of the reflected pulses.



iii. The termination value must be calculated according to:

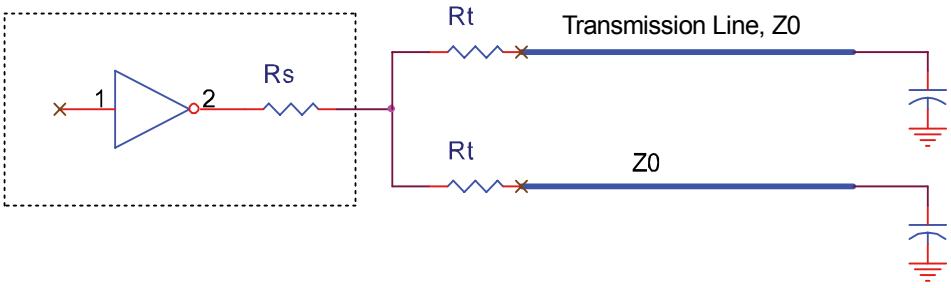
$R_t = Z0 - R_s * N$

R_t = termination resistor, Ω

R_s = output impedance of the driver

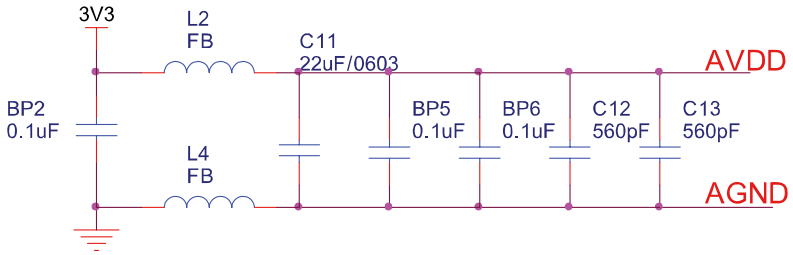
Z_0 = line impedance

N = number of lines



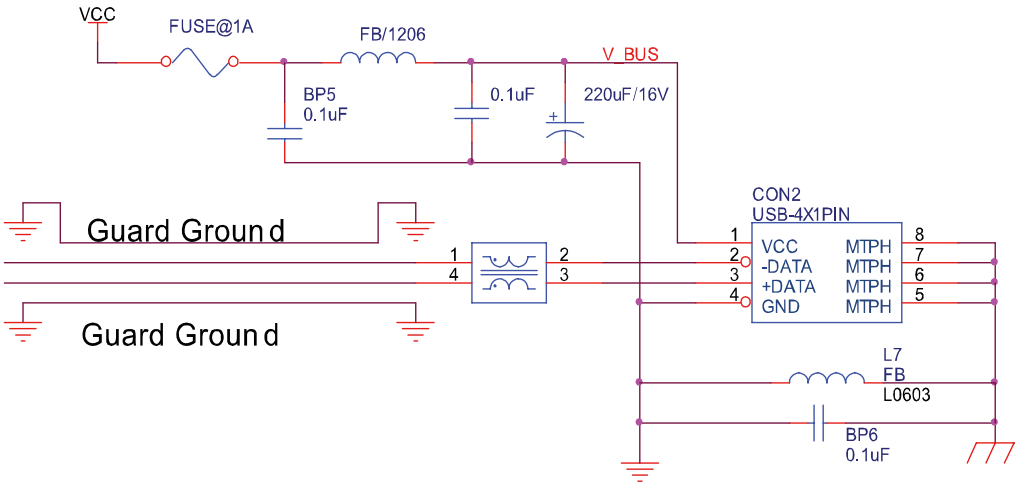
2.9 USB 2.0

1. **Route the Hi-Speed USB differential pairs over continuous ground or power planes. Avoid crossing anti-etch areas and any breaks in the internal planes (plane splits).**
2. Avoid placing a series of vias near the DP and DM lines, as these will create “break areas” in the ground plane below.
3. Avoid routing the USB differential pairs near I/O connectors, signal headers, crystals/ oscillators, magnetic and power connectors.
4. Maintain parallelism between USB differential signals, with the trace spacing needed to achieve **90 Ω differential impedance**.
5. We recommend the trace **Width/ Spacing/ Isolation** of USB differential pairs to be **8 mil/ 8 mil/ >20 mil**. And the mismatch of the differential pairs should be **less than ±70 mil**. These values may vary depending on the actual PCB parameters.
6. The maximum trace **length** of USB differential pairs should be **less than 2”**.
7. The common-mode choke used (**if really necessary**) on the DP and DM lines must be placed as close as possible to the USB connector and must have Z_{com}< 8 Ω @ 100 MHz and Z_{diff} < 300 Ω @ 100 MHz.
8. The analog power pins of EVA-X4150, AVDD0/1/2/3 and AVDDPLL0/1, need to be properly filtered for USB performance.



9. It is recommended to connect the analog ground pins of EVA-X4150, AVSS0/1/2/3 and AVSSPLL0/1, to an isolated (quiet) analog ground plane, which is connected to the digital ground plane with a single “Bridge” or Ferrite Bead. Please refer to section 2.4 for more details.
10. Place the external resistors of REXT0/1, pin U26 & P26, as close to the EVA-X4150 as possible. And connect another ends of these external resistors to the isolated analog ground plane described above.
11. Do not run any high-speed signal close to the external resistors of REXT0/1 to keep from interference and coupling.
12. Provide a good path from the USB connector shell to the chassis ground.
13. Maintain the maximum possible distance between Hi-Speed USB differential pairs, high-speed or low-speed clock, and non-periodic signals. The minimum recommended distances are as follows:
    – 20 mils between the DP and DM traces and low-speed non-periodic signal traces.
    – 50 mils between the DP and DM traces and clock/high-speed periodic signal traces.
    – 20 mils between two pairs of the DP and DM traces.
14. USB data lines must be routed as “**critical signals**”. Locate the USB connector close to EVA-X4150. The DP and DM signals in a pair must be routed in parallel to each other. Do not route these traces near high frequency signals. Guard ground traces on each side of the signal pair can minimize the induced common mode noise.

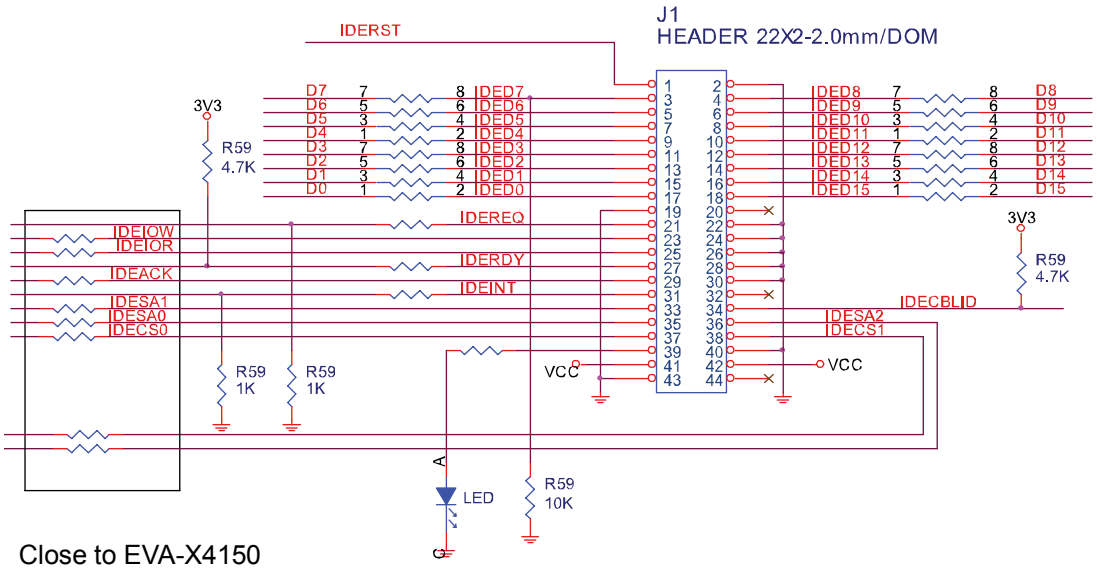
15. Ferrite beads and decoupling capacitor placed on VBUS are for EMI purposes, thus these components should be placed close to the USB connectors. A value of about 150 µF/10 V for the decoupling capacitor is recommended on each port.



2.10 IDE

The trace-length and impedance-match must be considered for IDE signals to enhance the EMI and signal integrity:

1. The pull-up resistors on open-collector signals, such as IORDY, should be more than 1 KΩ.
2. All IDE signals need to be serial terminated. Place the termination resistors for A[0..2], CS[0..1], /IOR, /IOW and /DACK near EVA-X4150. Place the termination resistors for D[0..15], DRQ, IORDY, and IRQ near IDE connector.
3. The termination value should be optimized to compensate for transceiver and trace impedance to match the characteristic cable impedance.
4. The 28th pin of IDE connectors (CSEL) should be pulled low.
5. Signals in the same channel should have the same length, the mismatch must be less than 1”.
6. Reference circuitry:



Close to EVA-X4150

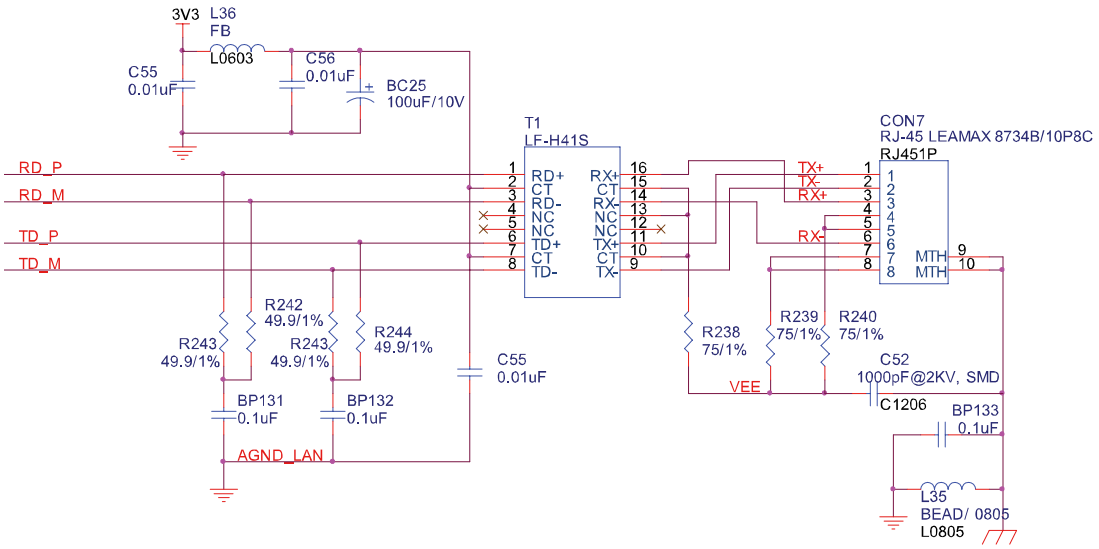
2.11 LPC Interface

A Low Pin Count (LPC) controller is integrated in EVA-X4150. The LPC interface is to replace ISA interface serving as a bus interface between the system processor and peripherals (e.g. LPC super I/O chip). Many of the signals are the same as signals found on the PCI interface. Data transfer on the LPC bus is serialized over a 4-bit bus.

Rout the LPC signals with the PCI design rule.

2.12 10/100 LAN

1. Recommended Schematics:



2. Magnetics Specification:

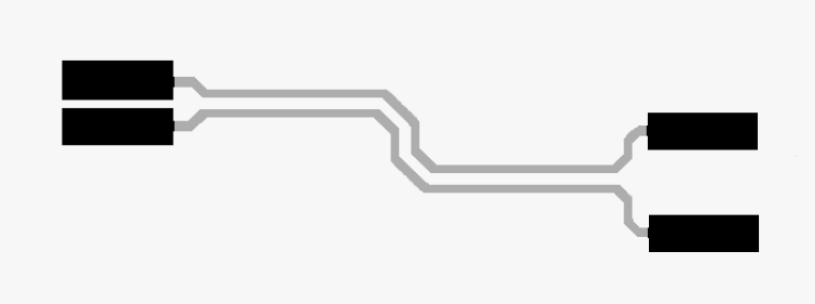
Parameters	Specification		Note
	Tx	Rx	
Turns Ratio	1:1 CT	1:1	
Inductance, μH	350	350	
Leakage Inductance, μH	TBD	TBD	
Capacitance, pF	15	15	
DC Resistance, Ω	0.4	0.4	

3. Magnetics Selection Guide:

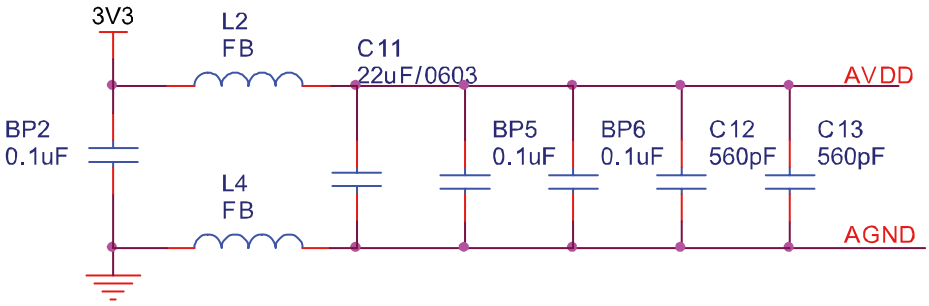
Manufacturer	Part Number	Note
Delta		
YCL		
Bothhand		
Pulse Engineering		

4. Keep the distance between the EVA-X4150 and the RJ-45 connector short (under 4”).
5. Route the differential traces, TX±, RX±, TD± & RD±, for 100 Ω differential impedance.
6. Keep the differential traces lengths equal to reduce signal skew.

7. Keep the differential traces close and symmetric to reduce noise.



8. The parallel termination resistors of TD± should be placed near the magnet. The parallel termination series resistors of RD± should be placed near the EVA-X4150.
9. It is recommended to route the differential traces' turn with arcs, and avoid any vias and corners.
10. The traces of TX± / TD± pair should be kept away from RX± / RD± pair. It is best to place ground guard traces between these two pair of traces.
11. We recommend the trace **Width/ Spacing/ Isolation** of TX± / TD± and RX± / RD± pairs to be **8 mil/ 10 mil/ >20 mil**. And the mismatch of the differential pairs should be **less than ±100 mil**.
12. Do NOT run any digital trace close to and parallel to the differential pairs.
13. The RJ-45 and output side of transformer should reference to quiet ground plane (chassis ground) which is isolated from the ground plane of the input side of transformer and EVA-X4150. Connect this quiet ground plane to system ground with only one connection (bridge). Do NOT run any signal into this isolated area.
14. The moat to isolate the quiet ground should be at least **100 mil**.
15. Avoid laying power and ground planes underneath the magnet to enhance EMI.
16. Provide a good path from the RJ-45 connector shell to the chassis ground.
17. The analog power pins of EVA-X4150, VCCAPLL, VCCABG, VCCA0/1 and AVDD33_0/1, need to be properly filtered for LAN performance.



18. It is recommended to connect the analog ground pins of EVA-X4150, VSSAPLL, VSSABG and VSSA0/1, to an isolated (quiet) analog ground plane, which is connected to the digital ground plane with a single "Bridge" or Ferrite Bead. Please refer to section 2.4 for more details.
19. **Place the external resistor of ISET, pin J24, as close to the EVA-X4150 as possible. And connect another end of the external resistor to the isolated analog ground plane described above.**
20. Do not run any high-speed signal close to the external resistor of ISET to keep from interference and coupling.

Appendix A

References

A.1 References

1. “EVA-X4150 Technical Manual”
2. “PCI Local Bus Specification” rev. 2.2
3. “EMC and the Printed Circuit Board”, Mark I. Montrose
4. “High-speed Digital Design”, Howard W. Johnson, PH.D.
5. “Noise reduction Techniques in the Electronic System”, Henry W. Ott
6. “Printed Circuit Board design Techniques for EMC Compliance”, Mark I. Montrose.

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