AIMB-350

Socket 478 Embedded ATX/ Micro ATX for Multimedia Applications

User Manual

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This manual is for the AIMB-350.

Part No.2006035010 1st Edition

Dec. 2005

Packing List

Before you begin installing your board, please make sure that the following materials have been shipped:

- 1 AIMB-350 all-in one single board computer
- 1 startup manual
- 1 CD-ROM or disks for utility, drivers, and manual (in PDF format)
- 1 UDMA/66 IDE flat cable p/n:1701400452
- 1 COM2(W/485/422)cable p/n:1701140201
- 1 DMA/33 IDE 40 to 44pin IDE flat cable p/n:1701440350
- 1 I/O shield p/n:1960001955
- 4 COM port cable kit 18CM p/n:1701400181

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Optional Items:

- 1 USB cable (2.54mm) p/n:1700000719
- 1 DVI cable p/n:1700000410
- 1 FDD cable p/n:1701340700
- 1 SATA cable p/n:1700001054
- 1 P4 CPU FAN p/n:1750000069
- 1 COM3.4 cable 20pin (22CM) cable p/n:1701200220

Model No. List	Description
AIMB-350F-00A1	SKT 478 Pentium M SBC w/8USB/2LAN/ 4COM/2PCIX/1PCI
AIMB-350G-00A1	SKT 478 Pentium M SBC w/8USB/ 2GigaLAN/4COM/1PCIX/1PCI
AIMB-350L-00A1	SKT 478 Pentium M SBC w/4USB/1LAN/ 4COM/1PCIX

Part Number	AIMB-350F-00A1	AIMB-350L-00A1	AIMB-350G-00A1
Form factor	EmbATX	EmbATX	MicroATX
LAN	2x 10/100	1x 10/100	2x Giga
USB	8ports	4ports	8ports
Display support	CRT/LVDS/TTL/DVI/TV out	CRT/LVDS	CRT/LVDS/TTL/DVI/ TV-out
SATA	2	2	2
COM	4 ports	4 ports	4 ports
Mini PCI	V	V	V
CF	V	V	V
Expansion slot	2 x PCI-X, 1x PCI	1x PCI-X, 1x PCI	1x PCI-X, 1x PCI

Additional Information and Assistance

Visit the Advantech web site at **www.advantech.com** where you can find the latest information about the product.

Step 1. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:

- Product name and serial number
- Description of your peripheral attachments
- Description of your software (operating system, version, application software, etc.)
- A complete description of the problem
- The exact wording of any error messages

FCC

This device complies with the requirements in part 15 of the FCC rules: Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and

2. This device must accept any interference received, including interference that may cause undesired operation

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this device in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense. The user is advised that any equipment changes or modifications not expressly approved by the party responsible for compliance would void the compliance to FCC regulations and therefore, the user's authority to operate the equipment.

Caution!

Achtung!

There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Contents

CHAPTER 1

General Information

This chapter gives background information on the AIMB-350.

Sections include:

- Introduction
- Features
- Specifications
- Board layout and dimensions

Chapter 1 General Information

1.1 Introduction

The AIMB-350 series is an Embedded ATX/Micro ATX form factor (Socket 478) design for Intel Pentium® M processors with 400MHz FSB and Intel's 855GME and 6300ESB chipsets that support enhanced Intel "SpeedStep" technology and Dynamic Video Memory Technology. For maximum performance, AIMB-350 also supports two 200 PIN SODIMM sockets for ECC DDR memory up to 2GB. These chipsets are specifically for embedded computing and provide an optimized onboard integrated graphics solution. "SpeedStep" technology intelligently focuses system power where the CPU needs it and automatically regulates power usage to preserve battery life.

This product uses Intel 855GME chipset for dual independent display. AIMB-350F and AIMB-350L allow CRT+LVDS, DVI+LVDS, CRT+DVI combinations. The dual independent display is suitable for POS, Kiosks and multiple display applications.

There are 2 Ethernet interfaces that can be used; one LAN for communication and the other one for backup purposes.

Other onboard comprehensive peripherals include 2 EIDEs, 2 SATAs, up to 6 USB 2.0, 4 serial ports (3x RS-232 and 1x RS-232/422/485), 1 FDD, 1 LPT, PS/2 Keyboard/mouse, watchdog timer, and a DIO interface. The SSD solution supports Type I/II CompactFlash cards, and the standard expansion interface includes PCI, PCI-X and miniPCI for user expansion purposes.

AIMB-350 series are the best *all-in-one* embedded motherboards specifically designed for the embedded market.

1.2 Features

- Intel Pentium M/Celeron M 400MHz FSB Socket 478 uFCPGA2 Processor
- 0~60°C operating temperature
- Intel 855GME dual independent display (CRT+LVDS, DVI+LVDS,CRT+DVI)
- Up to 2 x Gigabit LAN on board (AIMB-350G)

- Supports 2 SATA
- AGP, PCI, PCI-X multiple expansion
- Supports 8 x USB2.0 port
- Option up to 2 Channel 36bits LVDS for LCD
- Supports 400 MHz Front Side Bus
- Supports 200 MHz, 266 MHz and 333 MHz ECC DDR SDRAM

1.3 Specifications

1.3.1 Standard SBC Functions

- **CPU:** Intel Pentium M/Celeron M 400 MHz FSB Socket 478 uFCPGA2 Processor (Up to Pentium M 2 GHz)
- **System chipsets:** Intel 855GME + 6300ESB
- **BIOS:** Award 4 Mbit Flash memory
- **System memory:** 200 pin DIMM x 2, support ECC double data rate (DDR) 128 MB to 2 GB, accepts 128/256/512/1000 MB DDR 200/266/333 DRAM
- **2nd cache memory:** 1 or 2 MB on Pentium M processor, 512 MB on Celeron M
- **PCI interface:** Supports PCI Rev 2.2 Specification at 33 MHz
- **PCI-X interface:** Supports PCI-X Rev 2.2 Specification at 66 MHz
- **AGP interface:** Support AGP 2.0 slot (1x/2x/4x)
- **Enhanced IDE Interface:** Supports two enhanced IDE channels. Primary channel supports ATA-100 mode; Secondary channel only supports ATA-33 and PIO mode. CFC card occupies secondary master
- **Serial Ports:** Four serial ports: COM1, COM3, COM4: RS-232, COM2: RS-232/422/485
- **Parallel Ports:** one parallel port, support SPP/EPP/ECP
- **Keyboard/Mouse Connector:** Supports standard PC/AT Keyboard and a PS/2 Mouse
- **Power Management:** Supports Power Saving Mode including Normal/Standard/Suspend modes. APM 1.2 compliant.
- **FDD interface:** Support up to two FDD devices
- **DIO interface:** Supports 8 general purpose input/output ports
- **Watchdog Timer:** 0~255 Sec., System reset
- **Expansion Interface:** 4 x AGP, 32-bit PCI Slot and 64-bit PCI-X Slot, support PCI 2.2

- **Battery:** Lithium 3V/195 mAH
- **USB:** Up to 8 USB Intel 6300ESB ports, USB 2.0 compliant
- **SATA:** Intel 6300ESB supports data transfer rates up to 150 Mbyte/s, support RAID 0.1

1.3.2 Display Interface

- **Chipset:** Intel 855GME
- **Memory size:** Optimized Shared Memory Architecture, supports up to 64 MB frame buffer using system memory
- **Display modes:**
  CRT Modes: up to 2048 x 1536 at 75Hz;
  LCD Modes: up to 1280 x 1024 at 85Hz
- **LCD Interface:** 2 Channel LVDS (up to 36-bit)
- **LVDS:** Hirose connector support dual channel LVDS panel, up to UXGA panel resolution with frequency range from 25 MHz to 112-MHz

1.3.3 DVI

- **Chipset:** Chrontel CH7009
- Drives a DVI display at a pixel rate of up to 165MHz, supporting UXGA resolution displays
- DVI hot plug detection
- Compliant with DVI Specification 1.0

1.3.4 Solid State Disk

- Supports CompactFlash Type I/II disks

1.3.5 PCI bus Ethernet interface

- **Chipset:** Intel 82541GI (Gigabit), Intel 82551ER/82551QM(optional)
- **Connection:** onboard 2XRJ-45
- **Interface:** IEEE 802.3 z/ab(1000BASE-T) or IEEE 802.3u(100BASE-T) protocol compatible
- **Boot ROM:** build-in-system (Supported by 82541GI and 82551QM (optional))

1.3.6 Mechanical and Environmental

- **Dimensions (L x W):** 185 x 122 mm (7.3” x 4.8”)
- **Power supply voltage:** +5 V, +5V STB, +12V
- **Power requirements:**
  Typical: +5V@2.91A, +12V@0.09A(Pentium M 1.6G, 256 MB DDR333 with MPEG1)
  Max: +5V@4.54A, +12V@0.13A(Pentium M 1.6G, 256 MB DDR333 with HCT9.5)

- **Operating temperature:** 0 ~ 60°C (32 ~ 140°F),operation
- **Operating humidity:** 0% ~ 90% Relative Humidity, Non condensing

1.4 Board layout: dimensions

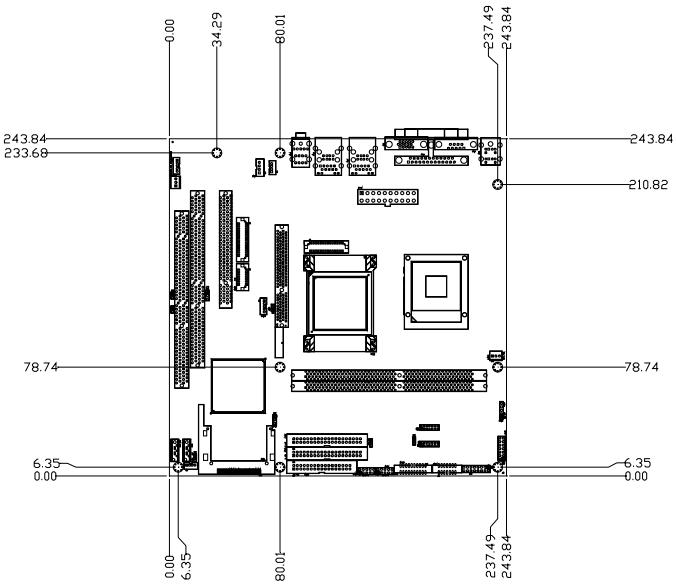


Figure 1.1: Board layout: dimensions (component side)

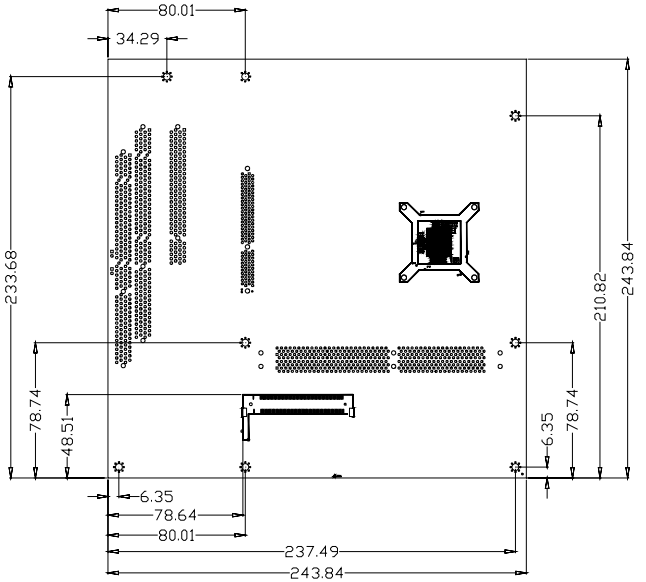


Figure 1.2: Board layout: dimensions (solder side)

CHAPTER 2

Installation

This chapter explains the setup procedures of AIMB-350 hardware, including instructions on setting jumpers and connecting peripherals, switches and indicators. Be sure to read all safety precautions before you begin the installation procedure.

Chapter 2 Installation

2.1 Jumpers

The AIMB-350 has a number of jumpers that allow you to configure your system to suit your application. The table below lists the functions of the various jumpers.

Table 2.1: Jumpers

Label	Function
JP2	VIA-VT6212 USB Controller Power Select
JP3	VIA-VT6212 USB Controller Wake-Up Function Select
JP4	Front Panel Connector
JP5	COM Port 1~6 Voltage Select Connector
JP6	COM Port 1~6 Ring/COM2 (RS-232/422/485)Select Connector
JP7	SM Bus Connector Power Select
JP8	PCI-X Clock Select Connector
JP9	PCI-X VIO Power Select Connector
JP10	AGP/DVO Mode Select
JP11	PCI-X Clock Select Connector
JP12	CMOS Clear Jumper

2.2 Connectors

Onboard connectors link the AIMB-350 to external devices such as LCD Panels, LEDs, hard disk drives, a keyboard, or floppy drives. The table below lists the function of each of the board's connectors.

Table 2.2: Connectors

Label	Function
CN1	CRT Connector
CN2	COM1 Connector
CN3	LPT Connector
CN4	Audio Connector
CN5	KB/MS Connector

Table 2.2: Connectors	
CN6	LAN2+USB 3/4 Connector
CN7	LAN1+USB 1/2 Connector
CN8	Panel Inverter Connector
CN9	CD-IN Connector
CN10	Internal Speaker Connector
CN11	LCD Connector
CN12	DVI Connector
CN13	Internal USB 7/8 Port Connector
CN14	Internal USB 5/6 Port Connector
CN15	SIR Connector
CN16	CompactFlash Connector
CN17	Primary IDE Connector
CN18	Secondary IDE Connector
CN19	SM Bus Connector
CN20	Floppy Connector
CN21	COM2 Connector
CN22	COM3~6 Connector
CN23	Digital IO Connector
CN24	Mini PCI Connector
CN25	TV OUT Connector
SA1	SATA1 Connector
SA2	SATA2 Connector
ATX1	ATX Power Connector
VCN1	LVDS Connector
FAN1	SYSTEM FAN
FAN2	CPU FAN
AGP1	AGP SLOT
PCI1	PCI SLOT
PCIX1	PCIX1 SLOT
PCIX2	PCIX2 SLOT

2.3 Locating Connectors (component side)

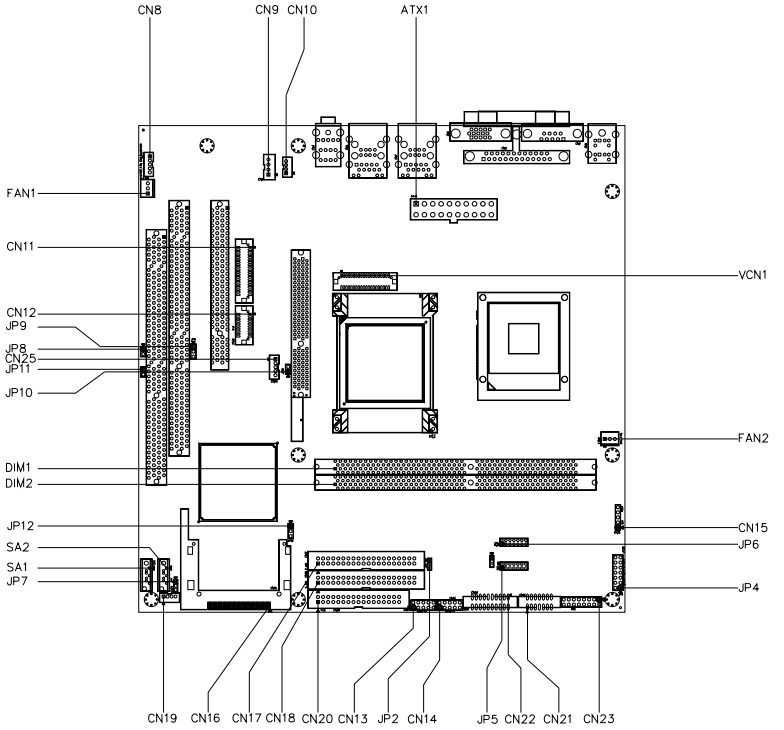


Figure 2.1: Jumper & Connector Locations

2.4 Locating Connectors (solder side)

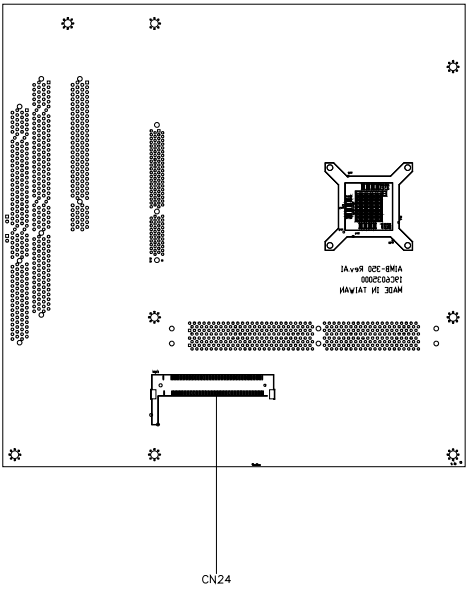
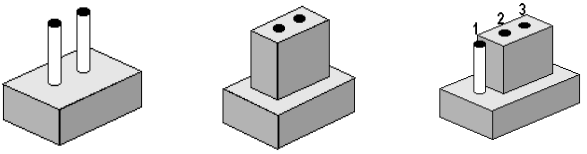


Figure 2.2: Connectors (component side)

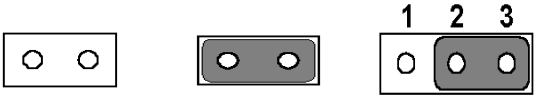
2.5 Setting Jumpers

You may configure your card to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper, you connect the pins with the clip. To “open” a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.



open closed closed 2-3

The jumper settings are schematically depicted in this manual as follows:.



open closed closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

2.6 USB Controller Power Select (JP2)

This jumper sets ALL USB ports to use 3.3V at anytime or 3.3V standby power (3.3VSB) when the system is in sleep mode.

Table 2.3: VIA-VT6212 USB Controller Power Select

Close pins	Result
1-2	3.3v
2-3	3.3VSB

*: Default value 3.3VSB

2.7 USB Wake-up Function (JP3)

Sets all the USB ports to wake-up or NOT wake-up during sleep mode.

Table 2.4: VIA-VT6212 USB Controller Wake-Up Function Select

Close pins	Result
1-2	Enable
2-3	Disable

*: Default value Enable

2.8 Front Panel Connector (JP4)

Table 2.5: Front Panel Connector Type: Pin-Header 14-Pin 2.54mm

Pin	Function	Pin	Function
7	3VSB(LAN_ACKLED)	8	LAN_ACKLED#
11	GND	12	PWRBTN#

*: LOW ACTIVE

2.9 COM Ports Ring and Voltage (JP5)

Table 2.6: COM Ports Ring & Voltage Select Jumper

Pin	Function	Pin	Function
1	VCC	2	VCC
3	RI#1	4	RI#2
5	+12V	6	+12V
7	NC	8	NC
9	VCC	10	VCC
11	RI#3	12	RI#4
13	+12V	14	+12V
15	NC	16	NC
17	VCC	18	VCC
19	RI#5	20	RI#6
21	+12V	22	+12V

*: LOW ACTIVE

2.10 COM Ports Ring and COM2 (RS232/422/485)(JP6)

Table 2.7: COM Ports Ring & COM2 (RS232/422/485)Select Jumper

Close Pins	COM2
1-2	RXD485
3-4	RXD422
5-6	RXD232 (Default: Close)
7-8	RI#1(Default: Close)
9-10	RI#2(Default: Close)
11-12	RI#3(Default: Close)
13-14	RI#4(Default: Close)
15-16	RI#5(Default: Close)
17-18	RI#6(Default: Close)

2.11 SM BUS Power Select (JP7)

This board can support client SMBUS 3.3V or 5V power when SM BUS.had been connected.

Table 2.8: SM BUS Power Select	
Close pins	Result
1-2	3.3V (Default: CLOSE)
2-3	5V

*: Default value 3.3V

2.12 PCI-X Socket Clock Set (JP8 & JP11)

This board can support PCI 33 MHz/66 MHz or PCI-X 66 MHz

Table 2.9: PCI-X Clock Select Connector		
JP8 Close pin	JP11 Close pin	Result
1-2 SHORT	1-2 SHORT(DEFAULT)	PCI 33
1-2 OPEN (DEFAULT)	1-2 SHORT(DEFAULT)	PCI 66
1-2 SHORT	1-2 OPEN	PCI-X 66

*: Default value (OPEN)

2.13 PCI-X Slot Power Select (JP9)

With the jumper set can provide 3.3V or 5V to PCI-X add-on card.

Table 2.10: PCI-X VIO Select Connector	
Close pins	Result
1-2	3.3V
2-3	5V

*: Default value (5V)

2.14 DVO or AGP Alternative Setting (JP10)

This board cannot support DVO and AGP at the same time. User can set the DVO or AGP using this jumper setting.

Table 2.11: DVO /AGP	
Close pins	Result
1-2	OPEN (DVO) CLOSE (AGP)

*: Default value DVO (OPEN)

2.15 Clear CMOS

Action to erase CMOS data.

Warning! *To avoid damaging the computer, always turn off the power supply before setting "Clear CMOS" Before turning on the power supply, set the jumper back to "3.0V Battery On".*

This jumper is used to erase CMOS data (including the setting of date, time and password) and reset system BIOS information.

The procedure for clearing CMOS is:

1. Turn off the system.
2. Short pin 1 and pin 2.
3. Turn on the system. The BIOS is now reset to its default setting.

2.16 Installing DIMMs

Notes *The modules can only fit into a socket one way. The gold pins must point down into the DIMM socket.*

The procedure for installing DIMMs appears below. Please follow these steps carefully.

1. Make sure that all power supplies to the system are switched off
2. Install the DIMM card. Install the DIMM so that its gold pins

point down into the DIMM socket.

3. Slip the DIMM module perpendicular into the socket, apply more pressure until the clips fix the DIMM and socket securely.

4. Check to ensure that the DIMM is correctly seated and all connector contacts touch. The DIMM should not move around in its socket.

2.17 ATX power control connector (ATX1)

The AIMB-350 supports ATX power. ATX1 supplies main power (+5V, +12V, 5VSB), and it is a 20-Pin power connector, w/Fixed Lock.

Important *Make sure that the ATX power supply can take at least a 10 mA load on the 5 V standby lead (5VSB). If not, you may have difficulty powering on your system.*

2.18 Printer port connector (CN3)

Normally, the parallel port is used to connect the card to a printer. The AIMB-350 includes a multi-mode (ECP/EPP/SPP) parallel port accessed via CN3 and a D-SUB 25-pin connector.

The parallel port interrupt channel is designated to be IRQ7.

You can select ECP/EPP DMA channel via BIOS setup.

2.19 CompactFlash Card Socket

The AIMB-350 provides a 50-pin socket for CompactFlash card type I/II.

2.19.1 CompactFlash(CN16)

The CompactFlash card occupies a secondary IDE channel which can be enabled/disabled via the BIOS settings.

2.20 Floppy drive connector (CN20)

You can attach up to two floppy drives to the AIMB-350's onboard controller. You can use any combination of 5.25" (360 KB and 1.2 MB) and/or 3.5" (720 KB, 1.44 MB, and 2.88 MB) drives.

A 34-pin daisy-chain drive connector cable is required for a dual-drive system. On one end of the cable is a 34-pin flat-cable connector. On the other end are two sets of floppy disk drive connectors. Each set consists of a 34-pin flat-cable connector (usually used for 3.5” drives) and a printed-circuit board connector (usually used for 5.25” drives).

2.20.1 Connecting the floppy drive

1. Plug the 34-pin flat-cable connector into CN20. Make sure that the red wire corresponds to pin one on the connector.
2. Attach the appropriate connector on the other end of the cable to the floppy drive(s). You can use only one connector in the set. The set on the end (after the twist in the cable) connects to the A: drive. The set in the middle connects to the B: drive.
3. If you are connecting a 5.25” floppy drive, line up the slot in the printed circuit board with the blocked-off part of the cable connector.

If you are connecting a 3.5” floppy drive, you may have trouble determining which pin is number one. Look for a number printed on the circuit board indicating pin number one. In addition, the connector on the floppy drive may have a slot. When the slot is up, pin number one should be on the right. Check the documentation that came with the drive for more information.

If you desire, connect the B: drive to the connectors in the middle of the cable as described above.

In case you need to make your own cable, you can find the pin assignments for the board’s connector in Appendix B.

2.21 IDE connector(CN17,CN18)

The AIMB-350 provides two IDE channels to which you can attach up to four Enhanced Integrated Device Electronics hard disk drives or CDROM to the AIMB-350’s internal controller. The AIMB-350's IDE controller uses a PCI interface. This advanced IDE controller supports faster data transfer, PIO Mode 3 or Mode 4, UDMA 33/66/100 mode.

2.21.1 Connecting the hard drive

Connecting drives is done in a daisy-chain fashion. It requires one of two cables (not included in this package), depending on the drive size. 1.8" and 2.5" drives need a 1 x 44-pin to 2 x 44-pin flat-cable connector. 3.5" drives use a 1 x 44-pin to 2 x 40-pin connector.

Wire number 1 on the cable is red or blue, and the other wires are gray.

1. Connect one end of the cable to CN17,CN18. Make sure that the red (or blue) wire corresponds to pin 1 on the connector, which is labeled on the board (on the right side).
2. Plug the other end of the cable into the Enhanced IDE hard drive, with pin 1 on the cable corresponding to pin 1 on the hard drive. (See your hard drive's documentation for the location of the connector.)

If desired, connect a second drive as described above.

Unlike floppy drives, IDE hard drives can connect to either end of the cable. If you install two drives, you will need to set one as the master and one as the slave by using jumpers on the drives. If you install only one drive, set it as the master.

2.22 VGA/LVDS interface connections

The AIMB-350's display interface can drive conventional CRT displays and is capable of driving a wide range of LVDS flat panel displays as well. The board has two display connectors: one for standard CRT VGA monitors, and one for LVDS/DVI flat panel displays. AIMB-350 with 852GME can support dual independent displays like CRT+LVDS or CRT+DVI.

2.22.1 CRT display connector (CN1)

CN1 is a standard 15-pin connector used for conventional CRT displays. Users can drive a standard progressive scan analog monitor with pixel resolution up to 2048 x 1536 at 75 Hz. Pin assignments for CRT display connector CN1 are detailed in Appendix B.

2.22.2 LVDS LCD panel connector(CN11,VCN1)

AIMB-350 uses the Intel 855GME to supports single or dual-channel LVDS panels up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz.

The display mode can be 2 channels (2 x 24bit) LVDS LCD panel displays Users can connector to either an 18, 24, 36 LVDS with VCN1 and LCD with CN11.

2.22.3 LCD inverter connector(CN8)

The LCD inverter is connected to CN8 via a 5-pin connector to provide +5V/+12V power.

2.22.4 DVI connector (CN12)

Digital Visual Interface (DVI) is the standard interface for high-performance connection between PCs and Flat Panel Displays, Digital CRT displays, Projectors, and HDTV. AIMB-350 is able to drive a DVI connector display at a pixel rate of up to 165MHz, supporting UXGA resolution displays and hot plug detection. DVI can connect with PCM-258 to have standard DVI connector.

2.23 USB connectors (CN6,CN7,CN13,CN14)

The AIMB-350 board provides up to eight USB (Universal Serial Bus) ports. This gives complete Plug and Play, and hot attach/detach for up to **127** external devices. The USB interfaces comply with USB specification Rev. 2.0, and are fuse protected.

There are 4 USB connectors for external and 4 USB for internal use. The 4 external USBs are combine with LAN+2 USB in CN6 and CN7. The internal USB interfaces are accessed through the 5 x 2-pin flat-cable connectors, CN13 (USB7, 8) and CN14 (USB5, 6). You will need an adapter cable if you use a standard USB connector. The adapter cable has a 5 x 2-pin connector on one end and a USB connector on the other. The USB interfaces can be disabled in the system BIOS setup.

2.24 Ethernet configuration

The AIMB-350 is equipped with two high performance 32-bit PCI-bus Ethernet interfaces which are fully compliant with IEEE 802.3U 10/100Mbps CSMA/CD standards. These are supported by all major network operating systems.

The AIMB-640 supports 2 x 10/100Base-T or 2 x 1000Base-T Ethernet connections with onboard RJ-45 connectors (CN6, CN7). AIMB-350M/AIMB-350L series supports 10/100Base-T LAN, AIMB-350F series supports 1000Base-T LAN.

2.24.1 LAN connector (CN6,CN7)

10/100 or 1000 Base-T connects are standard RJ45 connectors on AIMB-350.

2.24.2 Network boot

The Network Boot feature can be utilized by incorporating the Boot ROM image files for the appropriate network operating system. The Boot ROM BIOS files are included in the system BIOS, which is on the utility

CD disc. Boot ROM function is supported by 82541GI and 82551QM(optional), 82551ER can not support this function.

2.25 Front Panel Connector (JP4)

Next is to install external switches to monitor and control AIMB-350. These features are optional: install them only if necessary. JP4 is an 2 x 7 pin header, 180 degree, male. It provides connections for reset, power, and hard disk indicator.

2.25.1 Reset (Pin13&Pin14)

If a reset switch is installed, it should be an open single pole switch. Momentarily pressing the switch will activate a reset. The switch should be rated for 10 mA, 5V.

2.25.2 HDD LED (Pin1&Pin2)

The HDD LED indicator for hard disk access is an active low signal (24 mA sink rate). The HDD LED indicator lights up when the HDD is reading or writing.

2.25.3 Power LED (Pin 3 & Pin 4)

The Power LED indicator lights up when the power is on.

2.25.4 Suspend LED (Pin 5 & Pin 6)

The Suspend LED indicator lights up when the computer is in suspend.

2.25.5 Power Button (Pin 9 & Pin10)

AIMB-350 provides an ATX power input connector. When connected with PIN 9 & PIN 10, it enables power On/Off from the chassis.

2.26 COM port connector (CN2,CN21,CN22)

The AIMB-350 provides six serial ports (COM1,COM3~COM6: RS-232 and COM2: RS-232/RS-422/RS-485). CN2 supports COM1 with D-SUB 9-Pin standard connector, CN21 supports COM2, CN22 supports COM3~6,. and JP6 is for COM2 RS-232/RS-422/RS-485 selection. It provides connections for serial devices (a mouse, etc.) or a communication network. You can find the pin assignments for the COM port connector in Appendix B.

2.27 MINI PS/2, KB/Mouse connector (CN5)

The AIMB-350 board provides a keyboard connector that supports both a keyboard and a PS/2 style mouse. In most cases, especially in embedded applications, a keyboard is not used. If the keyboard is not present, the standard PC/AT BIOS will report an error or fail during power-on self-test (POST) after a reset. The AIMB-350's BIOS standard setup menu allows you to select "All, but Keyboard" under the "Halt On"selection. This allows no-keyboard operation in embedded system applications, without the system halting under POST.

2.28 Audio Connector (CN4)

AIMB-350 can support AC97 2.2 compliant Audio line_in, line_out and mic_in with on board standard connector.

2.29 DI/O connector (CN23)

The AIMB-350 supports DIO interface with CN23, which is a 2 x 8 dual line pin header, supplying 8 general purpose input or output ports.

One characteristic of digital circuit are their fast response to high or low signals, the kind of responses that are needed for harsh and critical industrial operating environments.

Generally, Digital Input and Output are signals to control external devices that needs On/Off circuits or TTL devices. For detailed signal assignments refer to Appendix A.

2.30 SATA Connector (SA1, SA2)

AIMB-350 can support Serial ATA by two COMAX C504C connectors (SA1, SA2), data transfer rates up to 150 Mbyte/s, enabling very fast data and file transfer, and independent DMA operation on two ports. It also supports alternate Device ID and RAID Class Code options for support of Soft RAID.

2.31 CD-In Connector (CN9)

AIMB-350 has a CD-In connector for the CD-ROM driver audio signal interface. CD-In connector is a 2.54mm pitch 4 pin connector.

2.32 Internal Speaker Connector (CN10)

There is a Wafer-Box 4-Pin 2.54 mm connector for the internal speaker purpose.

2.33 SIR Connector (CN15)

This connector support wireless 115.2 Kbps infrared transmission and receive mode.The IR module should mount on system case. It is a 5 pin connector.

2.34 SM Bus Connector (CN19)

The System Management Bus (SM Bus) which uses 12C bus to make a communication between the South Bridge and the rest of the system. In AIMB-350 the South Bridge is dedicated to one PCI slot. The other will handle the remaining I2C buses to other on-board devices such as the PCI, PCI-X1, PCI-X2, LAN1 and LAN2.

2.35 System and CPU FAN Conn. (FAN1 and FAN2)

These 2 FAN connectors both have +12V FAN power and FAN speed detection. AIMB-350 recommends FAN1 for system FAN and FAN2 for CPU.

2.36 AGP,PCI, PCI-X Conn(AGP1, PCI1, PCIX1, PCIX2)

These 4 connectors all follow standards. AIMB-350M has 4 x AGP slots, 1 x PCI, and 1 PCI-X. AIMB-350F-00A1 has PCI-X and AIMB-350L also has PCI-X.

CHAPTER 3

Software Configuration

This chapter details the software configuration information. It shows you how to configure the card to match your application requirements. Award System BIOS will be covered in Chapter 4.

Sections include:

- Introduction
- VGA display software configuration
- Connectors to Standard LCDs

Chapter 3 Software Configuration

3.1 Introduction

The system BIOS and custom drivers are located on a 512 KB, 32-pin (JEDEC spec.) Flash ROM device, designated U10. A single Flash chip holds the system BIOS, VGA BIOS, and network Boot ROM image. The display can be configured via software. This method minimizes the number of chips and eases configuration. You can change the display BIOS simply by reprogramming the Flash chip.

NOTE: Due to Intel not supporting Win98, and Windows ME drivers, AIMB-350 does not recommended installing Win98, Windows ME.

3.2 VGA display firmware configuration

The board's onboard VGA interface supports a wide range of popular LCDs, flat panel displays and traditional analog CRT monitors. The 855GME chip with optimized Shared Memory Architecture, supports up to 64 MB frame buffer using system memory to provide LVDS mode up to 1280 x 1024 @ 48bpp, the interface can drive CRT displays with resolutions up to 2048 x 1536 @ 24bpp (75Hz).

The VGA interface is configured completely via the software utility, so you do not have to set any jumpers. Configure the VGA display as follows:

1. Apply power to the board with a color TFT display attached. This is the default setting for this board. Ensure that the AWDFLASH.EXE and *.BIN files are located in the working drive.

NOTE: Ensure that you do not run AWDFLASH.EXE while your system is operating in EMM386 mode.

2. At the prompt, type AWDFLASH.EXE and press <Enter>. The VGA configuration program will then display the following:

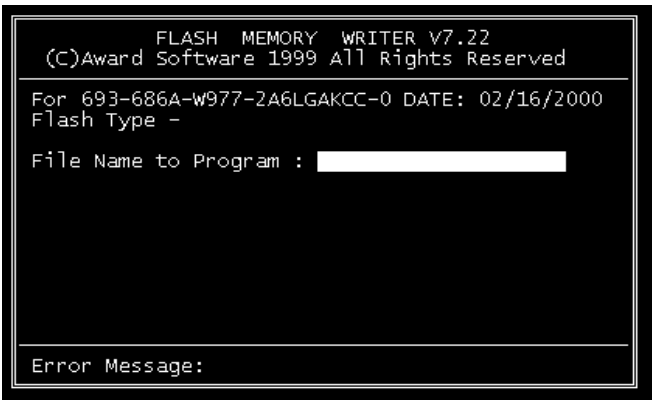


Figure 3.1: VGA setup screen

3. At the prompt, enter the new BIN file which supports your display. When you are sure that you have entered the file name correctly press <Enter>.
4. The screen will ask “Do you want to save BIOS?”. If you change your mind or have made a mistake, press N to abort and end the setup procedure. Press Y if you wish to save the existing configuration before changing it. Then type the name under which you want to save the current configuration.
5. The prompt will then ask “Are you sure?”. Press Y if you want the new file to be written into the BIOS. Press N to exit the program.

The new VGA configuration will then write to the ROM BIOS chip. This configuration will remain the same until you run the AWDFLASH.EXE program and change the settings.

3.3 Connectors to Standard LCDs

The following table illustrates typical LCD connection pinouts for the AIMB-350.

3.3.1 AU M170EG01(1280 x1024 LVDS LCD)

Table 3.1: Connections to LCD/Flat Panel (CN15)

LCD Connector		Flat Panel Connector	
JAE FI-X30C2L		DF13-40P	
Pin	**Signal**	**Pin**	**Signal**
1	RxOIN0-	7	OD0-
2	RxOIN0+	9	OD0+
3	RxOIN1-	13	OD1-
4	RxOIN1+	15	OD1+
5	RxOIN2-	19	OD2-
6	RxOIN2+	21	OD2+
7	VSS	23	GND
8	RxOCLKIN-	25	OCK-
9	RxOCLKIN+	27	OCK+
10	RxOIN3-	35	OD3-
11	RxOIN3+	37	OD3+
12	RxEIN0-	8	ED0-
13	RxEIN0+	10	ED0+
14	VSS	4	WP#
15	RxEIN1-	14	ED1-
16	RxEIN1+	16	ED1+
17	VSS	12	GND
18	RxEIN2-	20	ED2-
19	RxEIN2+	22	ED2+
20	RxECLKIN-	26	ECK-
21	RxECLKIN+	28	ECK+
22	RxEIN3-	36	ED3-
23	RxEIN3+	38	ED3+
24	VSS	34	GND
25	VSS	30	GND
26	NC	X	
27	VSS	34	GND
28	VCC	1	VDDSAFE
29	VCC	2	VDDSAFE

CHAPTER 4

Award BIOS Setup

This chapter describes how to set BIOS configuration data.

Chapter 4 Award BIOS Setup

4.1 System test and initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors. Non-fatal error messages usually appear on the screen along with the following instructions:

```
press <F1> to CONTINUE
```

Write down the message and press the F1 key to continue the bootup sequence.

4.1.1 System configuration verification

These routines check the current system configuration against the values stored in the board's CMOS memory. If they do not match, the program outputs an error message. You will then need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The CMOS memory has lost power and the configuration information has been erased.

The AIMB-350 Series' CMOS memory has an integral lithium battery backup. The battery backup should at least three years in normal service, but when it finally runs down, you will need to replace the complete unit.

4.2 Award BIOS setup

Award's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains the Setup information when the power is turned off.

4.2.1 Entering setup

Power on the computer and press <Del> immediately. This will allow you to enter Setup.

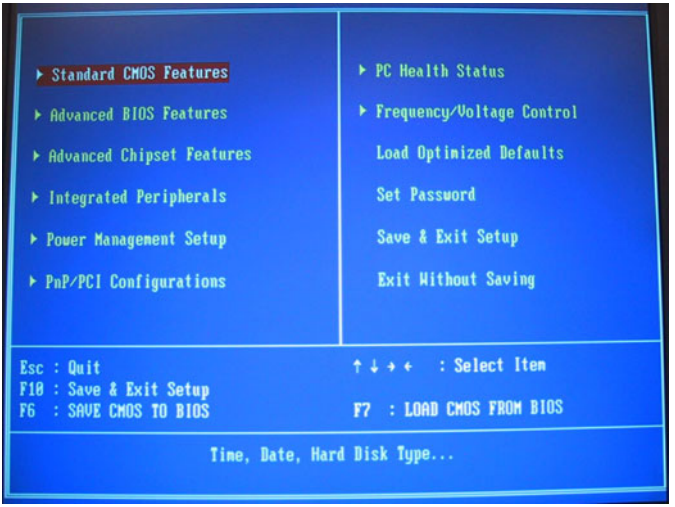


Figure 4.1: BIOS setup program initial screen

4.2.2 Standard CMOS Features setup

When you choose the Standard CMOS Features option from the Initial Setup Screen menu, the screen shown below is displayed. This standard Setup Menu allows users to configure system components such as date, time, hard disk drive, floppy drive and display. Once a field is highlighted, online help information is displayed in the right top of the Menu screen.

Figure 4.2: Standard CMOS Features setup

4.2.3 Advanced BIOS Features setup

By choosing the Advanced BIOS Features Setup option from the Initial Setup Screen menu, the screen below is displayed. This sample screen contains the manufacturer's default values for the AIMB-350 Series.

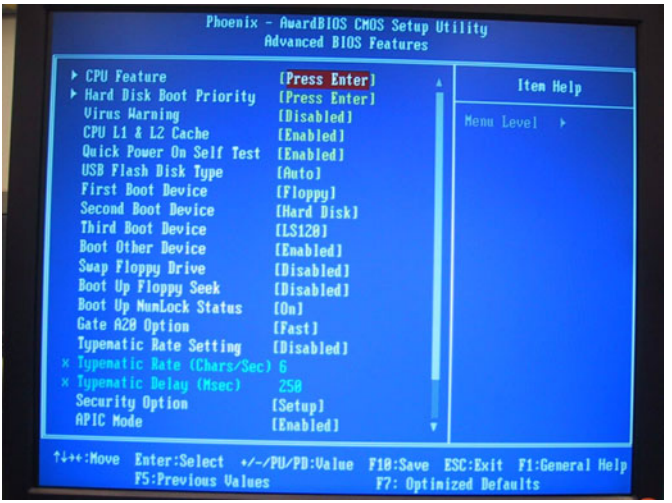


Figure 4.3: Advanced BIOS Features setup

4.2.4 Advanced Chipset Features setup

By choosing the Advanced Chipset Features option from the Initial Setup Screen menu, the screen below is displayed. This sample screen contains the manufacturer's default values for the AIMB-350 Series.

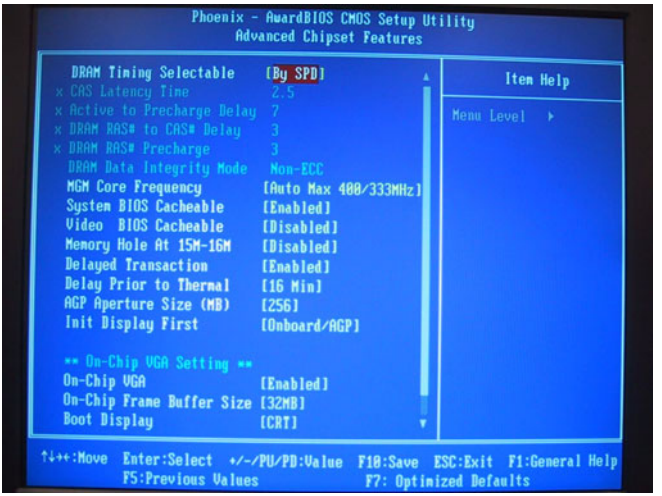


Figure 4.4: Advanced Chipset Features setup

4.2.5 Integrated Peripherals

Choosing the Integrated Peripherals option from the Initial Setup Screen menu should produce the screen below. Here we see the manufacturer's default values for the AIMB-350 Series.

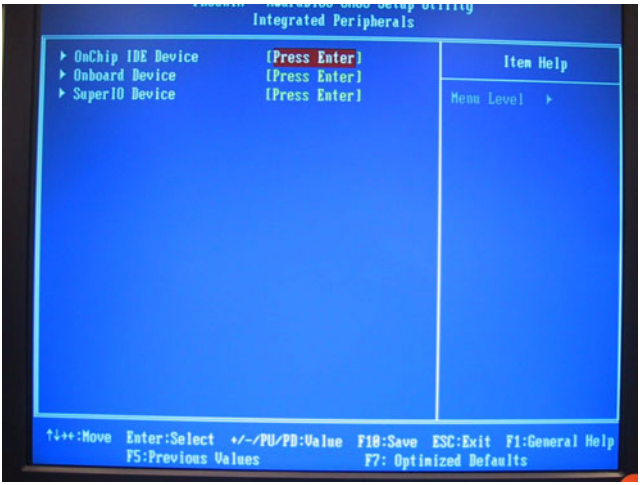


Figure 4.5: Integrated Peripherals

4.2.6 Power Management Setup

By choosing the Power Management Setup option from the Initial Setup Screen menu, the screen below is displayed. This sample screen contains the manufacturer's default values for the AIMB-350 Series.

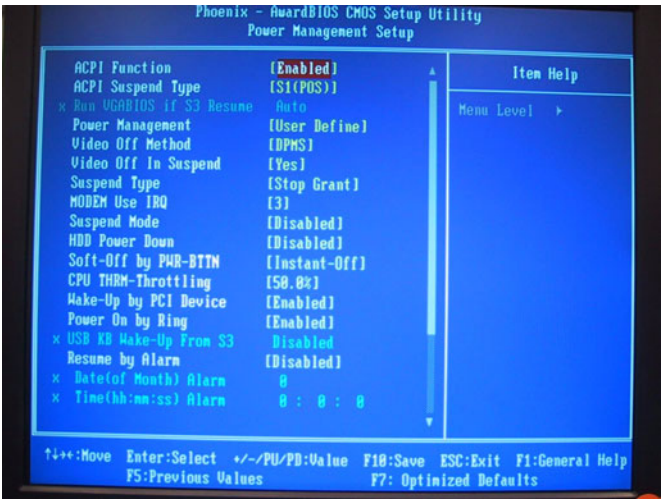


Figure 4.6: Power Management Setup

4.2.7 PnP/PCI Configurations

By choosing the PnP/PCI Configurations option from the Initial Setup Screen menu, the screen below is displayed. This sample screen contains the manufacturer's default values for the AIMB-350 Series.

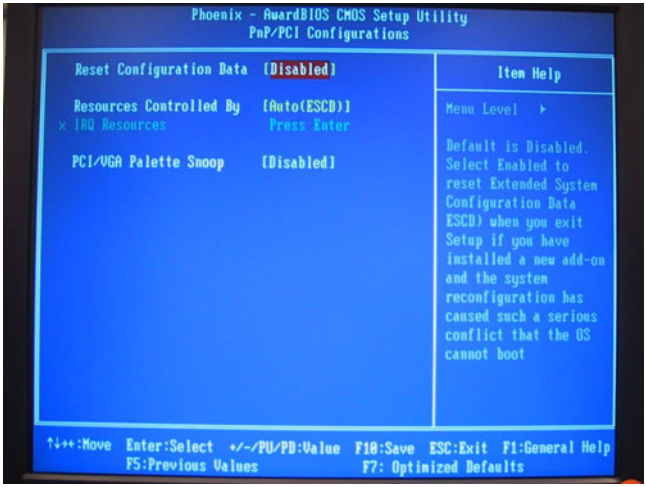


Figure 4.7: PnP/PCI Configurations

4.2.8 PC Health Status

The PC Health Status option displays information such as CPU and motherboard temperatures, fan speeds, and core voltage.

Figure 4.8: PC Health Status

4.2.9 Frequency/Voltage Control

By choosing the Frequency/Voltage Control option from the Initial Setup Screen menu, the screen below is displayed. This sample screen contains the manufacturer's default values for the AIMB-350

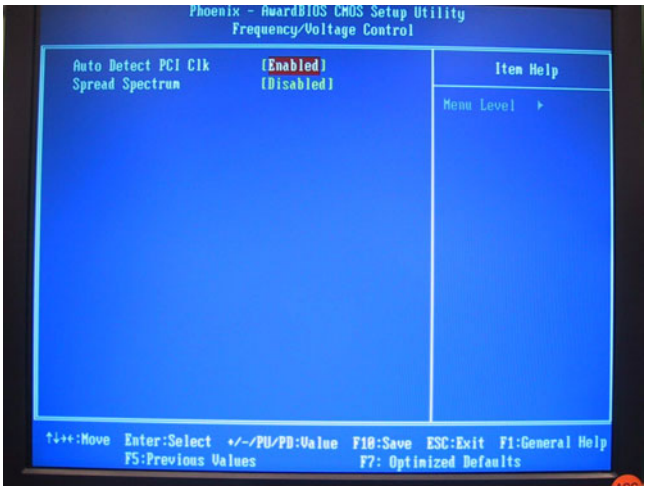


Figure 4.9: Frequency/Voltage Control

Caution *Incorrect settings in Frequency/Voltage Control may damage the system CPU, video adapter, or other hardware.*

4.2.10 Load Optimized Defaults

Load Optimized Defaults loads the default system values directly from ROM. If the stored record created by the Setup program should ever become corrupted (and therefore unusable), these defaults will load automatically when you turn the AIMB-350 Series system on.

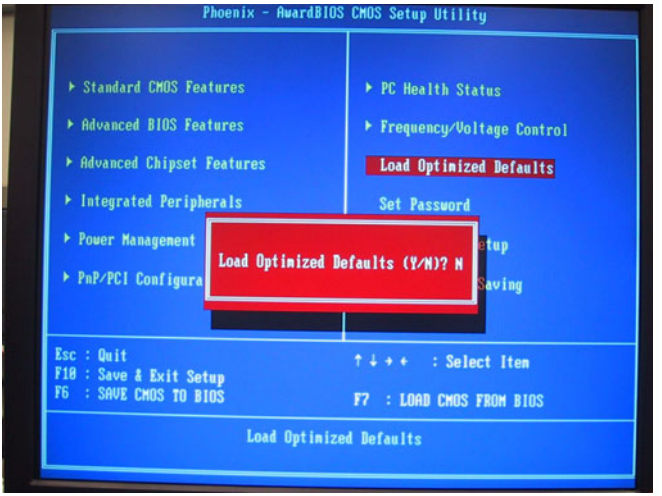


Figure 4.10: Load BIOS defaults screen

4.2.11 Set Password

Note *To enable this feature, you should first go to the Advanced BIOS Features menu, choose the Security Option, and select either Setup or System, depending on which aspect you want password protected. Setup requires a password only to enter Setup. System requires the password either to enter Setup or to boot the system. A password may be at most 8 characters long.*

To Establish a Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see “Enter Password,” enter the desired password and press <Enter>.
3. At the “Confirm Password” prompt, retype the desired password, then press <Enter>.
4. Select Save to CMOS and EXIT, type <Y>, then <Enter>.

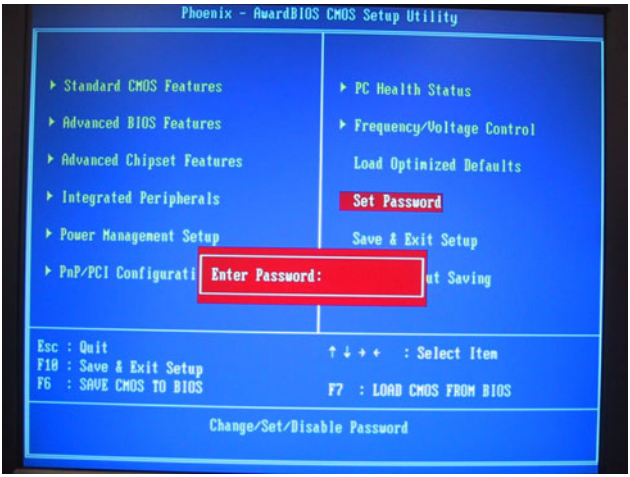


Figure 4.11: Set password

To Change a Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see “Enter Password,” enter the existing password and press <Enter>.
3. You will see “Confirm Password.” Type it again, and press <Enter>.
4. Select Set Password again, and at the “Enter Password” prompt, enter the new password and press <Enter>.

5. At the “Confirm Password” prompt, retype the new password, and press <Enter>.
6. Select Save to CMOS and EXIT, type <Y>, then <Enter>.

To Disable Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see “Enter Password,” enter the existing password and press <Enter>.
3. You will see “Confirm Password.” Type it again, and press <Enter>.
4. Select Set Password again, and at the “Enter Password” prompt, don’t enter anything; just press <Enter>.
5. At the “Confirm Password” prompt, again don’t type in anything; just press <Enter>.
6. Select Save to CMOS and EXIT, type <Y>, then <Enter>.

4.2.12 Save & Exit Setup

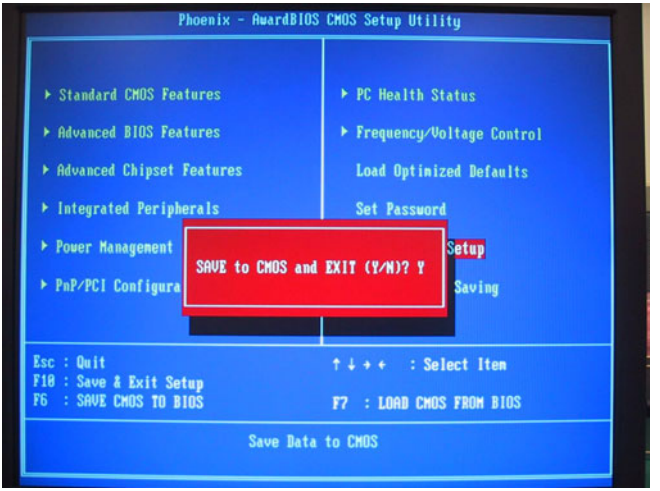


Figure 4.12: Save to CMOS and EXIT

If you select this option and press <Y> then <Enter>, the values entered in the setup utilities will be recorded in the chipset's CMOS memory. The microprocessor will check this every time you turn your system on and use the settings to configure the system. This record is required for the system to operate.

4.2.13 Exit Without Saving

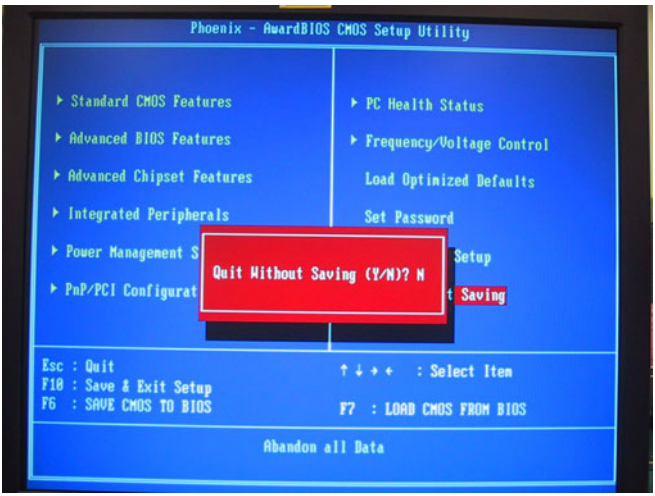


Figure 4.13: Quit without saving

Selecting this option and pressing <Enter> lets you exit the Setup program without recording any new values or changing old ones.

CHAPTER 5

PCI SVGA Setup

Introduction

Installation of SVGA drivers

-for Windows 2000/XP

Further information

Chapter 5 PCI SVGA Setup

5.1 Introduction

The board has an onboard interface. The specifications and features are described as follows:

5.1.1 Chipset

The AIMB-350 uses an Intel 855GME + 6300ESB chipset for its graphic controller. It supports LVDS LCD displays, conventional CRT monitors.

5.1.2 Display memory

The 855GME chip with optimized Shared Memory Architecture, supports up to 64 MB frame buffer using system memory to provide LVDS mode up to 1280 x 1024 @ 48bpp with frequency range from 25 MHz to 112 MHz. the interface can drive CRT displays with resolutions up to 2048 x 1536 @ 24 bpp 75 Hz.

5.1.3 Display types

CRT and panel displays can be used simultaneously. The board can be set in one of three configurations: on a CRT, on a flat panel display, or on both simultaneously. The system is initially set to simultaneous display mode. If you want to enable the CRT display only or the flat panel display only, please contact Intel Corporation LTD., or our sales representative for detailed information.

Notes: *Due to Intel not supporting Win98, and Windows ME drivers, AIMB-350 does not recommended installing Win98 or Windows ME.*

5.2 Installation of the SVGA Driver

Complete the following steps to install the SVGA driver. Follow the procedures in the flowchart that apply to the operating system that you are using within your board.

Notes:

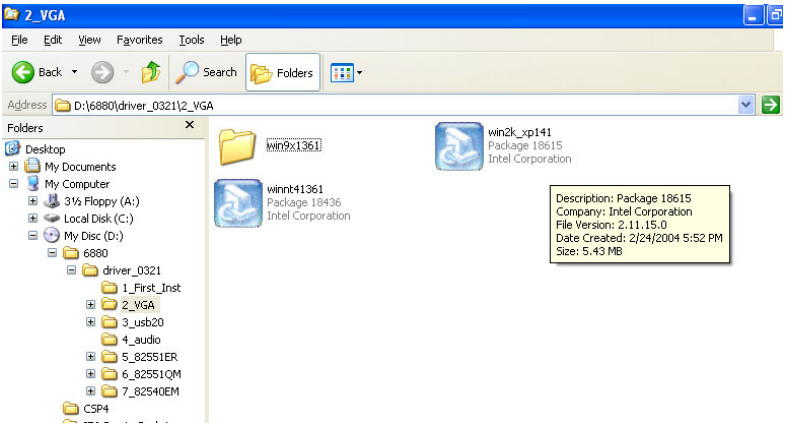
1. The windows illustrations in this chapter are intended as examples only. Please follow the listed steps, and pay attention to the instructions which appear on your screen.

2. For convenience, the CD-ROM drive is designated as "D" throughout this chapter.

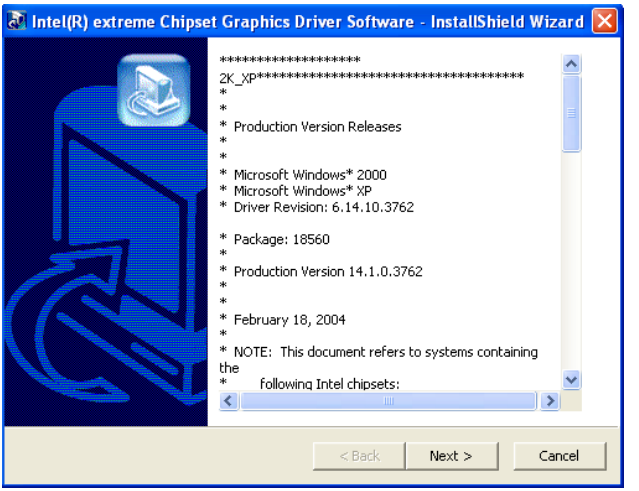
5.2.1 Installation for Windows 2000/XP

To install SVGA driver for Window 2000/XP, please run the setup wizard "Intel Extreme Graphic 2" in CD-ROM. Example of installation is shown as bellow:

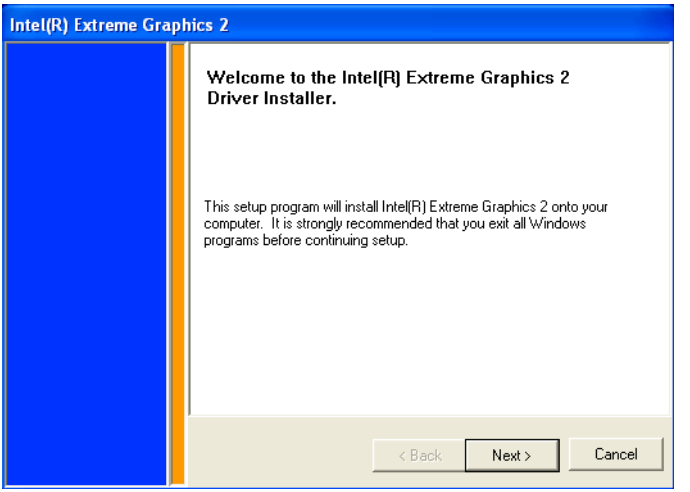
1. Select the path: D:\2_VGA, then double click "win2k_xp141" to run "Install Shield Wizard"



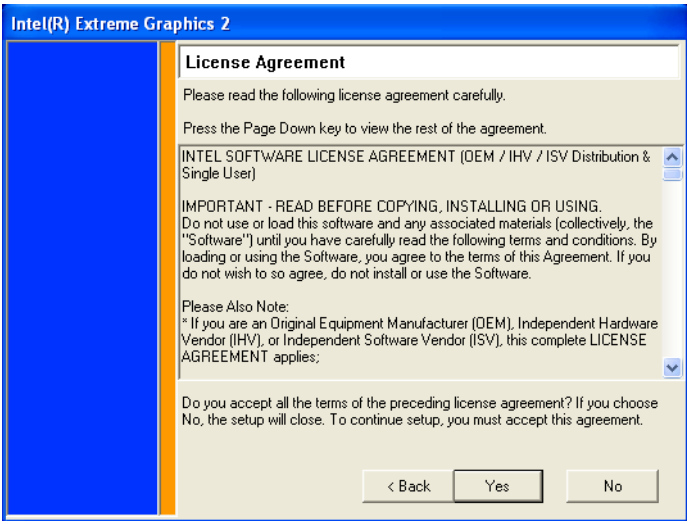
2. Press the "Next" button.



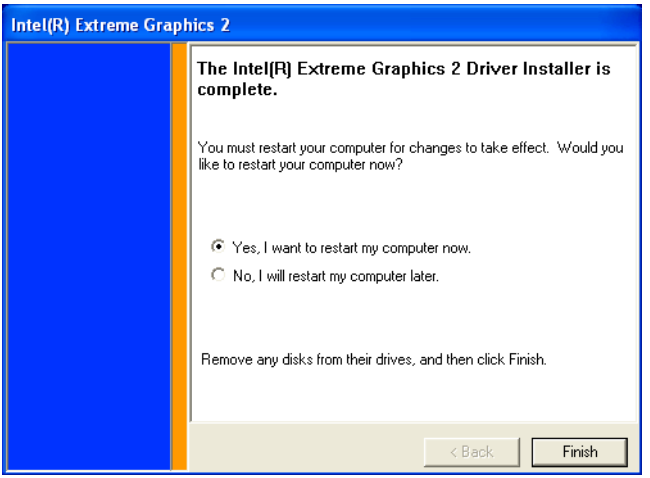
3. Press the "Next" button.



4. In order to continue setup, you must accept the agreement, press the "Yes" button and wait a minute.



5. Choose the option "Yes, I want to restart my computer now." and press the "Finish" button.



5.3 Further Information

For further information about the AGP/VGA installation in your AIMB-350, including driver updates, troubleshooting guides and FAQ lists, visit the following web resources:

Intel website:	www.intel.com.
Advantech websites:	www.advantech.com www.advantech.com.tw

CHAPTER 6

PCI Bus Ethernet Interface

This chapter provides information on Ethernet configuration.

- Introduction
- Installation of Ethernet drivers for Windows XP
- Further information

Chapter 6 PCI Bus Ethernet Interface

6.1 Introduction

The board is equipped with two high performance 32-bit Ethernet chipsets which are fully compliant with 802.3u 100BASE-T or 802.3z/ab 1000BASE-T.

The Ethernet port provides a standard RJ-45 jack. The network boot feature can be utilized by incorporating the boot ROM image files for the appropriate network operating system. The boot ROM BIOS files are combined with system BIOS, which can be enabled/disabled in the BIOS setup.

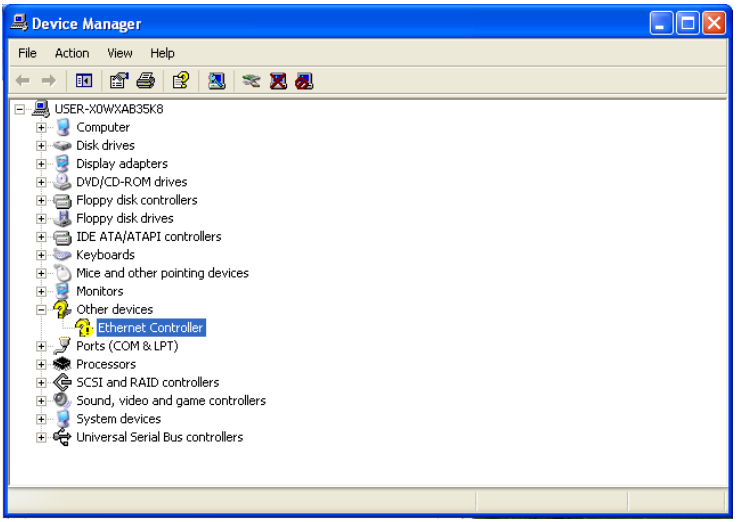
6.2 Installation of Ethernet driver

Before installing the Ethernet driver, note the procedures below. You must know which operating system you are using in your board series, and then refer to the corresponding installation flowchart. Then just follow the steps described in following procedure.

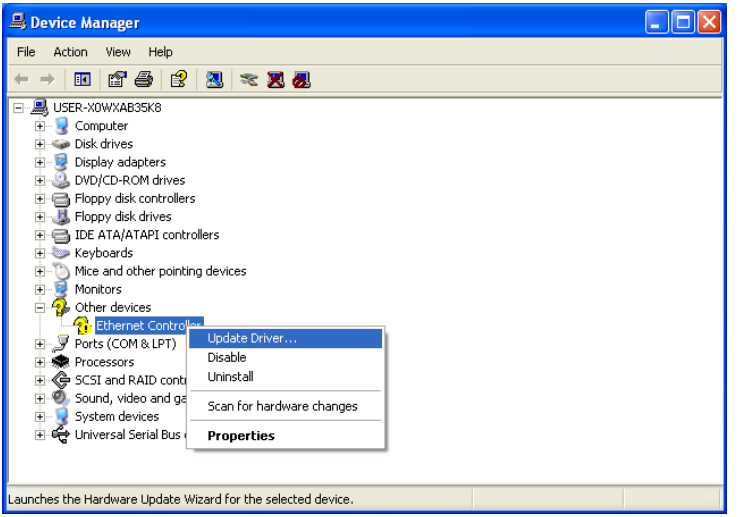
Note: The windows illustrations in this chapter are examples only. Follow the steps and pay attention to the instructions which appear on your screen.

6.2.1 Installation Fast Ethernet (10/100Mbps Intel 82551) for Windows XP

1. Select “Ethernet Controller” from Device Manager.

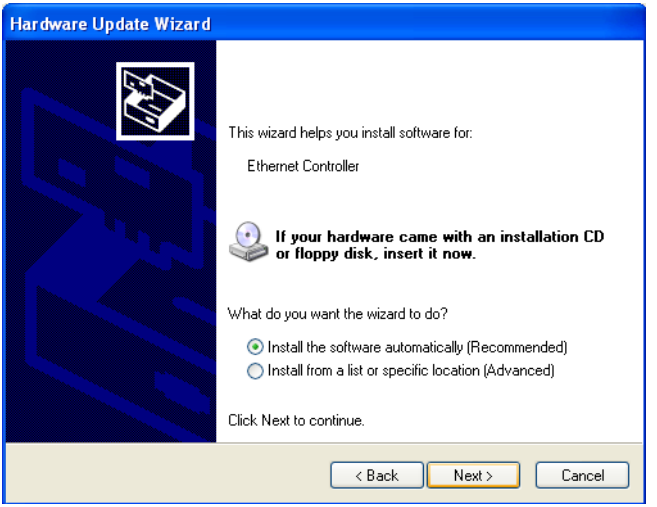


2. Select “Update Driver”.

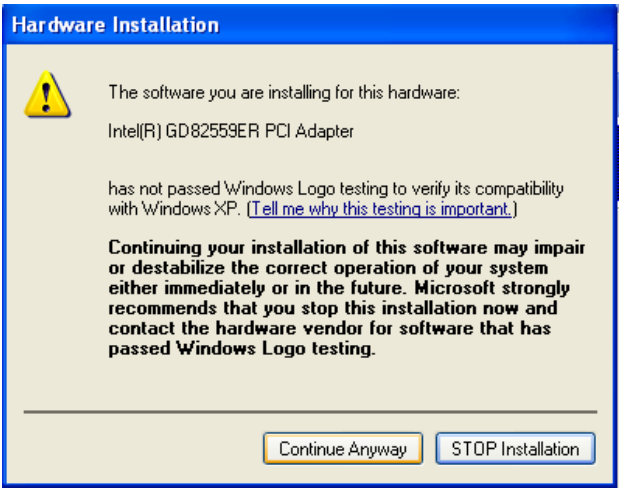


3. Click the “Next” button.

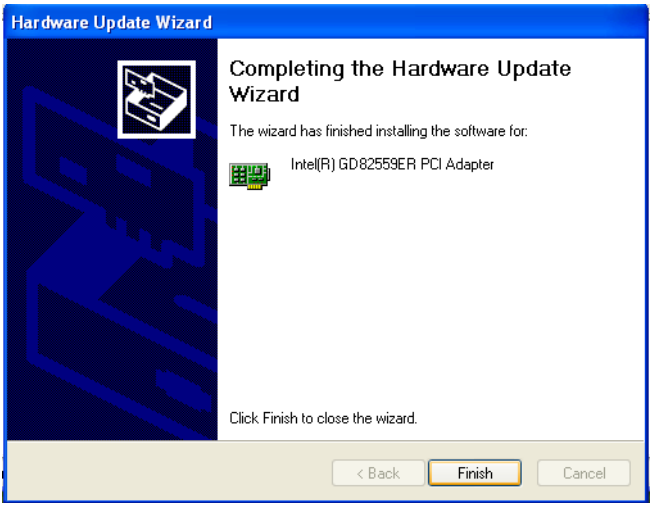
4. Click the “Next” button.



5. Please choose “Continue Anyway”.

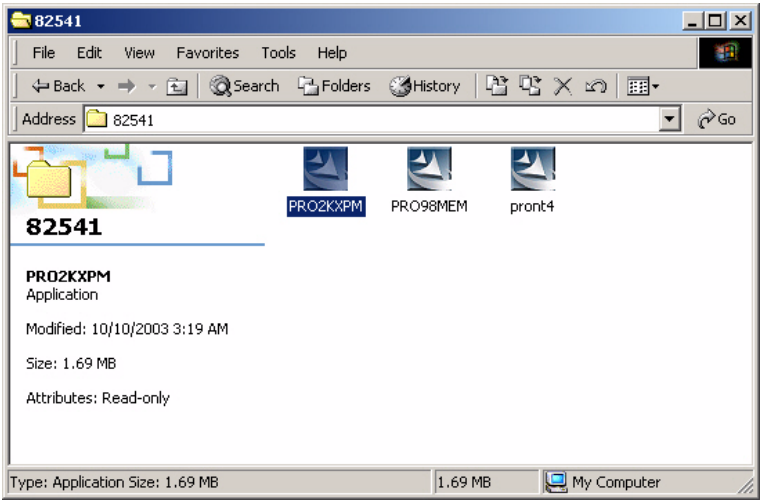


6. Click the “Finish” button



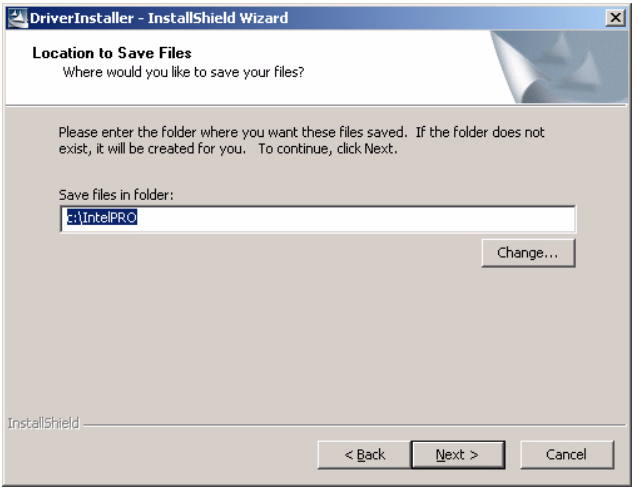
6.2.2 Installation Gigabit Ethernet (10/100/1000Mbps intel 82541) for Windows XP

1. Select Driver from Driver CD, and click from 82541 directory "PRO2KXPM" intel driver installer program. (Ex: E:\AIMB-350\LAN\82541GI\PRO2KXPM).



2. Read the "License Agreement" carefully, select "I accept the items in the license agreement." then click "Next>" go to next step.

3. Select the location to save Driver Installer file, default is: C:\Intel-PRO.



4. Click the “Install Base Driver” to install 82541 Gigabit LAN driver.

5. Intel Driver Installer will install driver automatically.

6. The "Found New Hardware" box will pop on the screen, then the driver install has completed.

CHAPTER 7

Audio Setup

- Introduction
- Installation of audio driver for Windows XP

Chapter 7 Audio Setup

7.1 Introduction

The AIMB-350 supports AC97 audio.

7.2 Driver installation

7.2.1 Before you begin

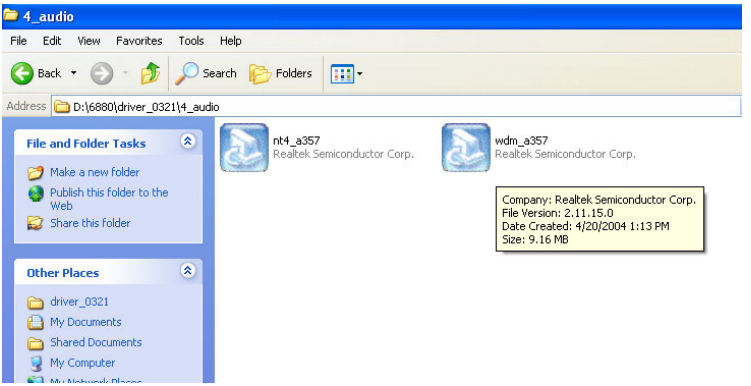
Please read the instructions in this chapter carefully before you attempt installation. The audio drivers for the AIMB-350 board are located on the audio driver CD. Run the supplied SETUP program to install the drivers; don't copy the files manually.

Note: The files on the software installation diskette are compressed. Do not attempt to install the drivers by copying the files manually. You must use the supplied SETUP program to install the drivers.

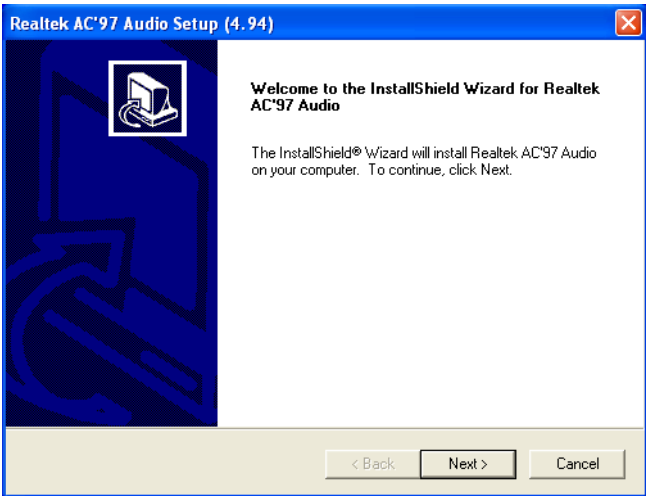
7.2.2 Windows XP driver

To install audio drivers for Window XP, please run the setup wizard on the CD-ROM. An example installation is shown below:

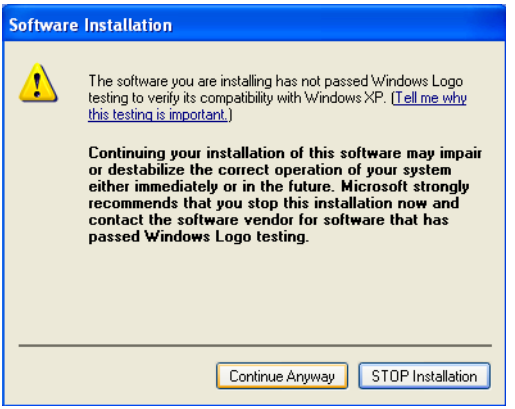
1. Select the path: D:\wdm_a357, then double click to run "Install Shield Wizard".



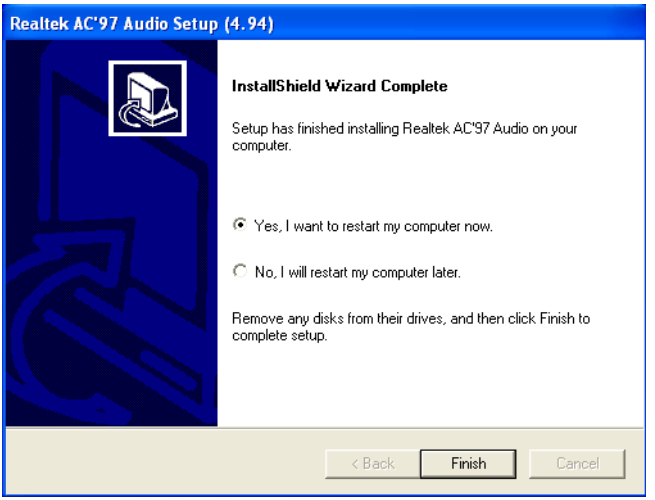
2. Press the "Next" button and wait for a moment.



3. Choose the option "Continue Anyway".



4. Choose the option "Yes, I want to restart my computer now", then click "Finish" button to reboot your computer.



Appendix A

Programming GPIO & Watchdog Timer

The board is equipped with a watchdog timer that resets the CPU if processing comes to a standstill for any reason. This feature ensures system reliability in industrial standalone or unmanned environments.

Appendix A Programming GPIO & Watchdog Timer

A.1 Supported GPIO Register

Bellow are detailed description of the GPIO addresses and programming sample.

A.1.1 GPIO Registers

CRF0 (GP10-GP17 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP10-GP17 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

Extended Function Index Registers (EFIRs)

The EFIRs are write-only registers with port address 2Eh or 4Eh on PC/AT systems.

Extended Function Data Registers (EFDRs)

the EFDRs are read/write registers with port address 2Fh or 4Fh on PC/AT systems.

A.1.2 GPIO Example program-1

```
------------------------------------------------
/* Winbond 83627*/
 #include <dos.h>
 #include <conio.h>
#include <stdio.h>
#define SuperIO_A0          0x2E
#define SuperIO_A1          0x2F
#define DIO_A0               0x300
void main()
{
    unsigned Temp;
    unsigned ErrFlag;
    ErrFlag=0;
   clrscr();
   /*---Winbond W83627--*/
  outportb(SuperIO_A0, 0x87); /* External Function (Two Successive
writes of 0x87)*/
outportb(SuperIO_A0, 0x87); /* External Function (Two Successive
writes of 0x87)*/
/*--Global CR20--*/
outportb(SuperIO_A0, 0x20);
Temp-inportb(SuperIO_a1); /*Temp must be 0x52*/
/*--Global CR2A--*/
outportb(SuperIO_A0,0x2A);
Temp=inportb(SuperIO_A1);
Temp=Temp | 0xFC; /*set pin 121-128*/
outportb(SuperIO_A1, Temp);
/*--Configure Logical Device 7 GPIO Port1--*/
outportb(SuperIO_A0, 0x07);
outportb(SuperIO_A1,0x07);/*GP15 GP16 gp17*/
/*--CR30--*/
```

```
outportb(SuperIO_A0,0x30);
outportb(SuperIO_A1,0x01); /*Enable GPIO Port*/
/*--CR60--*/ /*Select FDC I/O Base*/
Temp=DIO_A0;
Temp>>=8; /* right shift 8 bit*/
outportb(SuperIO_A0,0x60);
outportb(SuperIO_A1,Temp);/*0x03*/
/*--CR61--*/ /*Select FDC I/O Base*/
Temp=DIO_A0;
Temp&=0x0FF;
outportb(SuperIO_A0, 0x61);
outportb(SuperIO_A1, Temp);/*0x00*/
/*--CRF0--*/ /*Configure logical device 1, configuration register CRF0*/
outportb(SuperIO_A0, 0xF0);
outportb(SuperIO_A1, 0xFF);
gotoxy(6,6);
printf("!!aimb-350 DIO Testing!!);
gotoxy(6,7);
printf("-->Set jumpers on CN23(1-2)and CN23(13-14)");
gotoxy(6,8);
printf("-->Press any key to start.");
while(!bioskey(1));
/*--CRF0--*/
outportb(SuperIO_A0,0xF0);
outportb(SuperIO_A1,0x0F);/*set GP10-GP17 I/O=>"1" is input, "0"is
output=>(10101010)*/
/*--CRF1--*/
outportb(SuperIO_A0,0XF1);
outportb(SuperIO_A1,0x00);
/*--CRF1--*/
outportb(SuperIO_A0,0xF1);
Temp=inportb(SuperIO_A1);
```

```
Temp=Temp | 0x00;
/*printf (“Temp=”%s,Temp);*/
if(Temp!=0x0B)
ErrFlag=1;
/*----------------------------------------------------------*/
/*--Exit extended function mode--*/
outportb(SuperIO_A0,0xAA);
if(ErrFlag==0)
{   gotoxy(10,13);
     printf (“Testing is successful!”);
}
else
{   gotoxy(10,13);
     printf(“Testing is Failed!”);          }   }
```

Appendix B

Pin Assignments

This appendix contains information of a detailed or specialized nature. It includes:

- CRT Connector
- COM1 connector
- LPT Connector
- Audio Connector
- KB/MS Connector
- LAN2+USB1/2 Connector
- LAN1+USB3/4 Connector
- LCD/LVDS Inverter Connector
- CD-IN Connector
- Internal Speaker Connector
- LCD Connector
- DVI Connector
- Internal USB 5,6/7,8Port Connector
- SIR Connector
- Compact Flash Connector
- Primary IDE Connector
- Secondary IDE Connector
- SM Bus Connector
- Floppy Connector
- COM Connector
- Digital IO Connector
- Mini PCI Connector
- TV-Out Connector
- SATA Connector
- ATX Power Connector
- LVDS Connector
- SYSTEM/CPU FAN Connector
- AGP SLOT
- PCI SLOT
- PCIX SLOT

Appendix B Pin Assignments

B.1 CRT Connector (CN1)

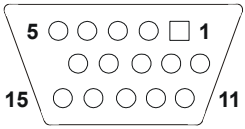


Table B.1: CRT Connector (CN1)

Description		D-SUB HD CONN.15P 90D(Blue)			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	RED	6	GND	11	NC
2	GREEN	7	GND	12	DDC DATA
3	BLUE	8	GND	13	H-SYNC
4	NC	9	NC	14	V-SYNC
5	GND	10	GND	15	DDC CLOCK

B.2 COM1 Connector(CN2)

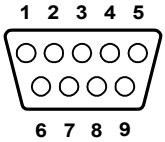


Table B.2: COM1 Connector (CN2)

Description		D-SUB CONN.9P 90D(M) (Green)	
Pin	**Signal**	**Pin**	**Signal**
1	DCD*	6	DSR*
2	RX	7	RTS*
3	TX	8	CTS*
4	DTR*	9	RI
5	GND		

*: LOW ACTIVE

B.3 LPT1 Connector(CN3)

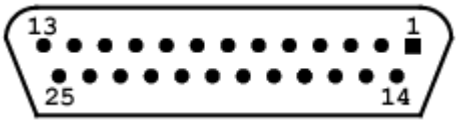


Table B.3: Primary IDE connector (CN3)

Description		D-SUB CONN.25P 90D(M)	
Pin	**Signal**	**Pin**	**Signal**
1	STROBE*	14	ATUO FEED*
2	PD0	15	ERROR*
3	PD1	16	INT*
4	PD2	17	SELECT IN*
5	PD3	18	GND
6	PD4	19	GND
7	PD5	20	GND
8	PD6	21	GND
9	PD7	22	GND
10	ACK*	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SELECT		

*: LOW ACTIVE

B.4 Audio Connector (CN4)

Table B.4: Audio Connector (CN4)

Description		Phone Jack 13P 90D(F)	
Pin	**Signal**	**Pin**	**Signal**
A1	GND	A2	LINE IN (R)
A3	NC	A4	NC
A5	LINE IN (L)		
B1	GND	B2	LINE OUT (R)
B3	NC	B4	NC
B5	LINE OUT (L)	12	GND
C1	GND	C2	MIN_IN2
C3	NC	C4	NC
C5	MIC_IN1		

B.5 Keyboard + PS/2 Mouse Connector (CN5)

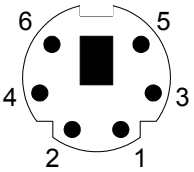


Table B.5: Keyboard + PS/2 Mouse Connector (CN5)

Description		MINI DIN 6P 90D(F)
Pin	**Signal**	
1	KB DATA	
2	MS DATA	
3	GND	
4	+5V	
5	KB CLOCK	
6	MS CLOCK	

B.6 LAN2 USB3/4 Connector (CN6)

Table B.6: LAN2 USB3/4 Connector (CN6)

Description		Phone Jack RJ45 + USB*2 90D(F)	
Pin	**Signal**	**Pin**	**Signal**
1	LAN_V25	2	LAN_MDI0+
3	LAN_MDI0-	4	LAN_MDI1+
5	LAN_MDI1-	6	LAN_MDI2+
7	LAN_MDI2-	8	LAN_MDI3+
9	LAN_MDI3-	10	GND
11	LINK_LED#	12	ACT_LED#
13	LINK1000_LED#	14	LINK100_LED#
15	USB1_5V	16	USBD1-
17	USBD1+	18	GND
19	USB2_5V	20	USBD2-
21	USBD2+	22	GND
23	GND	24	GND
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND

B.7 LAN1 USB1/2 Connector(CN7)

Table B.7: LAN1 USB1/ 2 Connector(CN7)

Description		Phone Jack RJ45 + USB*2 90D(F)	
Pin	**Signal**	**Pin**	**Signal**
1	LAN_V25	2	LAN_MDI0+
3	LAN_MDI0-	4	LAN_MDI1+
5	LAN_MDI1-	6	LAN_MDI2+
7	LAN_MDI2-	8	LAN_MDI3+
9	LAN_MDI3-	10	GND
11	LINK_LED#	12	ACT_LED#
13	LINK1000_LED#	14	LINK100_LED#
15	USB1_5V	16	USBD1-
17	USBD1+	18	GND
19	USB2_5V	20	USBD2-
21	USBD2+	22	GND
23	GND	24	GND
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND

B.8 LCD/LVDS INVERTER Connector(CN8)

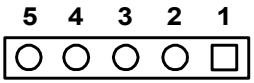


Table B.8: LCD/LVDS INVERTER Connector(CN8)

Description		WAFER BOX 2.0mm 5P 180D
Pin	**Signal**	
1	+12V	
2	GND	
3	BKLTEN	
4	VBR	
5	+5V	

B.9 CD-IN Connector (CN9)

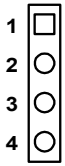


Table B.9: CD-IN Connector (CN9)

Description	WAFER BOX 2.54mm 4P 180DMALE
Pin	**Signal**
1	CDIN-R
2	GND
3	GND
4	CDIN-L

B.10 Internal Speaker Connector (CN10)

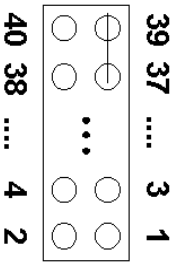
Table B.10: Internal Speaker Connector(CN10)

Description	WAFER BOX 2.0mm 4P 180D
Pin	**Signal**
1	OUTA-
2	OUTA+
3	OUTB+
4	OUTB-

B.11 LCD Connector(CN11)

Table B.11: LCD Connector (CN11)

Description		DF13-40DP-1.25V	
Pin	**Signal**	**Pin**	**Signal**
1	VDDSAFE_5V	2	VDDSAFE_5V
3	GND	4	GND
5	VDDSAFE_3V	6	VDDSAFE_3V
7	VCON	8	GND
9	PD0-B0	10	PD1-B1
11	PD2-B2	12	PD3_B3
13	PD4-B4	14	PD5_B5
15	PD6-B6	16	PD7_B7
17	PD8_G0	18	PD9_G1
19	PD10_G2	20	PD11_G3
21	PD12_G4	22	PD13_G5
23	PD14_G6	24	PD15_G7
25	PD16_R0	26	PD17_R1
27	PD18_R2	28	PD19_R3
29	PD20_R4	30	PD21_R5
31	PD22_R6	32	PD23_R7
33	GND	34	GND
35	SHFCLK	36	FLM
37	M	38	LP
39	EN_BKL	40	ENVEE



B.12 DVI Connector (CN12)

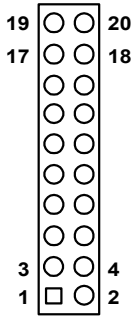


Table B.12: DVI Connector(CN12)

Description		**DF13-20DP 1.25mm**	
Pin	**Signal**	**Pin**	**Signal**
1	TMDS_C0#	2	VCC_DVI
3	TMDS_C0	4	TMDS_CK#
5	GND	6	TMDS_CK
7	TMDS_C1#	8	GND
9	TMDS_C1	10	MDVI_CLK
11	GND	12	MDVI_DATA
13	TMDS_C2#	14	HP_DET
15	TMDS_C2	16	MI2C_DATA
17	PD8	18	MI2C_CLK
19	NC	20	NC

B.13 USB5/6/USB7/8 Connector (CN13, CN14)

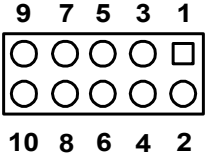


Table B.13: USN5/6/USB7/8 Connector(CN13,CN14)

Description		Pin HEADER 5*2 180D 2.54mm	
Pin	**Signal**	**Pin**	**Signal**
1	USB VCC	2	USB VCC
3	DATA1-	4	DATA2-
5	DATA1+	6	DATA2+
7	USB GND	8	USB GND
9	USB GND	10	USB GND

B.14 SIR Connector (CN15)

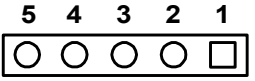


Table B.14: SIR Connector(CN15)

Description	Wafer-Box 5-pin 2.54mm
Pin	**Signal**
1	+5V
2	CIR RX
3	IR RX
4	GND
5	IR TX

B.15 Compact Flash Connector(CN16)

Table B.15: Compact Flash Connector(CN16)

Description		HEADER FOR CF Type II 50-pin 90D(M)	
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	IDE_SDD3
3	IDE_SDD4	4	IDE_SDD5
5	IDE_SDD6	6	IDE_SDD7
7	IDE_SDCS1*	8	GND
9	GND	10	GND
11	GND	12	GND
13	VCC	14	GND
15	GND	16	GND
17	GND	18	IDE_SDA2
19	IDE_SDA1	20	IDE_SDA0
21	IDE_SDD0	22	IDE_SDD1
23	IDE_SDD2	24	NC
25	GND	26	NC
27	IDE_SDD11	28	IDE_SDD12
29	IDE_SDD13	30	IDE_SDD14
31	IDE_SDD15	32	IDE_SDCS3*
33	NC	34	IDE_SDIOR*
35	IDE_SDIOW*	36	WE*
37	IDE_IRQ15	38	VCC
39	CSEL*	40	NC
41	IDE_RST*	42	IDE_SLORDY
43	NC	44	REG
45	IDE_SDACTIVE*	46	IDE_SATASET
47	IDE_SDD8	48	IDE_SDD9
49	IDE_SDD10	50	GND

*: LOW ACTIVE

B.16 Primary IDE Connector(CN17)

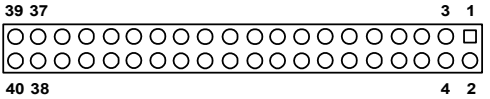


Table B.16: Primary IDE Connector(CN17)

Description	Box-Header 40-Pin 2.54mm (Blue)		
Pin	**Signal**	**Pin**	**Signal**
1	IDE-RST*	2	GND
3	IDE_PDD7	4	IDE_PDD8
5	IDE_PDD6	6	IDE_PDD9
7	IDE_PDD5	8	IDE_PDD10
9	IDE_PDD4	10	IDE_PDD11
11	IDE_PDD3	12	IDE_PDD12
13	IDE_PDD2	14	IDE_PDD13
15	IDE_PDD1	16	IDE_PDD14
17	IDE_PDD0	18	IDE_PDD15
19	GND	20	NC
21	IDE_PDDREQ	22	GND
23	IDE_PDIOW*	24	GND
25	IDE_PDIOR*	26	GND
27	IDE_PIORDY	28	IDE_PCSEL
29	IDE_PDDACK*	30	GND
31	IDE_IRQ14	32	NC
33	IDE_PAD1	34	IDE_PATADET
35	IDE_PAD0	36	IDE_PAD2
37	IDE_PDCS1*	38	IDE_PDCS3*
39	IDE_PDACTIVE*	40	GND

*: LOW ACTIVE

B.17 Secondary Slave IDE Connector(CN18)

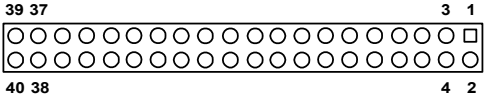


Table B.17: Secondary Slave IDE Connector(CN18)

Description		Box-Header 40-Pin 2.54mm (Black)	
Pin	**Signal**	**Pin**	**Signal**
1	IDE-RST*	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	NC
21	IDE_DREQ	22	GND
23	IOW*	24	GND
25	IOR*	26	GND
27	CHRDY	28	NC
29	IDE DACK*	30	GND
31	IDE_IRQ	32	NC
33	A1	34	DMA33/66
35	A0	36	A2
37	CS0*	38	CS1*
39	ACTIVE*	40	GND

*: LOW ACTIVE

B.18 SM BUS Connector(CN19)

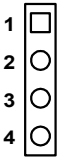


Table B.18: SM BUS Connector(CN19)

Description	Wafer-Box 4-Pin 2.0mm
Pin	**Signal**
1	GND
2	SMB DAT
3	SMB CLK
4	5V/+3.3V

B.19 FDD Connector (CN20)

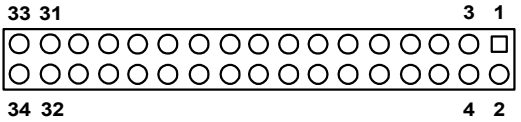


Table B.19: FDD Connector (CN20)

Description	Box-Header 34-Pin 2.54mm		
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	DRVDENA
3	GND	4	NC
5	GND	6	NC
7	GND	8	INDEX
9	GND	10	MTR A*
11	GND	12	DS B*
13	GND	14	DS A*
15	GND	16	MTR B*
17	GND	18	DIR
19	GND	20	STEP*
21	GND	22	WDATA*
23	GND	24	WGATE*
25	GND	26	TRAK0*

Table B.19: FDD Connector (CN20)

Description	Box-Header 34-Pin 2.54mm		
Pin	**Signal**	**Pin**	**Signal**
27	GND	28	WR*
29	GND	30	RDATA*
31	GND	32	HDSEL*
33	GND	34	DSKCHG*

*: LOW ACTIVE

B.20 COM2 Connector (CN21)

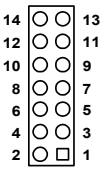


Table B.20: COM2 Connector(CN21)

Description	Box-Header 14-Pin 2.0mm		
Pin	**Signal**	**Pin**	**Signal**
1	NDCD*	2	DSR*
3	RX	4	RTS*
5	TX	6	CTS*
7	DTR*	8	RI
9	GND	10	GND
11	TXD485P	12	TXD485N
13	RXD485P	14	RXD485N

*: LOW ACTIVE

B.21 COM3~4 Connector (CN22)

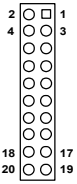


Table B.21: COM3~4 Connector (CN22)

Description		Box-Header 20-Pin 2.0mm	
Pin	**Signal**	**Pin**	**Signal**
1	DCD3*	2	DSR3*
3	RX3	4	RTS3*
5	TX3	6	CTS3*
7	DTR3*	8	RI_3
9	GND	10	GND
11	DCD4*	12	DSR4*
13	RX4	14	RTS4
15	TX4	16	CTS4*
17	DTR4*	18	RI_4
19	GND	20	GND

*: LOW ACTIVE

B.22 Digital IO Connector (CN23)

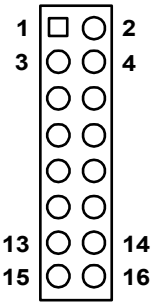


Table B.22: Digital IO Connector (CN23)

Description		Pin-Header 16-Pin 2.54mm	
Pin	**Signal**	**Pin**	**Signal**
1	DIO-IN0	2	5V
3	DIO_IN1	4	DIOOUT0
5	DIO_IN2	6	GND
7	DIO_IN3	8	DIOOUT1
9	GND	10	12V
11	NC	12	NC
13	DIO_OUT3	14	GND
15	DIO_OUT4	16	12V

*: LOW ACTIVE

B.23 TV OUT Connector(CN25)

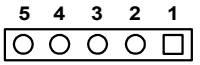


Table B.23: TV OUT Connector(CN25)

Description	Wafer-Box 5-Pin 2.54mm
Pin	**Signal**
1	Y-OUT
2	C-OUT
3	GND
4	GND
5	CVBS_OUT

B.24 SATA Connector (SATA1/SATA2)

Table B.24: SATA Connector (SATA1/SATA2)

Description		DIP 7P 180D(M) 1.27mm	
Pin	**Signal**	**Pin**	**Signal**
1	GND	5	SATA_RXN
2	SATA_TXP	6	SATA_RXP
3	SATA_TXN	7	GND
4	GND	8	NC

B.25 ATX Power Connector (ATX1)

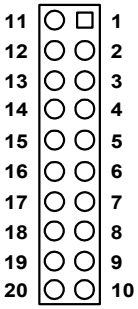


Table B.25: ATX Power Connector (ATX1)

Description		Wafer ATX PWR 20-Pin	
Pin	**Signal**	**Pin**	**Signal**
1	3.3V	11	3.3V
2	3.3V	12	-12V
3	GND	13	GND
4	+5V	14	PSON*
5	GND	15	GND
6	+5V	16	GND
7	GND	17	GND
8	PWROK	18	-5V
9	5VSB	19	+5V
10	+12V	20	+5V

*: LOW ACTIVE

B.26 LVDS Connector (VCN1)

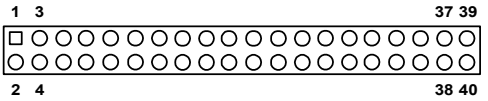


Table B.26: LVDS Connector (VCN1)

Description		DF 13-40P	
Pin	**Signal**	**Pin**	**Signal**
1	VDDSAFE	2	VDDSAFE
3	GND	4	GND
5	VDDSAFE	6	VDDSAFE
7	LVDS0_N0	8	LVDS1_N0
9	LVDS0-P0	10	LVDS1_P0
11	GND	12	GND
13	LVDS0_N1	14	LVDS1_N1
15	LVDS0_P1	16	LVDS_P1
17	GND	18	GND
19	LVDS0_N2	20	LVDS1_N2
21	LVDS0_P2	22	LVDS_P2
23	GND	24	GND
25	LVDS0_CLKN	26	LVDS1_CLKN
27	LVDS0_CLKP	28	LVDS1_CLKP
29	GND	30	GND
31	LVDS_DDCPCLK	32	LVDS_DDCPDATA
33	GND	34	GND
35	LVDS0_N3	36	LVDS1_N3
37	LVDS0_P3	38	LVDS1_P3
39	NC	40	LVDS_VCON

B.27 SYSTEM/CPU FAN Control Conn. (FAN1/FAN2)

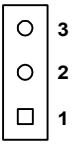


Table B.27: SYSTEM/CPU FAN Control Connector(FAN1/FAN2)

Pin	Signal
1	FAN_PWM CONTROL
2	+12V
3	FAN DETECT

B.28 AGP SLOT (AGP1)

Table B.28: AGP SLOT (AGP1)

Pin	Signal	Pin	Signal
A1	+12V	B1	OVRCNT#
A2	TYPEDET#	B2	+5V
A3	NC	B3	+5V
A4	USB-	B4	USB+
A5	GND	B5	GND
A6	AGP_INTA#	B6	AGP_INTB#
A7	AGP_RST#	B7	AGP_CLK66M
A8	AGP_GNT#	B8	AGP_REQ#
A9	3.3V	B9	3.3V
A10	AGP_ST1	B10	AGP_ST0
A11	RESERVE	B11	AGP_ST2
A12	AGP_PIPE#	B12	AGP_RBF#
A13	GND	B13	GND
A14	AGP_WBF#	B14	RESERVE
A15	AGP_SBA1	B15	AGP_SBA0
A16	3.3V	B16	3.3V
A17	AGP_SBA3	B17	AGP_SBA2
A18	AGP_SB_STB#	B18	AGP_SB_STB
A19	GND	B19	GND
A20	AGP_SBA5	B20	AGP_SBA4
A21	AGP_SBA7	B21	AGP_SBA6

Table B.28: AGP SLOT (AGP1)

Pin	Signal	Pin	Signal
A22	RESERVE	B22	RESERVE
A23	GND	B23	GND
A24	RESERVE	B24	3.3VSB
A25	3.3V	B25	3.3V
A26	AGP_AD30	B26	AGP_AD31
A27	AGP_AD28	B27	AGP_AD29
A28	3.3V	B28	3.3V
A29	AGP_AD26	B29	AGP_AD27
A30	AGP_AD24	B30	AGP_AD25
A31	GND	B31	GND
A32	AGP_ADSTB1#	B32	AGP_ADSTB1
A33	AGP_C/BE3#	B33	AGP_AD23
A34	VDDQ	B34	VDDQ
A35	AGP_AD22	B35	AGP_AD21
A36	AGP_AD20	B36	AGP_AD19
A37	GND	B37	GND
A38	AGP_AD18	B38	AGP_AD17
A39	AGP_AD16	B39	AGP_C/BE2#
A40	VDDQ	B40	VDDQ
A41	AGP_FRAME#	B41	AGP_IRDY#
A42	RESERVE	B42	3.3V_AUX
A43	GND	B43	GND
A44	RESERVE	B44	RESERVE
A45	3.3V	B45	3.3V
A46	AGP_TRDY#	B46	AGP_DEVSEL#
A47	AGP_STOP#	B47	1.8V
A48	AGP_PME#	B48	AGP_PERR#
A49	GND	B49	GND
A50	AGP_PAR#	B50	AGP_SERR#
A51	AGP_AD15	B51	AGP_C/BE1#
A52	VDDQ	B52	VDDQ
A53	AGP_AD13	B53	AGP_AD14
A54	AGP_AD11	B54	AGP_AD12
A55	GND	B55	GND
A56	AGP_AD9	B56	AGP_AD10
A57	AGP_C/BE0#	B57	AGP_AD8

Table B.28: AGP SLOT (AGP1)

Pin	Signal	Pin	Signal
A58	VDDQ	B58	VDDQ
A59	AGP_ADSTB0#	B59	AGP_ADSTB0
A60	AGP_AD6	B60	AGP_AD7
A61	GND	B61	GND
A62	AGP_AD4	B62	AGP_AD5
A63	AGP_AD2	B63	AGP_AD3
A64	VDDQ	B64	VDDQ
A65	AGP_AD0	B65	AGP_AD1
A66	AGP_VREFCG	B66	AGP_VREFCG

*: LOW ACTIVE

B.29 PCI SLOT Connector (PCI1)

Table B.29: PCI SLOT Connector (PCI1)

Pin	Signal	Pin	Signal
A1	GND (TRST#)	B1	-12V
A2	+12V	B2	GND (TCK)
A3	VCC5V (TMS)	B3	GND
A4	VCC5V (TDI)	B4	NC (TDO)
A5	VCC5V	B5	VCC5V
A6	INTF#	B6	VCC5V
A7	INTH#	B7	INTG#
A8	VCC5V	B8	INTE#
A9	GNT#1 (REV)	B9	PCICLK1 (PRSNT#1)
A10	VCC5V	B10	PREQ#1 (REV)
A11	GNT#2 (REV)	B11	PCICLK2 (PRSNT#2)
A12	GND	B12	GND
A13	GND	B13	GND
A14	3VSB	B14	PREQ#2 (REV)
A15	RST#	B15	GND
A16	VCC5V	B16	PCICLK
A17	GNT#0	B17	GND
A18	GND	B18	REQ#0
A19	PCI_PME#	B19	VCC5V
A20	AD30	B20	AD31
A21	VCC3	B21	AD29
A22	AD28	B22	GND
A23	AD26	B23	AD27
A24	GND	B24	AD25
A25	AD28	B25	VCC3V
A26	IDSEL	B26	C/BE#3
A27	VCC3V	B27	AD23
A28	AD22	B28	GND
A29	AD20	B29	AD21
A30	GND	B30	AD19
A31	AD18	B31	VCC3V
A32	AD16	B32	AD17
A33	VCC3V	B33	C/BE#2
A34	FRAME#	B34	GND

Table B.29: PCI SLOT Connector (PCI1)

Pin	Signal	Pin	Signal
A35	GND	B35	IRDY#
A36	TRDY#	B36	VCC3V
A37	GND	B37	DEVSEL#
A38	STOP#	B38	GND
A39	VCC3V	B39	LOCK#
A40	SMBCLK	B40	PERR#
A41	SMBDAT	B41	VCC3V
A42	GND	B42	SERR#
A43	PAR	B43	VCC3V
A44	AD15	B44	C/BE#1
A45	VCC3V	B45	AD14
A46	AD13	B46	GND
A47	AD11	B47	AD12
A48	GND	B48	AD10
A49	AD9	B49	GND
A50	NC	B50	NC
A51	NC	B51	NC
A52	C/BE#0	B52	AD8
A53	VCC3V	B53	AD7
A54	AD6	B54	VCC3V
A55	AD4	B55	AD5
A56	GND	B56	AD3
A57	AD2	B57	GND
A58	AD0	B58	AD1
A59	VCC5V	B59	VCC5V
A60	REQ64#	B60	ACK64#
A61	VCC5V	B61	VCC5V
A62	VCC5V	B62	VCC5V

*: LOW ACTIVE

B.30 PCIX SLOT Connector (PCIX1)

Table B.30: PCIX SLOT Connector (PCIX1)

Pin	Signal	Pin	Signal
A1	PX_TRST#	B1	-12V
A2	+12V	B2	PX_TCK
A3	PX_TMS	B3	GND
A4	PX_TDI	B4	NC (TDO)
A5	VCC5V	B5	VCC5V
A6	PX_INTB#	B6	VCC5V
A7	PX_INTD#	B7	PX_INTC#
A8	VCC5V	B8	PX_INTA#
A9	NC	B9	NC
A10	PX_VIO	B10	NC
A11	NC	B11	NC
A12	GND	B12	GND
A13	NC	B13	NC
A14	3VSB	B14	NC
A15	PX_RST#	B15	GND
A16	PX_VIO	B16	PX_CLK0
A17	PX_GNTD#	B17	GND
A18	GND	B18	PX_REQD#
A19	PCI_PME#	B19	PX_VIO
A20	PX_AD30	B20	PX_AD31
A21	VCC3V	B21	PX_AD29
A22	PX_AD28	B22	GND
A23	PX_AD26	B23	PX_AD27
A24	GND	B24	PX_AD25
A25	PX_AD24	B25	VCC3V
A26	PX1_IDSEL	B26	PX_CBE#3
A27	VCC3V	B27	PX_AD23
A28	PX_AD22	B28	GND
A29	PX_AD20	B29	PX_AD21
A30	GND	B30	PX_AD19
A31	PX_AD18	B31	VCC3V
A32	PX_AD16	B32	PX_AD17
A33	VCC3V	B33	PX_CBE#2
A34	PX_FRAME#	B34	GND

Table B.30: PCIX SLOT Connector (PCIX1)

Pin	Signal	Pin	Signal
A35	GND	B35	PX_IRDY#
A36	PX_TRDY#	B36	VCC3V
A37	GND	B37	PX_DEVSEL#
A38	PX_STOP#	B38	PX_PCIXCAP (REV)
A39	VCC3V	B39	PX_PLOCK#
A40	SMBCLK (SDONE)	B40	PX_PERR#
A41	SMBDAT (SB0#)	B41	VCC3V
A42	SMBCLK (SDONE)	B42	PX_SERR#
A43	PX_PAR	B43	VCC3V
A44	PX_AD15	B44	PX_CBE#1
A45	VCC3V	B45	PX_AD14
A46	PX_AD13	B46	GND
A47	PX_AD11	B47	PX_AD12
A48	GND	B48	PX_AD10
A49	PX_AD9	B49	PX_M66EN
A50	NC	B50	NC
A51	NC	B51	NC
A52	PX_CBE#0	B52	PX_AD8
A53	VCC3V	B53	PX_AD7
A54	PX_AD6	B54	VCC3V
A55	PX_AD4	B55	PX_AD5
A56	GND	B56	PX_AD3
A57	PX_AD2	B57	GND
A58	PX_AD0	B58	PX_AD1
A59	PX_VIO	B59	PX_VIO
A60	PX_REQ64#	B60	PX_ACK64#
A61	VCC5V	B61	VCC5V
A62	VCC5V	B62	VCC5V
A63	GND	B63	NC
A64	PX_CBE#7	B64	GND
A65	PX_CBE#5	B65	PX_CBE#6
A66	PX_VIO	B66	PX_CBE#4
A67	PX_PAR64	B67	GND
A68	PX_VIO	B68	PX_AD63
A69	GND	B69	PX_AD61
A70	PX_AD60	B70	PX_VIO

Table B.30: PCIX SLOT Connector (PCIX1)

Pin	Signal	Pin	Signal
A71	PX_AD58	B71	PX_AD59
A72	GND	B72	PX_AD57
A73	PX_AD56	B73	GND
A74	PX_AD54	B74	PX_AD55
A75	PX_VIO	B75	PX_AD53
A76	PX_AD52	B76	GND
A77	PX_AD50	B77	PX_AD51
A78	GND	B78	PX_AD49
A79	PX_AD48	B79	PX_VIO
A80	PX_AD46	B80	PX_AD47
A81	GND	B81	PX_AD45
A82	PX_AD44	B82	GND
A83	PX_AD42	B83	PX_AD43
A84	PX_VIO	B84	PX_AD41
A85	PX_AD40	B85	GND
A86	PX_AD38	B86	PX_AD39
A87	GND	B87	PX_AD37
A88	PX_AD36	B88	PX_VIO
A89	PX_AD34	B89	PX_AD35
A90	GND	B90	PX_AD33
A91	PX_AD32	B91	GND
A92	NC	B92	NC
A93	GND	B93	NC
A94	NC	B94	GND

*: LOW ACTIVE

B.31 PCIX SLOT Connector (PCIX2)

Table B.31: PCIX SLOT Connector (PCIX2)

Pin	Signal	Pin	Signal
A1	PX_TRST#	B1	-12V
A2	+12V	B2	PX_TCK
A3	PX_TMS	B3	GND
A4	PX_TDI	B4	NC (TDO)
A5	VCC5V	B5	VCC5V
A6	PX_INTB#	B6	VCC5V
A7	PX_INTD#	B7	PX_INTC#
A8	VCC5V	B8	PX_INTA#
A9	NC	B9	NC
A10	PX_VIO	B10	NC
A11	NC	B11	NC
A12	GND	B12	GND
A13	NC	B13	NC
A14	3VSB	B14	NC
A15	PX_RST#	B15	GND
A16	PX_VIO	B16	PX_CLK0
A17	PX_GNTA#	B17	GND
A18	GND	B18	PX_REQA#
A19	PCI_PME#	B19	PX_VIO
A20	PX_AD30	B20	PX_AD31
A21	VCC3V	B21	PX_AD29
A22	PX_AD28	B22	GND
A23	PX_AD26	B23	PX_AD27
A24	GND	B24	PX_AD25
A25	PX_AD24	B25	VCC3V
A26	PX1_IDSEL	B26	PX_CBE#3
A27	VCC3V	B27	PX_AD23
A28	PX_AD22	B28	GND
A29	PX_AD20	B29	PX_AD21
A30	GND	B30	PX_AD19
A31	PX_AD18	B31	VCC3V
A32	PX_AD16	B32	PX_AD17
A33	VCC3V	B33	PX_CBE#2
A34	PX_FRAME#	B34	GND

Table B.31: PCIX SLOT Connector (PCIX2)

Pin	Signal	Pin	Signal
A35	GND	B35	PX_IRDY#
A36	PX_TRDY#	B36	VCC3V
A37	GND	B37	PX_DEVSEL#
A38	PX_STOP#	B38	PX_PCIXCAP (REV)
A39	VCC3V	B39	PX_PLOCK#
A40	SMBCLK (SDONE)	B40	PX_PERR#
A41	SMBDAT (SB0#)	B41	VCC3V
A42	SMBCLK (SDONE)	B42	PX_SERR#
A43	PX_PAR	B43	VCC3V
A44	PX_AD15	B44	PX_CBE#1
A45	VCC3V	B45	PX_AD14
A46	PX_AD13	B46	GND
A47	PX_AD11	B47	PX_AD12
A48	GND	B48	PX_AD10
A49	PX_AD9	B49	PX_M66EN
A50	NC	B50	NC
A51	NC	B51	NC
A52	PX_CBE#0	B52	PX_AD8
A53	VCC3V	B53	PX_AD7
A54	PX_AD6	B54	VCC3V
A55	PX_AD4	B55	PX_AD5
A56	GND	B56	PX_AD3
A57	PX_AD2	B57	GND
A58	PX_AD0	B58	PX_AD1
A59	PX_VIO	B59	PX_VIO
A60	PX_REQ64#	B60	PX_ACK64#
A61	VCC5V	B61	VCC5V
A62	VCC5V	B62	VCC5V
A63	GND	B63	NC
A64	PX_CBE#7	B64	GND
A65	PX_CBE#5	B65	PX_CBE#6
A66	PX_VIO	B66	PX_CBE#4
A67	PX_PAR64	B67	GND
A68	PX_VIO	B68	PX_AD63
A69	GND	B69	PX_AD61
A70	PX_AD60	B70	PX_VIO

Table B.31: PCIX SLOT Connector (PCIX2)

Pin	Signal	Pin	Signal
A71	PX_AD58	B71	PX_AD59
A72	GND	B72	PX_AD57
A73	PX_AD56	B73	GND
A74	PX_AD54	B74	PX_AD55
A75	PX_VIO	B75	PX_AD53
A76	PX_AD52	B76	GND
A77	PX_AD50	B77	PX_AD51
A78	GND	B78	PX_AD49
A79	PX_AD48	B79	PX_VIO
A80	PX_AD46	B80	PX_AD47
A81	GND	B81	PX_AD45
A82	PX_AD44	B82	GND
A83	PX_AD42	B83	PX_AD43
A84	PX_VIO	B84	PX_AD41
A85	PX_AD40	B85	GND
A86	PX_AD38	B86	PX_AD39
A87	GND	B87	PX_AD37
A88	PX_AD36	B88	PX_VIO
A89	PX_AD34	B89	PX_AD35
A90	GND	B90	PX_AD33
A91	PX_AD32	B91	GND
A92	NC	B92	NC
A93	GND	B93	NC
A94	NC	B94	GND

*: LOW ACTIVE

Appendix C

System Assignments

This appendix contains information of a detailed nature. It includes:

- System I/O ports
- 1st MB memory map
- DMA channel assignments
- Interrupt assignments

Appendix C System Assignments

C.1 System I/O Ports

Table C.1: System I/O ports

Addr. range (Hex)	Device
00-0F	Master DMA controller
20-21F	Master Interrupt controller
40-5F	Timer/Counter
60-6F	Keyboard controller
(60h)	KBC Data
(61h)	Misc Functions & Spkr Ctrl
(64h)	KBC Command/Status
70-77	RTC/COMS/NMI-Disable
78-7F	-available for system use-
80	-reserved-(debug port)
81-8F	DMA Page Registers
90-91	-available for system use-
92	System Control
93-9F	-available for system use-
A0-A1H	Slave Interrupt Controller
C0-DF	Slave DMA Controller
E0-FF	-available for system use-
100-1EF	-available for system use-
170-178	Secondary IDE Control
1F0-1F8	Primary IDE Control
200-20F	Game Port
295-296	Hardware Monitor
2E8-2EF	COM4
2F8-2FF	COM2
378-37F	Parallel Port (Standard & AFF)
3C0-3CF	EGA
3D0-3DF	VGA
3E8-3EF	COM3
3F0-3F1	Configuration Index/Data
3F0-3F7	Floppy Controller
3F8-3FF	COM1
778-77A	Parallel Port (ECP Extensions) (Port 378+400)

Table C.1: System I/O ports

Addr. range (Hex)	Device
CF8-CFB	PCI Configuration Address
CFC-CFF	PCI Configuration Data
D00-FFFF	-available for system use-

C.2 1st MB memory map

Table C.2: 1st MB memory map

Addr. range (Hex)	Device
F0000h - FFFFFh	System ROM
*D0000h - EFFFFh	Unused (reserved for Ethernet ROM)
C0000h - CFFFFh	Expansion ROM (for VGA BIOS)
B8000h - BFFFFh	CGA/EGA/VGA text
B0000h - B7FFFh	Unused
A0000h - AFFFFh	EGA/VGA graphics
00000h - 9FFFFh	Base memory

* If Ethernet boot ROM is disabled (Ethernet ROM occupies about 16 KB)

* E0000 - EFFFF is reserved for BIOS POST

C.3 DMA channel assignments

Table C.3: DMA channel assignments

Channel	Function
0	Available
1	Available (audio)
2	Floppy disk (8-bit transfer)
3	Available (parallel port)
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

* Parallel port ECP mode DMA select 1 or 3

C.4 Interrupt assignments

Table C.4: Interrupt assignments

Interrupt#	Interrupt source
IRQ 0	Interval timer
IRQ 1	Keyboard
IRQ 2	Interrupt from controller 2 (cascade)
IRQ 3	COM2
IRQ 4	COM1
IRQ 5	COM4
IRQ 6	FDD
IRQ 7	LPT1
IRQ 8	RTC
IRQ 9	Reserved (audio)
IRQ 10	COM3
IRQ 11	Reserved for watchdog timer
IRQ 12	PS/2 mouse
IRQ 13	INT from co-processor
IRQ 14	Primary IDE
IRQ 15	Secondary IDE for CFC

Appendix D

Intel Speedstep Technology

- Introduction and Installation

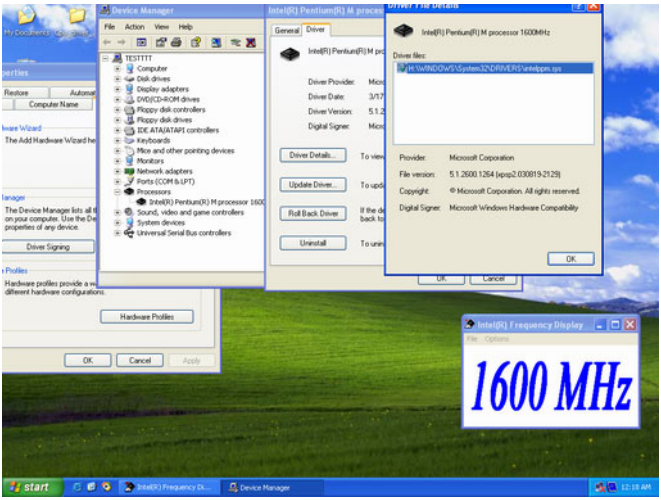
Appendix D Intel Speedstep Technology

D.1 Intel® Pentium® M SpeedStep instruction

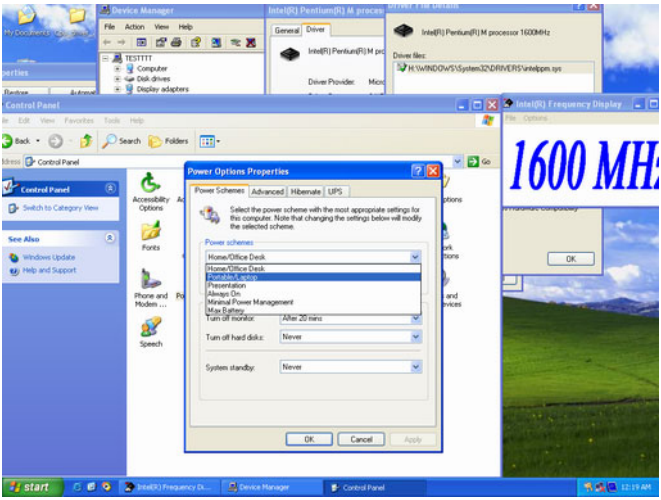
Mobile Intel® Pentium® M processors with Enhanced Intel SpeedStep® technology lets users customize the performance of their PC. Enhanced Intel SpeedStep technology provides the Pentium M processor with a flexible, multi-point operating mode, completely self managed, and with a very low CPU and memory overhead, which optimizes its power and performance according to demand.

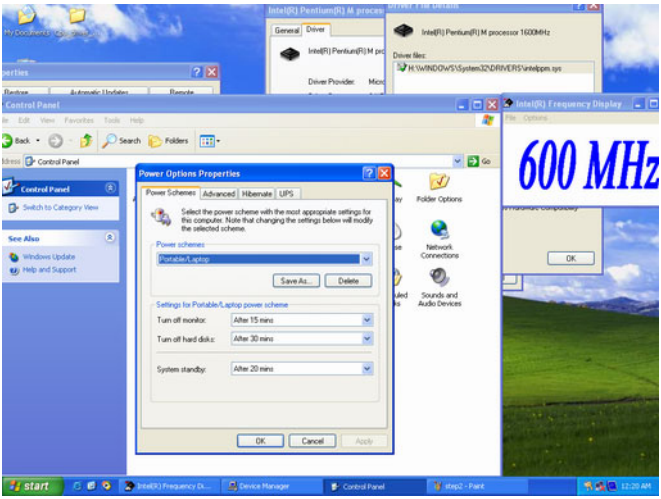
Advantech products with Intel® Pentium® M processors support speed stepping features in Windows XP, To implement the speed stepping feature under Windows XP, please follow the following steps:

Step 1. Update “Processor" driver by using "cpu_driver_winxp.zip”

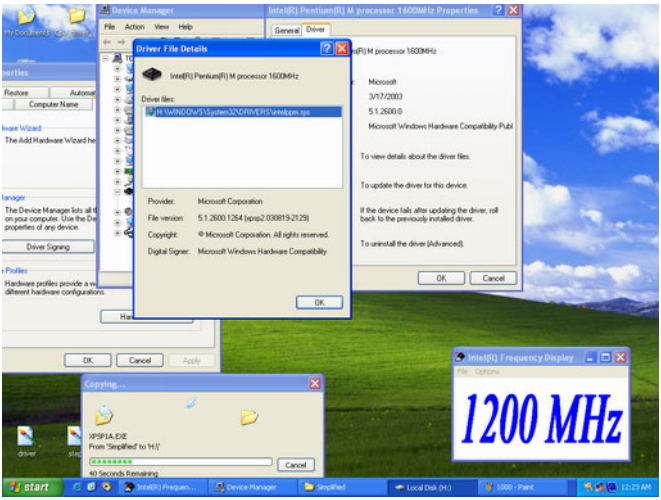


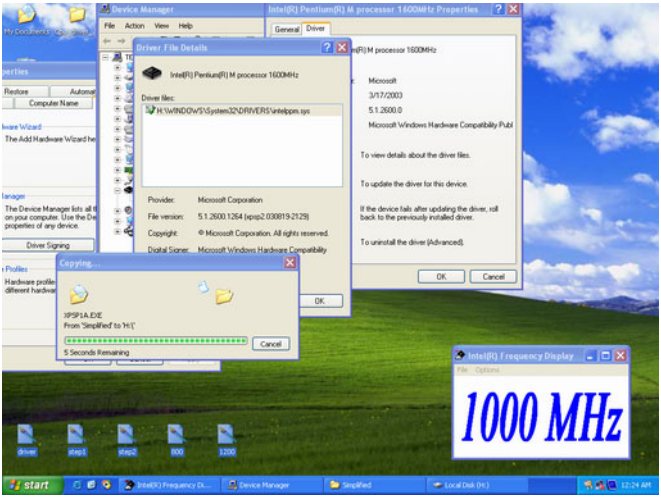
Step 2. Change “Power schemes" to "Portable/Laptop”

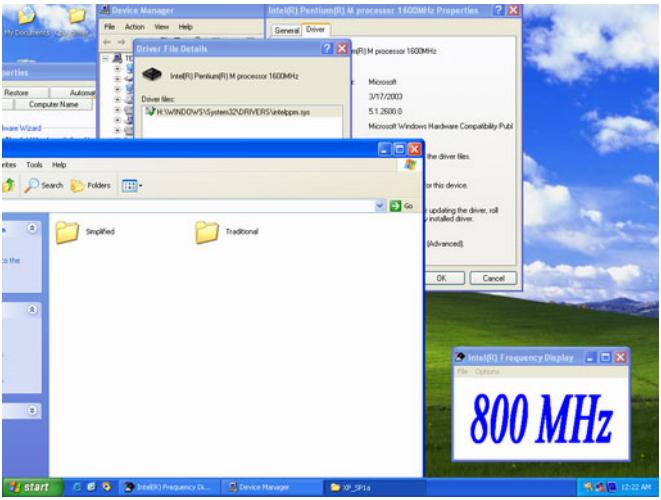

Power Options Properties
1600 MH


Power Options Properties
600 MHz

Step 3. Discover the different CPU freq. by using the Frequency Display utility







The Result of Pentium M speed stepping:

1.1 G---600 MHz / 800 MHz / 1.1 GHz (Intel® Pentium® M)

1.6 G---600 MHz / 800 MHz / 1.0 GHz /1.2 GHz / 1.4 GHz / 1.6 GHz(Intel® Pentium® M)