

# **SOM-ETX**

**Board and  
Design Specification**

*Your ePlatform Partner*

**ADVANTECH**

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## General Information

This chapter explains the concept of the SOM-ETX (System-on-Module) module. It also gives the reasons why SOM-ETX can give the most value and benefits to embedded system applications.

## 1.1 Overview

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SOM-ETX is a new form factor to develop embedded systems. It allows easier system design by eliminating costly connectors and adapter cables. This makes it easier to develop a customized system with an off-the-shelf embedded PC and reduce the time to market of your product.

This standard is a reference for dimension and pinout of SOM-ETX boards. Different SOM-ETX CPU boards will provide a different set of features. Please refer the manual of your SOM-ETX CPU board for details or consult your supplier for supported features. SOM-ETX boards are only interchangeable as long as they provide the same features (e.g. 2 channel LVDS video output). In order to maintain interchangeability consult your supplier application engineers for assistance.

For SOM-ETX basic function please refer the SOM-ETX evaluation schematic. This can help engineers to understand some features better. Some non-standard features like the panel interface are not usable without external parts. Also parts for EMV/ ESD protection are not included on the SOM-ETX CPU board. No SOM-ETX signals need any external Pull-up or Pull down.

To create a backplane for SOM-ETX boards, it's highly recommended to have experience with PCI device development. Also experience with signal integrity and timing for the layout of your backplane is recommended.

Please contact your supplier for advice. In addition to this document, the user should refer to the following industry standard specifications:

ISA Bus specification P996 rev 1.1

PCI Bus specification Rev 2.1

USB specification 1.1

ATX specification

HIROSE Catalog “FX8 SERIES”

## **Connector Assignments and Descriptions**

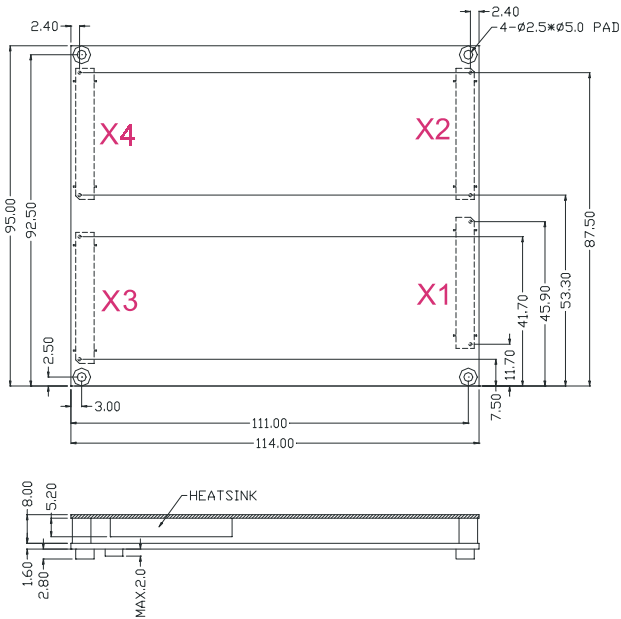
This chapter tells how to set up the SOM-ETX module hardware. It includes instructions on connecting peripherals, switches and indicators. Make sure you read all the safety precautions before you begin the installation procedure.e:

## 2.1 Connector Locations

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The board has a number of connectors that allow you to configure your system to suit your application.

The tables below shows the function of each of the board's connectors:



*Figure 2.1: SOM-ETX Connectors*

## 2.2 Pin Assignments

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## 2.2.1 Pin Assignments (X1 Connector)

**Table 2.1: Connector X1 (PCI-Bus, USB, Sound)**

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ#3	10	GNT#3
11	GNT#2	12	3V
13	REQ12	14	GNT#1
15	REQJ1	16	3V
17	GNT#0	18	N.C.
19	VCC	20	VCC
21	SERIRQ	22	REQ#0
23	AD0	24	3V
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE#0	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SNDL
47	AD15	48	ASGND
49	CBE#1	50	SNDR
51	VCC	52	VCC
53	PAR	54	SERR#
55	GPERR#	56	N.C.
57	PME#	58	USB20
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB30
63	IRDY#	64	STOP#
65	FRAME#	66	USB21
67	GND	68	GND
69	AD16	70	CBE#2
71	AD17	72	USB31
73	AD19	74	AD18
75	AD20	76	USB00
77	AD22	78	AD21
79	AD23	80	USB10
81	AD24	82	CBE#3
83	VCC	84	VCC
85	AD25	86	AD26
87	AD28	88	USB01
89	AD27	90	AD29
91	AD30	92	USB11
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

## 2.2.2 Pin Assignments (X2 Connector)

**Table 2.2: Connector X2 (ISA-Bus)**

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	MASTER#
7	SD12	8	DREQ7
9	SD11	10	DACK#7
11	SD10	12	DREQ6
13	SD9	14	DACK#6
15	SD8	16	DREQ5
17	MEMW#	18	DACK#5
19	MEMR#	20	DREQ0
21	LA17	22	DACK#0
23	LA18	24	IRQ14
25	LA19	26	IRQ15
27	LA20	28	IRQ12
29	LA21	30	IRQ11
31	LA22	32	IRQ10
33	LA23	34	IO16#
35	GND	36	GND
37	SBHE#	38	M16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA2	44	TC
45	SA3	46	DACK#2
47	SA4	48	IRQ3
49	SA5	50	IRQ4
51	VCC	52	VCC
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	REFSH#
63	SA11	64	DREQ1
65	SA12	66	DACK#1
67	GND	68	GND
69	SA13	70	DREQ3
71	SA14	72	DACK#3
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	VCC	84	VCC
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	NOWS#
91	DREQ2	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	IOCHK#	98	RSTDRV
99	GND	100	GND

## Pin Assignments (X3 Connector)

**Table 2.3: Connector X3 (VGA, LCD, Video, COM1, COM2, LPT/ Floppy, Irda, Mouse, Keyboard)**

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	N.C.	10	DDDA
11	LCDDO16	12	LCDDO18
13	LCDDO17	14	LCDDO19
15	GND	16	GND
17	LCDDO13	18	LCDDO15
19	LCDDO12	20	LCDDO14
21	GND	22	GND
23	LCDDO8	24	LCDDO11
25	LCDDO9	26	LCDDO10
27	GND	28	GND
29	LCDDO4	30	LCDDO7
31	LCDDO5	32	LCDDO6
33	GND	34	GND
35	LCDDO1	36	LCDDO3
37	LCDDO0	38	LCDDO2
39	VCC	40	VCC
41	LTGIO2 (reserved)	42	LTGIO0 (reserved)
43	LTGIO1 (reserved)	44	BLON#
45	BIASON	46	DIGON
47	COMP	48	Y
49	SYNC	50	C
51	LPT/FLPY#	52	N.C.
53	VCC	54	GND
55	/STB_DRV0	56	/AFD_DENSEL
57	FIR (reserved)	58	PD7
59	IRRX	60	/ERR_HDSEL#
61	IRTX	62	PD6
63	RXD2	64	/INIT_DIR#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	/SLIN_STEP#
71	DCD2#	72	PD4_DSKCHG#
73	DSR2#	74	PD3_RDATA#
75	CTS2#	76	PD2_WP#
77	TXD2#	78	PD1_TRK0#
79	RI2#	80	PD0_INDEX#
81	VCC	82	VCC
83	RXD1	84	/ACK_DRV1
85	RTS1#	86	/BUSY_MOT1
87	DTR1#	88	PE_WDATA#
89	DCD1#	90	/SLCT_WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

## 2.2.3 Pin Assignments (X4 Connector)

**Table 2.4: Connector X4 (IDE1, IDE2, ETHERNET, FEATURE)**

Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH	10	LILED
11	WDTRIG	12	ACTLED
13	ROMBCS#	14	SPPEDLED
15	EXT_PRG	16	12CLK
17	VCC	18	VCC
19	OVCR#	20	GPCS#
21	N.C.	22	I2DAT
23	SMBCLK	24	SMBDATA
25	SIDE_CS3#	26	N.C.
27	SIDE_CS1#	28	DASP_S
29	SIDE_A2	30	PIDE_CS3#
31	SIDE_A0	32	PIDE_CS1#
33	GND	34	GND
35	PDIAG_S	36	PIDE_A2
37	SIDE_A1	38	PIDE_A0
39	SIDE_INTRO	40	PIDE_A1
41	N.C.	42	N.C.
43	SIDE_AK#	44	PIDE_INTRO
45	SIDE_RDY	46	PIDE_AK#
47	SIDE_IOR#	48	PIDE_RDY
49	VCC	50	VCC
51	SIDE_IOW#	52	PIDE_IOR#
53	SIDE_DRQ	54	PIDE_IOW#
55	SIDE_D15	56	PIDE_DRQ
57	SIDE_D0	58	PIDE_D15
59	SIDE_D14	60	PIDE_D0
61	SIDE_D1	62	PIDE_D14
63	SIDE_D13	64	PIDE_D1
65	GND	66	GND
67	SIDE_D2	68	PIDE_D13
69	SIDE_D12	70	PIDE_D2
71	SIDE_D3	72	PIDE_D12
73	SIDE_D11	74	PIDE_D3
75	SIDE_D4	76	PIDE_D11
77	SIDE_D10	78	PIDE_D4
79	SIDE_D5	80	PIDE_D10
81	VCC	82	VCC
83	SIDE_D9	84	PIDE_D5
85	SIDE_D6	86	PIDE_D9
87	SIDE_D8	88	PIDE_D6
89	N.C.	90	N.C.
91	RXD-	92	PIDE_D8
93	RXD_	94	SIDE_D7
95	TXD-	96	PIDE_D7
97	TXD+	98	HDRST#
99	GND	100	GND

## 2.3 Safety precautions

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**Warning!**



*For your safety and that of the equipment, always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on; sensitive electronic components can be damaged by a sudden rush of power.*

**Caution!**



*Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.*

## 2.4 Pin Descriptions

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### 2.4.1 Connector X1 (PCI-Bus, USB, Sound)

**N.C.** Not connected.

**GND** Ground.

**VCC +5V** power supply.

**3V +3.3V** voltage generated onboard for supply of external devices up to 500mA.

**PCICLK1..4** PCI clock outputs for external PCI devices.

**REQ#0..3** Bus Request signals of PCI Masters. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.

**GNT#0..3** Grant signals to PCI Masters. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.

**AD0..31** PCI Address and Data Bus Lines. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.

**CBE#0..3** PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.

**PAR** Parity bit of PCI bus. It is the even parity bit across PAD[31:0] and CBE#[3:0].

**SERR#** System Error or PCI Clock RUN. If the Northbridge detects parity errors in DRAMs, it will assert SERR# to notify the system.

**GPERR#** Parity Error. For PCI operation per exception granted by PCI 2.1 specification.

**PME#** Power management event.

**LOCK#** Lock Resource Signal. This pin indicates the PCI master or the bridge intends to do exclusive transfers.

**DEVSEL#** Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.

**TRDY#** Target Ready. This pin indicates the target is ready to complete the current data phase of transaction.

**IRDY#** Initiator Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.

**STOP#** Stop. This signal indicates the target is requesting the master to stop the current transaction.

**FRAME#** Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. It will be as an output driven by Northbridge on behalf of CPU, or as an input during PCI master access.

**PCIRST#** PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.

**INTA#, INTB#, INTC#, INTD#** PCI interrupt pin A, B, C and D.

**USB00, USB01** Universal Serial Bus Port 0. These are the serial data pair for USB Port 0. (0->neg., 1-> pos.).

**USB10, USB11** Universal Serial Bus Port 1. These are the serial data pair for USB Port 1. (0->neg., 1-> pos.).

**SNDL** Line-level stereo output left. This pin can drive a 5k Ohm AC load.

**SNDR** Line-level stereo output right. This pin can drive a 5k Ohm AC load.

**AUXAL** Auxiliary A input left. Normally intended for connection to an internal or external CD-ROM analog output.

**AUXAR** Auxiliary A input right. Normally intended for connection to an internal or external CD-ROM analog output.

**MIC** Microphone input.

**ASGND** Analog ground for soundcontroller.

**ASVCC** Analog supply voltage for soundcontroller.

**SERIRQ** Serial interrupt request. This pin is used to support the serial interrupt protocol.

### **2.4.2 Connector X2 (ISA-Bus)**

**SD0..15** These signals provide data bus bits 0 to 15 for the peripheral devices. All 8-bit devices use SD0 0..7 for data transfers. The 16-bit devices will use SD0..15. To support 8-bit devices, the data on SD8..15 will be gated to SD0..7 during 8-bit transfers to these devices. 16-bit CPU cycles will be converted to two 8-bit cycles for 8-bit peripheral automatically.

**SA0..19** Address bits 0 through 15 are used to address I/O devices and address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA17..23 allow access of up to 16MB of memory. SA0..19 are gated on the ISA-bus when BALE is high and latched on falling edge of BALE.

**SBHE#** Bus High Enable indicates a transfer of data on the upper byte of the data bus (SD8..15). 16 bit I/O devices use SBHE to condition data bus buffers tied to SD8..15.

**BALE** Bale is an active high pulse which is generated at the beginning of any bus cycle initiated by a CPU module. It indicates when the SA0..19, LA17..23, AEN, and SBHEJ signals are valid.

**AEN** AEN is an active high output that indicates a DMA transfer cycle, only resources with a active DACK#? signal should respond to the command lines when AEN is high.

**MEMR#** MEMR# instructs memory devices to drive data onto the data bus. MEMR# is active on all memory read cycles.

**SMEMR#** SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active on memory read cycles to addresses below 1MB.

**MEMW#** MEMW# instructs memory devices to store the data present on the data bus. MEMW# is active on all memory write cycles.

**SMEMW#** SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active on all memory write cycles to address below 1MB.

**IOR#** I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or DMA controller. IOR# is inactive (high) during refresh cycles.

**IOW#** I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or DMA controller. IOW# is inactive (high) during refresh cycles.

**IOCHK#** is an active low input signal which indicates that an error has taken place on the module bus.

If I/O checking is enabled on the CPU module, an IOCHK# assertion by a peripheral device generates an NMI to the processor.

**IOCHRDY** The I/O channel ready is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles initiated by the CPU are 4 wait states for 8 bit peripherals and 1 wait state for 16 bit peripherals. One wait state is inserted as a default for all DMA cycles. Any peripheral that cannot present read data or strobe in write data in this amount of time use IOCHRDY to extend these cycles.

This signal should not be held low for more than 2.5 us for normal operation. Any extension to more than 2,5 us does not guarantee proper DRAM memory contents because memory refresh is stopped while IOCHRDY is low.

**M16#** The M16# signal determines when a 16 bit to 8 bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module is requesting a 16 bit memory cycle and the M16# line is high. If M16# is high, 16 bit CPU cycles are converted into two 8 bit cycles on the bus automatically. If M16# is low, an access to peripherals is done 16 bit wide.

**IO16#** The IO16# signal determines when a 16 bit to 8 bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module is requesting a 16 bit I/O cycle and the IO16# line is high. If IO16# is high, 16 bit CPU cycles are converted into two 8 bit cycles on the bus automatically. If IO16# is low, an access to peripherals is done 16 bit wide.

**REFSH#** is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us to prevent loss of DRAM data.

**NOWS#** The Zero wait state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default the CPU inserts 4 wait states for 8 bit transfers and 1 wait state for 16 bit transfers.

**MASTER#** This signal is used with a DRQ line to gain control of the system bus. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, a bus master may pull MASTER# low, which will allow it to control the system address, data and control lines. After MASTER# is low, the bus master must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. If this signal is held low for more than 15 us, system memory may be lost because of lack of refresh.

**SYSCLK** SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with 40-60 % duty cycle. Slower and higher frequencies may be supplied by different CPU modules. This signal is supplied at all times except when the CPU module is in sleep mode.

**OSC** is supplied by CPU modules. It has a nominal frequency of 14,31818 MHz and a duty cycle of 40- 60 %. This signal is supplied at all times except when the CPU module is in sleep mode.

**RESETDRV** This active high output is system reset generated from CPU modules to reset external devices.

**DREQ0, 1, 2, 3, 5, 6, 7** The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU modules DAM controllers. DREQ0..3 are used for transfers between 8 bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16 bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on CPU modules.

**DACK#0, 1, 2, 3, 5, 6, 7** DMA acknowledge 0..3 and 5..7 are used to acknowledge DMA requests. They are low active.

**TC** The active high output TC indicates that one of the DMA channels has transferred all data.

**IRQ3..7, 9..15** These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on CPU modules. All IRQ signals are active high. The interrupt requests are prioritized, with IRQ9 through IRQ12 and IRQ14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An inter-

rupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt service routine).

### **2.4.3 Connector X3 (VGA, LCD, Video, COM1, COM2, IrDA, Mouse, Keyboard, LPT or Floppy)**

**HSY** Horizontal Sync: This output supplies the horizontal synchronization pulse to the monitor. It is normally not needed for flat panels.

**VSY** Vertical Sync: This output supplies the vertical synchronization pulse to the monitor. It is normally not needed for flat panels.

**R, G, B** CRT analog video outputs.

**DDCK, DDDA** These two pins are functionally suitable for a DDC interface between the graphics controller chip and the CRT monitor.

**BIASON** Controls panel contrast voltage.

**DIGON** Controls panel digital power.

**BLON#** Controls backlight level by means of pulse width modulation.

**LTGIO0..2** General purpose I/Os, can be used for LCD DDC detection.

**SYNC** Composite Sync for SCART PAL TV's that use the EURO AV Connector. It is fed to the "Video In" pin of this connector to provide a signal that the TV can overlay the RGB data onto. This pin may also be used as a general I/O pin for controlling video switch, or for the other Internal timing signals including Hsync, Vsync, etc.

**Y DAC Output:** outputs either Y (Luminance) for S-Video, or Red for RGB Video (SCART).

**C DAC Output:** outputs either C (Color/Chrominance) for S-Video, or Green for RGB Video.

**COMP DAC Output:** outputs either Composite Video, or Blue for RGB Video.

**LCDDO0..19** LCD data output pins for one channel LVDS support.

**DTR1#, DTR2#** Active low data terminal ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link.

**RI1#, RI2#** This active low input is for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem.

**TXD1, TXD2** Transmitter serial data output from Serial port.

**RXD1, RXD2** Receiver serial data input.

**CTS1#, CTS2#** This active low input for serial ports . Handshake signal which notifies the UART that the modem is ready to receive data.

**RTS1#, RTS2#** This active low output for serial port. Handshake signal notifies the modem that the UART is ready to transmit data.

**DCD1#, DCD2#** This active low input for serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem.

**DSR1#, DSR2#** This active low input is for serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link.

**KBDAT** This is the bidirectional keyboard data signal.

**KBCLK** This is the keyboard clock signal.

**MSDAT** This is the bidirectional mouse data signal.

**MSCLK** This is the mouse clock signal.

**IRTX, IRRX** Infrared transmit and receive pin.

**LPT/FLPY#** This signal decides whether LPT or floppy interface will be used with ETX-interface. The following signals are multifunctional and depending on level of signal LPT/FLPY# LPT-interface (LPT/FLPY#: high, default) or floppy-interface (LPT/FLPY#: low) will be used.

**/STB\_DRV0 LPT/FLPY# (high):** This active low pulse is used to strobe the printer data into the printer.

**LPT/FLPY# (low):** Drive select 0.

**/AFD\_DENSEL**

**LPT/FLPY# (high):** This active low output causes the printer to automatically feed one line after each line is printed.

**LPT/FLPY# (low):** Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected.

**PD0\_INDEX#**

**LPT/FLPY# (high):** This bidirectional parallel data bus is used to transfer information between CPU and peripherals.

**LPT/FLPY# (low):** This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.

**PD1\_TRK0#**

**LPT/FLPY# (high):** Refer to PD0.

**LPT/FLPY# (low):** This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.

**PD2\_WP#**

**LPT/FLPY# (high):** Refer to PD0.

**LPT/FLPY# (low):** This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected.

**PD3\_RDATA#**

**LPT/FLPY# (high):** Refer to PD0.

**LPT/FLPY# (low):** The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.

**PD4\_DSKCHG#**

**LPT/FLPY# (high):** Refer to PD0.

**LPT/FLPY# (low):** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of location base+7.

**PD6\_MOT0**

**LPT/FLPY# (high):** Refer to PD0.

**LPT/FLPY# (low):** These active-low outputs select motor drives 0.

**PD5/PD7** Refer to PD0

**/ERR\_HDSEL#**

**LPT/FLPY# (high):** This active low signal indicates an error situation at the printer.

**LPT/FLPY# (low):** This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.

**/INIT\_DIR#**

**LPT/FLPY# (high):** This active low signal is used to initiate the printer when low.

**LPT/FLPY# (low):** This active low output determines the direction of the head movement (low = step-in, high = step-out).

**/SLIN\_STEP#**

**LPT/FLPY# (high):** This active low signal selects the printer.

**LPT/FLPY# (low):** This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.

### **/ACK\_DRV1**

**LPT/FLPY#** (high): This active low output from the printer indicates it has received the data and is ready to receive new data.

**LPT/FLPY#** (low): Active low, output select drives 1.

### **/BUSY\_MOT1**

**LPT/FLPY#** (high): This signal indicates the printer is busy and not ready to receive new data.

**LPT/FLPY#** (low): These active-low outputs select motor drives 1.

### **PE\_WDATA#**

**LPT/FLPY#** (high): This signal indicates that the printer is out of paper.

**LPT/FLPY#** (low): This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.

### **/SLCT\_WGATE#**

**LPT/FLPY#** (high): This active high output from the printer indicates that it has power on.

**LPT/FLPY#** (low): This active-low, high-drive output enables the write circuitry of the selected disk drive.

**FIR** For internal use only! Do not connect!

## **2.4.4 Connector X4 (IDE 1, IDE2, Ethernet, Feature)**

**PIDE\_D0..15** Primary IDE ATA Data Bus. These are the Data pins connected to Primary Channel.

**SIDE\_D0..15** Secondary IDE ATA Data Bus. These are the Data pins connected to Secondary Channel.

**PIDE\_A0..2** Primary IDE ATA Address Bus. These are the Address pins connected to Primary Channel.

**SIDE\_A0..2** Secondary IDE ATA Address Bus. These are the Address pins connected to Secondary Channel.

**PIDE\_CS1#** IDE Chip Select 1 for Primary Channel 0. This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.

**PIDE\_CS3#** IDE Chip Select 3 for Primary Channel 1. This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.

**SIDE\_CS1#** IDE Chip Select 1 for Secondary Channel 0. This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.

**SIDE\_CS3#** IDE Chip Select 3 for Secondary Channel 1. This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.

**PIDE\_DRQ** Primary IDE DMA Request for IDE Master. This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.

**SIDE\_DRQ** Secondary IDE DMA Request for IDE Master. This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.

**PIDED\_AK#** Primary IDE DACK# for IDE Master. This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.

**SIDED\_AK#** Secondary IDE DACK# for IDE Master. This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.

**PIDE\_RDY** Primary IDE Ready. This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can deassert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different function. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE Busmaster to strobe the input data. In write cycle, this pin is used by IDE device to notify IDE Busmaster as DMA Ready (DDMARDY#).

**SIDE\_RDY** Secondary IDE Ready. This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can deassert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions. In read cycle, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE Busmaster to strobe the input data. In write cycles, this pin is used by IDE device to notify IDE Busmaster as DMA Ready (DDMARDY#).

**PIDE\_IOR#** Primary IDE IOR# Command. This is the IOR# command output pin to notify the Primary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.

In read cycle, this pin is used by IDE Busmaster to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Busmaster will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.

**SIDE\_IOR#** Secondary IDE IOR# Command. This is the IOR# command output pin to notify the Secondary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different function. In read cycle, this pin is used by IDE Busmaster to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Busmaster will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.

**PIDE\_IOW#** Primary IDE IOW# Command. This is the IOW# command output pin to notify the Primary IDE device that the available Write Data is already asserted by IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin is driven by IDE Busmaster to force IDE device to terminate current transaction. After receiving this input, IDE device will deassert DRQ to STOP current transaction.

**SIDE\_IOW#** Secondary IDE IOW# Command. This is the IOW# command output pin to notify the Secondary IDE device that the available Write Data is already asserted by IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin is driven by IDE Busmaster to force IDE device to terminate current transaction. After receiving this input, IDE device will deassert DRQ to STOP current transaction.

**DASP\_S** Time-multiplexed, open collector output which indicates that a drive is active, or that a slave drive is present on Secondary IDE channel. Necessary for using IDE master/slave-mode on Secondary IDE channel.

**PDIAG\_S** Output by the drive if it is jumpered in the slave mode; input to the drive if it is jumpered in the master mode. The signal indicates to a master that the slave has passed its internal Diagnostic command. Necessary for using IDE master/slave-mode on Secondary IDE channel.

**HDRST#** Low active hardware reset (RSTDRV inverted).

**PIDE\_INTRQ** Primary channel interrupt signal.

**SIDE\_INTRQ** Secondary channel interrupt signal.

**TXD-,TXD+** Analog Twisted Pair Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface directly with an isolation transformer.

**RXD-,RXD+** Analog Twisted Pair Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation.

**ACTLED** The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.

**LILED** The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.

**SPEEDLED** The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.

**SPEAKER** This is the speaker output signal, connected to a speaker between output and VCC.

**BATT** 3 V backup cell input. BATT should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VBATT = 2.4 - 3.3 V)

**PWGIN** High active input for the ETX-PC indicates that power from the power supply is ready. It can also be used as low active reset input signal.

**I2CLK, I2DAT** Clock and data line of I2C-Bus. Switched I/O-lines with approximate 10kHz. Do not use as multi master. Intended for I2C and other simple I/O-devices.

**SMBDATA, SMBCLK** Clock and data line of SM-Bus. For future use. Do not use today.

**KBINH** Keyboard Inhibit.

**5V\_SB** Power supply pin for internal Suspend circuit. AT or ATX hardware configure input.

**PS\_ON** Remove All Circuit Power Except Internal Suspend Circuit. PS\_ON will become active high to disable all the circuits except internal Suspend circuit

**PWRBTN#** Power Button Input. This input is used to support the ACPI Power Button function.

**OVCR#** Over current detect input. This pin is used to monitor the USB power over current.

**ROMKBCS#** For internal use only!

**EXT\_PRG** For internal use only!

**WDTRIG** For internal use only!

**GPCS#** For internal use only!



## **Mechanical Characteristics**

This chapter gives the mechanical specifications for the SOM-db4400

## 3.1 Mechanical Characteristics

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### 3.1.1 Dimensions of SOM-ETX

The SOM-ETX without heat sink is up to 12 mm thick, and the top components are up to 8 mm high. The bottom components are a maximum of 2 mm high, while the headers X1 to X4 (FX8-100P-SV) on SOM-ETX are 2.8mm high. These will be connected to their counterpart receptacles (FX8-100S) on the Carrier Board.

Please read section 2.2 regarding receptacles for the FX8-100S specification and chapter 2.3 about Carrier Board layout for accurate placement of receptacles FX8-100S.

The heatspreader offered on some SOM-ETX modules, gives the ETX board thermal coupling. Heat dissipation devices such as the heat sink with fan or heat pipe, may need to be connected to the heatspreader.

The dissipation of heat will fluctuate between different CPU boards. Please refer to the SOM-ETX manual for exact specifications and cooling requirements of the heatspreader.

### 3.1.2 Specification of receptacles FX8-100S

The receptacles for SOM-ETX connection allow the base to be stacked at different heights.

Manufacturer	Order number	Resulting height between backplane and SOM-ETX board
HIROSE	FX8-100S-SV	3 + 0.3/-0.2 mm

Current capacity: 0.4 A per pin

Rated voltage: 100 V AC

Insulation resistance: 10 ohms or greater @ 250 V DC

Withstand voltage: 300V AC r.m.s.

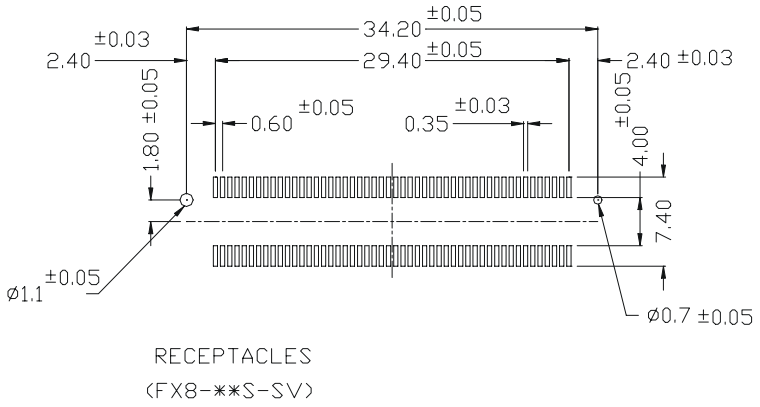
Contact resistance: 45 ohms or less @ 100 mA DC

Insulation: PPS resin (Light brown, UL94V-0)

Contacts: Phosphor bronze

(Contacts and leads - gold plating)

### 3.1.3 Footprint of receptacles FX8-100S





CHAPTER

# 4

## Literature and Standards Links

## LITERATURE, STANDARDS, LINKS

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It is not in the responsibility of the ETX specification to supply information about standard PC technology. Nevertheless, for your convenience, we herewith include a selection of information sources.

### 4.1 ISA-Bus, Standard PS/2 - Connectors

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- ISA System Architecture, Addison-Wesley Publishing Company, ISBN 0-201-40996-8
- AT BUS Design IEEE P996 Compatible, Edward Solari, Annabooks San Diego CA. ISBN 0-929392-08-6  
[www.annabooks.com](http://www.annabooks.com)
- PC Handbook, Sixth Edition, John P. Choisser and John O. Foster, Annabooks San Diego CA. ISBN 0-929392-36-1, [www.annabooks.com](http://www.annabooks.com)
- AT IBM Technical Reference Vol. 1&2, 1985
- ISA Bus Specifications and Application Notes, January 30, 1990, Intel
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989
- Personal Computer Bus Standard P996, Draft D2.00, January 18, 1990, IEEE Inc.
- ePanorama PC Hardware Linkpage <http://www.us-epanorama.net/pc/>

### 4.2 RS232C

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EIA-232-E Interface between data terminal equipment and data circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)

National Semiconductor's Interface Data Book includes applications notes. These notes are also available online at <http://www.national.com/>. A search engine is provided to search the text of the available application notes. Entering "232" as search criteria should generate a current list of related application notes.

### **4.3 ATA**

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The ATA specification of X3T10 is available from several ftp servers.

Please search for “ata3-r6” on ftp search engines.

It’s highly recommended to have a view on “4.2 I/O cable” in this specification by using harddisks on DMA3 or PIO4-Mode.

### **4.4 USB**

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The USB specification maybe obtained from the USB Implementers Forum web site at [www.usb.org](http://www.usb.org)

### **4.5 PCI**

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The PCI local bus specification maybe obtained from the PCI Special Interest Group web site at

<http://www.pcisig.com/>.

### **4.6 ATX**

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The ATX specification maybe obtained from the Intel website.

Please go to <http://developer.intel.com/> and make quick search for ATX specification. Some other documents are available on

<http://www.teleport.com/~ffsupprt/>.

